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Analysis and Design of Power Efficient Class D Amplifier Output Stages

Joseph S. Chang, Meng-Tong Tan, Zhihong Cheng, and Yit-Chow Tong

***Abstract*—A Class D amplifier comprises a pulse width modulator and an output stage. In this paper, we analyze the power dissipation mechanisms and derive the overall power efficiency of the output stage realized using the finger and waffle layouts. We compare the relative merits of these layouts. We propose two design methodologies to determine the aspect ratios of the transistors in the output stage for optimum power efficiency (optimum for a given fabrication process, supply voltage and load resistance): 1) optimization to a *single* modulation index point and 2) optimization to a *range* of modulation indexes. For the design of an output stage with optimum power efficiency (and small IC area), we recommend optimization to a *range* of modulation indexes and a layout realized by the waffle structure. The theoretical analysis and derivations are verified on the basis of computer simulations and measurements on fabricated prototype IC's.**

***Index Terms*—Amplifier, Class D , efficiency, optimization, output stage.**

List of Parameters Used

α	W_p/W_n.
β	Gain factor (μA/V^2) of a MOS Transistor (MOST).
β_n	Gain factor of an nMOST.
β_p	Gain factor of a pMOST.
$C_{\rm GSO}$	Gate-to-source capacitance per unit gate width.
$C_{\rm GDO}$	Gate-to-drain capacitance per unit gate width.
$C_{\rm GBO}$	Gate-to-substrate capacitance per unit gate width.
C_J	Zero-biased p-n junction area capacitance.
$C_{\rm JSW}$	Zero-biased p-n junction periphery capacitance.
C_L	Output filter capacitance.
$C_{\rm ox}$	Oxide capacitance per unit gate area.
C_p	Total parasitic capacitance.
$C_{\rm pad}$	Bond pad capacitance.
D	Modulation index (V_s/V_c).
$\varepsilon_{\rm ox}$	Permittivity of the gate oxide.
f_c	Triangular signal (carrier) frequency.
f_s	Input signal frequency.
η	Efficiency of the amplifier ($\eta = P_{\rm OUT}/P_E$).
$i_{\rm DD}$	Supply current.
i_o	Load current.
I_0	Maximum output current ($V_{\rm DD}/R_L$).
$I_{\rm mean}$	Mean value of the short-circuit current.
L	Channel length of a MOST.
L_n	Channel length of an nMOST.
L_p	Channel length of a pMOST.
$L_{\rm DS}$	Length of the source or drain area.
L_o	Output filter inductance.
P_E	Total power drawn from the supply.
$P_{\rm out}$	Output power at the load.
$R_{\rm ctn}$	n-type contact resistance per contact.
$R_{\rm ctp}$	p-type contact resistance per contact.
$r_{\rm on}$	Total on-resistance of a Class D bridge output stage.
R_L	Load resistance.
R_n	Source or drain area resistance per square of an nMOST.
R_p	Source or drain area resistance per square of a pMOST.
τ	Rise or fall time of a PWM signal.
T	Tapering factor of a string of inverters .[7]
$t_{\rm ox}$	Gate oxide thickness.
μ_n	Electron mobility.
μ_p	Hole mobility.
$V_{\rm DD}$	Supply voltage.
$V_{\rm GS}$	Gate-to-source voltage.
$V_{\rm DS}$	Drain-to-source voltage.
V_s	Peak voltage of the input signal.
V_c	Peak voltage of the triangular carrier signal.
$V_{\rm th}$	Threshold voltage of a MOST.
$V_{\rm thn}$	Threshold voltage of an nMOST.
$V_{\rm thp}$	Threshold voltage of a pMOST.
W_n	Channel width of the nMOST output stage inverter.
W_p	Channel width of the pMOST output stage inverter.

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I. Introduction

There is a continuing demand including auditory prosthesis [1] and hearing instruments (aids) [2]–[6] for circuits featuring micropower, low voltage and small IC area. The Class D amplifier, depicted in Fig. 1, is often used as the power amplifier in hearing instruments due to its high efficiency (>80%) over a large modulation index range (output signal swing). Despite the recent interest in several low-voltage low-power Class D amplifier designs and architectures [3]–[6], the design and optimization (in terms of power efficiency) of the output stage of the Class D amplifier remain largely empirical: design the aspect ratio of the transistors of the output stage to be as large as tolerable so as to obtain an output stage with a low on-resistance, typically $<30\,\Omega$.

In this paper, we show that the empirical design methodology does not necessarily yield an optimized design. We analyze the power dissipation mechanisms and derive the overall power efficiency of the Class D output stage for the finger and waffle layouts. We show that there is a tradeoff between the different power dissipation mechanisms when designing the output transistor aspect ratios. We propose two novel design methodologies leading to mathematical expressions that specify the optimized aspect ratios of the output stage transistors, optimized in terms of the power efficiency for a given fabrication process, supply voltage, and load resistance.

II. Power Dissipation Mechanisms

The Class D amplifier, as depicted in Fig. 1, comprises a pulse width modulator (PWM) and a bridge output stage. The bridge output stage consists of two cascades of CMOS inverters, and the load comprises an LC filter and load resistor R_L. The power dissipation mechanisms are due to 1) parasitic capacitance $P_c = (1/2) f_c C_p V_{\rm DD}^2$; 2) short-circuit current during the transitions, $P_s = I_{\rm mean} V_{\rm DD}$; and 3) on-resistance $P_r = (1/T)_s \int_0^{T_s} i_o^2 r_{\rm on}\, dt$.

We derive the three power dissipation mechanisms for the bridge output stage (comprising two strings of N inverters) realized using the

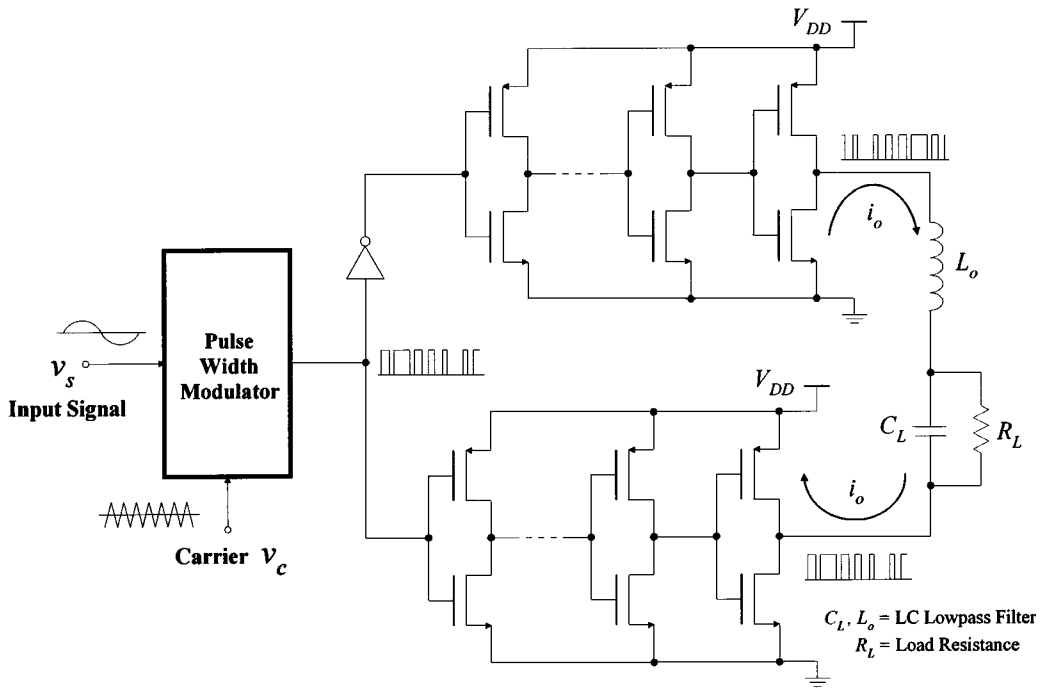

Fig. 1. Block diagram of a full-bridge output Class D power amplifier.

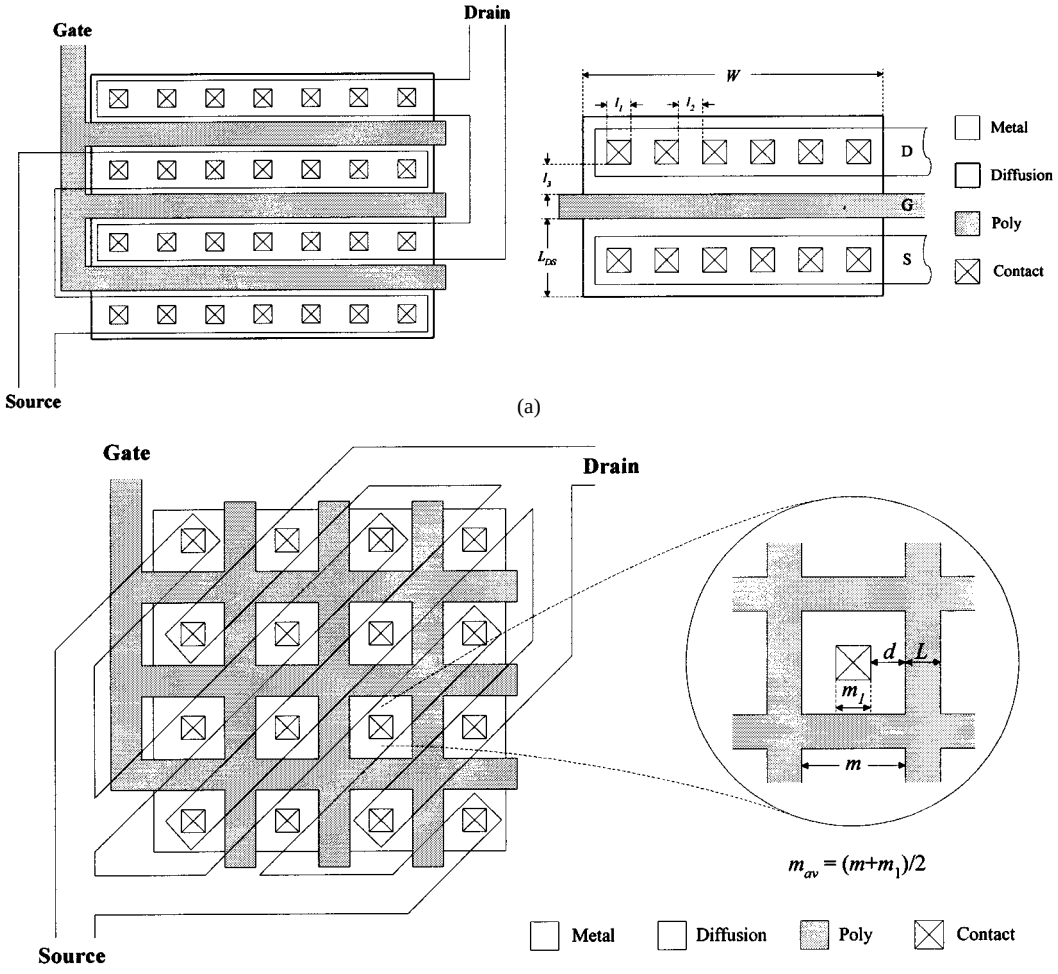

Fig. 2. IC layout of a transistor based on (a) the finger layout and (b) the waffle layout.

TABLE I
SUMMARY OF POWER DISSIPATION MECHANISMS

	Finger Layout	Waffle Layout
P_c	$\frac{1}{2}V_{DD}^2 f_c\left[2C_{pad}+(K_1+K_2)W_p\sum_{i=0}^{N-1}T^{-i}\right]$	
K_1	$2\left(1+\frac{1}{\alpha}\right)\left[C_{ox}L+(C_{GSO}+C_{GDO})\right]$	$2\left(1+\frac{1}{\alpha}\right)\left[C_{ox}L+(C_{GSO}+C_{GDO})\right]$
K_2	$2\left[\left(C_{JP}+\frac{C_{JN}}{\alpha}\right)L_{DS}+\left(1+\frac{1}{\alpha}\right)(C_{GDO}+2C_{JSW})\right]$	$2\left[\frac{m}{4}\left(C_{JP}+\frac{C_{JN}}{\alpha}\right)+\left(1+\frac{1}{\alpha}\right)(C_{GDO}+C_{JSW})\right]$
P_s	$K_3(V_{DD}-2V_{th})^3 f_c\tau W_p\sum_{i=0}^{N-1}T^{-i}$	
K_3	$\frac{1}{6}\frac{\varepsilon_{ox}\mu_p}{t_{ox}L}$	$\frac{1}{6}\frac{\varepsilon_{ox}\mu_p}{t_{ox}L}$
P_r	$\frac{1}{T_s}\int_0^{\tau_s} i_o^2(t)r_{on}dt\approx\frac{1}{2}D^2I_0^2r_{on}$	
r_{on}	$\frac{K_4+\alpha K_5}{W_p}+\frac{2K_6}{(V_{DD}-V_{th})W_p}$	$\frac{K_4+\alpha K_5}{W_p}+\frac{2K_6}{(V_{DD}-V_{th})W_p}$
K_4	$(l_1+2l_3)R_p+2(l_1+l_2)R_{ctp}$	$2\left[8mR_{ctp}+(2md/m_{av})R_p\right]$
K_5	$(l_1+2l_3)R_n+2(l_1+l_2)R_{ctn}$	$2\left[8mR_{ctn}+(2md/m_{av})R_n\right]$
K_6	$\frac{L}{\mu_p C_{ox}}$	$\frac{L}{\mu_p C_{ox}}$

finger [Fig. 2(a)] and waffle [Fig. 2(b)] layouts and summarize them in Table I. In these derivations, we have assumed that $L_n = L_p =$ minimum L and $\beta_n = \beta_p = \beta$.

Using these derivations, we shall now describe two design methodologies for designing the transistor widths W for power efficiency.

III. POWER EFFICIENCY OPTIMIZATION

We shall assume that the three power dissipation mechanisms are independent and the total power dissipation is a summation of the individual power dissipations.

A. Optimization to a Single Modulation Index

The power efficiency can be written as $\eta(W_p) = 1/[1 + F(W_p)]$ where $F(W_p) = P_c/P_{\rm out}+P_s/P_{\rm out}+P_r/P_{\rm out}$. For maximum power efficiency, we would need to satisfy the condition $\partial F(W_p/\partial W_p) = 0$. The optimized channel width for the desired single modulation index D

$$W_p = D \times \sqrt{\frac{B_1}{B_2+B_3}} \tag{1}$$

where

$$B_1 = \left(K_4 + K_5 + \frac{2K_6}{(V_{\rm DD}-V_{\rm th})}\right)\Big/ R_L,$$
$$B_2 = D^{-2}R_L f_c(K_1+K_2)\sum_{i=0}^{N-1}T^{-i}$$

and

$$B_3 = \frac{2D^{-2}K_3R_L(V_{\rm DD}-2V_{\rm th})^3}{V_{\rm DD}^2}f_c\tau\sum_{i=0}^{N-1}T^{-i}.$$

We note here that the higher the desired modulation index, the better is the maximum efficiency (the maximum efficiency being $D = 1$) but at the cost of a larger IC area due to the larger transistor W. In summary, to design an optimum power efficient Class D output stage to a given single modulation index D, fabrication process, $V_{\rm DD}$, and R_L, the W_p of the pMOS transistor in the output inverter is given by (1). For the nMOS transistor, the optimum channel width W_n is given by α. The remaining transistor widths of the preceding inverters in the Class D output stage are designed according to the tapering factor T [7]. The optimized channel width given by (1) applies to both the finger and waffle layouts.

This optimization to a single modulation index is simplistic because the signal swing in an amplifier usually varies over a range of modulation indexes. Furthermore, this simplistic optimization raises the question of how to choose the appropriate D and implies that the power efficiency of a design whose transistor width W is optimized in this manner may not be optimum over a range of modulation indexes. This is depicted in the design examples in Fig. 3.

B. Optimization to a Range of Modulation Indexes

We rewrite the power efficiency η as a function of two variables W_p and D

$$\eta(W_p, D) = \frac{P_{\rm out}}{P_{\rm out}+P_c+P_s+P_r} = \frac{x_1D^2}{x_2D^2+x_3} \tag{2}$$

where

$$x_1 = (1/2)I_0^2R_L, \qquad x_2 = (1/2)I_o^2(r_{\rm on}+R_L)$$

and

$$x_3 = P_c + P_s.$$

We can show that the average power efficiency over the range of D_1 to D_2 is

$$\eta_{\rm av}(W_p) = \frac{1}{D_2-D_1}\int_{D_1}^{D_2}(W_p, D)\,dD = \frac{1}{D_2-D_1}\{[x_4D_2 - x_4\sqrt{x_5}\tan^{-1}(D_2/x_5)] - [x_4D_1 - x_4\sqrt{x_5}\tan^{-1}(D_1/x_5)]\} \tag{3}$$

where

$$x_4 = \frac{x_1}{x_2}, \quad x_5 = \frac{x_3}{x_2}$$

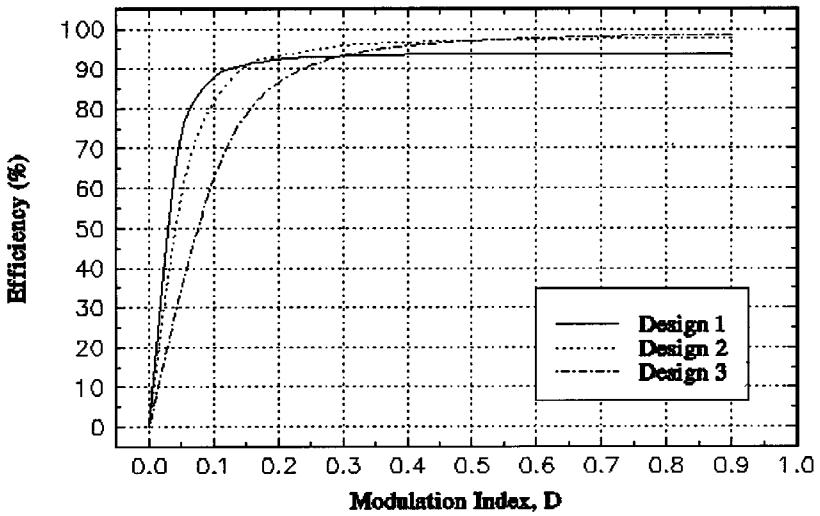

Fig. 3. Power efficiency curves of a Class D output stage optimized for maximum efficiency to a single modulation index at different modulation indexes. Design 1: $D = 0.1$; Design 2: $D = 0.25$; and Design 3: $D = 0.9$.

TABLE II
COMPARISON OF TWO CLASS D AMPLIFIER OUTPUT STAGE DESIGNS

Optimized to a *single* modulation index (eqn. 1), D = 0.9			
Layout	**Optimized W_P (μm)**	**Normalized Area**	**Average Power Dissipation**
Finger	11,913	5.8	12.1 %
Waffle	13,972	5	11.7 %
Optimized to a *range* of modulation indices (eqn. 4), D_1 = 0.025 to D_2 = 0.8			
Layout	**Optimized W_P (μm)**	**Normalized Area**	**Average Power Dissipation**
Finger	2609	1.2	7.4 %
Waffle	2965	1.0	7.0%

To determine W_p for maximum average power efficiency, we set $d\eta_{\rm av}(W_p)/dW_p = 0$

$$\Rightarrow \frac{1}{D_2 - D_1}\left\{\left[D_2\frac{dx_4}{dW_p} + \frac{D_2 x_4 \frac{dx_5}{dW_p}}{2x_5\left(1+\frac{D_2^2}{x_5}\right)} - \tan^{-1}\left(\frac{D_2}{\sqrt{x_5}}\right)\left(\frac{x_4\frac{dx_5}{dW_p}}{2\sqrt{x_5}} + \sqrt{x_5}\frac{dx_4}{dW_p}\right)\right] - \left[D_1\frac{dx_4}{dW_p} + \frac{D_1 x_4 \frac{dx_5}{dW_p}}{2x_5\left(1+\frac{D_1^2}{x_5}\right)} - \tan^{-1}\left(\frac{D_1}{\sqrt{x_5}}\right)\left(\frac{x_4\frac{dx_5}{dW_p}}{2\sqrt{x_5}} + \sqrt{x_5}\frac{dx_4}{dW_p}\right)\right]\right\} = 0. \quad (4)$$

The value of W_P in (4) may be obtained by a number of numerical methods, including the secant method [8]. In summary, to design an optimum power efficient Class D output stage for a given range of D_1 to D_2, fabrication process, $V_{\rm DD}$, and R_L, the W_p of the pMOS transistor in the output inverter is given by (4). The optimum channel width W_n is given by α and the remaining transistor widths of the preceding stages are designed according to T.

IV. DESIGN EXAMPLES, SIMULATION AND EXPERIMENTAL RESULTS

Consider a typical Class D amplifier output stage design for a hearing instrument whose application parameters are $V_{\rm DD} = 2.5$ V, $\tau = 5$ ns, $f_s = 1$ kHz, $R_L = 600\ \Omega$, $f_c = 40$ kHz, $L_o = 30$ mH, $L_n = L_p = 1.2\ \mu$m, and $C_L = 0.1\ \mu$F. For the finger layout,

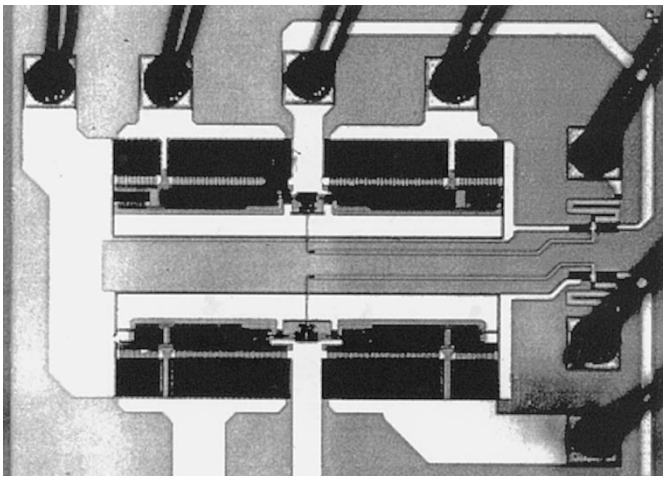

Fig. 4. The microphotograph of the two Class D output stages: top—waffle layout and bottom—finger layout.

$L_{\rm DS} = 4\ \mu$m, $l_1 = 1.6\ \mu$m, $l_2 = 1.2\ \mu$m, and $l_3 = 1.2\ \mu$m. For the waffle layout, $m = 4.8\ \mu$m, $m_1 = 3.2\ \mu$m. Note that although $V_{\rm DD} = 1.3$ V is typical in hearing instruments, it is unsuitable here due to the fabrication process used. The tapering factor was chosen to be $T = 9$.

This output stage is to be realized using a typical 1.2-μm bulk CMOS process whose parameters are $V_{\rm thn} = V_{\rm thp} = 0.75$ V, $\mu_n = 533$ cm^2/V·S, $\mu_p = 92$ cm^2/V·S, $\varepsilon_{\rm ox} = 3.45 \times 10^{-11}$ F/m, $C_{\rm ox} = 1.41 \times 10^{-3}$ F/m^2, $C_J = 0.35 \times 10^{-3}$ F/m^2, $C_{\rm GSO} = C_{\rm GDO} = 0.3 \times 10^{-9}$ F/m, $C_{\rm GBO} = 0.1 \times 10^{-9}$ F/m, $C_{\rm JSW} = 0.23 \times 10^{-9}$ F/m,

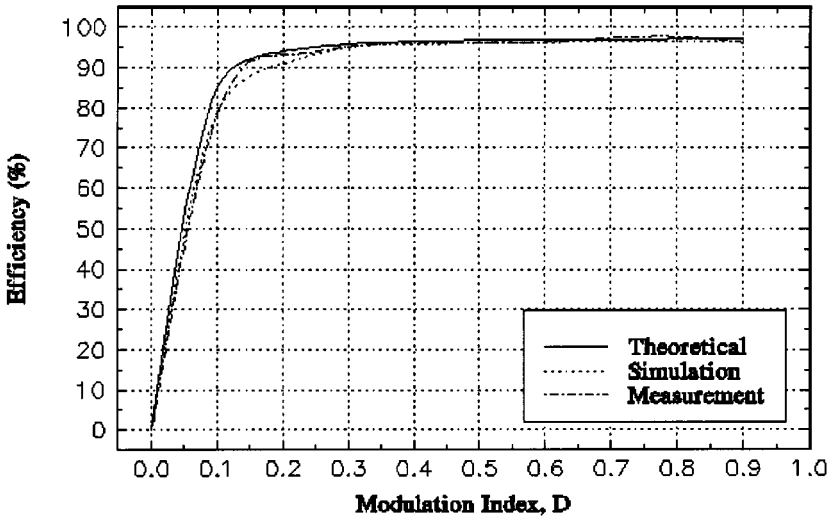

Fig. 5. Theoretical, simulated, and measured power efficiency of a Class D amplifier output stage based on the waffle layout.

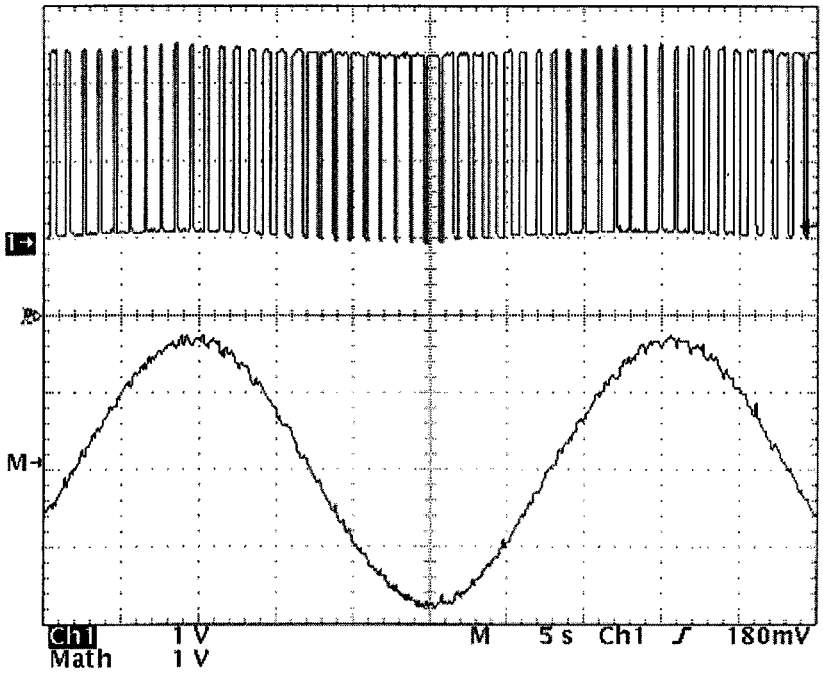

Fig. 6. Measured PWM signal (top) of a Class D output stage and demodulated output signal (bottom) across the load.

$C_{\rm pad} = 2$ pF/pad, $t_{\rm ox} = 2.20 \times 10^{-8}$ m, $R_n = 25\ \Omega/\square$, $R_p = 40\ \Omega/\square$, $R_{\rm ctn}(1.6\ \mu{\rm m} \times 1.6\ \mu{\rm m}) = 12\ \Omega$/contact, and $R_{\rm ctp}(1.6\ \mu{\rm m} \times 1.6\ \mu{\rm m}) = 18\ \Omega$/contact.

Using (1), we design the transistor W optimized to a single modulation index D at different modulation indexes ($D = 0.1, 0.2, \ldots, 1$) for the finger and waffle layouts. We can show that although the power efficiency of the output stage realized by the finger and waffle layouts is nearly equal, the IC area in the waffle layout is on average 12% smaller. On this basis, we recommend the waffle layout for the design of a Class D amplifier output stage optimized to a single modulation index.

Consider now a case where we compare a design optimized to a single modulation index at $D = 0.9$ and the other optimized to a range of modulation indexes $D_1 = 0.025$ to $D_2 = 0.8$. This modulation index range is typical in a hearing instrument design. Using (1) and (4), we compute the optimized W and summarize the salient parameters of this comparative study in Table II. We note here that by employing a waffle layout optimized to a range of modulation indexes, we obtain a greatly improved design over the finger layout optimized to a single modulation index. The improvement is a 42% relative reduction in power dissipation and requires only one sixth of the IC area. This improvement is very significant because the output stage dissipates the largest power in the amplifier and typically occupies 50% of the total Class D amplifier IC area. Based on these results, we recommend that the Class D amplifier output stage be designed using the waffle layout and optimized to a range of modulation indexes.

Fig. 4 depicts a microphotograph of an IC comprising two Class D output stages, a finger and waffle layout. The theoretical, simulated and measured power efficiencies for the waffle layout is shown in Fig. 5. We note that the theoretical, simulated, and measured power efficiencies agree well (although not shown, the theoretical, simulated, and measured power efficiencies for the finger layout also agree well), hence, verifying the theoretical derivations.

Fig. 6 depicts the measured waveforms of the PWM signal (top) at one of the Class D output stages and the demodulated output signal

(bottom) across the load. It can be observed here that the PWM signal is slightly amplitude modulated, whose frequency is the same as the frequency of the demodulated output signal. This amplitude modulation is due to the non-zero on-resistance of the Class D output stage; t he on-resistance has already been accounted for in the optimization methodologies described herein. We have analyzed the effect of this modulation and can show that it has negligible effect on the total harmonic distortion.

V. Conclusion

An analysis of the power dissipation mechanisms which determines the power efficiency of the output stage of a Class D amplifier has been presented. Expressions of these power dissipation mechanisms for the finger and waffle layouts have been derived. Two proposed methodologies to optimize (optimized for a given fabrication process, supply voltage, and load resistance) the aspect ratios of the transistors in the output stage have been presented. For the design of a Class D amplifier output stage, the proposed optimization based on a range of modulation indexes and realized by the waffle structure is recommended.

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An Adaptive Demodulator for the Chaotic Modulation Communication System with RBF Neural Network

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***Abstract*—Chaotic modulation is an important spread spectrum (SS) technique amongst chaotic communications. The logistic chaotic signal acts as the modulation signal in this paper. An adaptive demodulator based on the radial basis function (RBF) neural network is proposed. The demodulator makes use of the good approximate capacity of RBF network for a nonlinear dynamical system. Using the proposed adaptive learning algorithm, the source message can be recovered from the received SS signal. The recovering procedure is on line and adaptive. The simulated examples are included to demonstrate the new method. For the purpose of comparison, the extended-Kalman-filter-based (EKF) demodulator was also performed. The results indicate that the mean square error (MSE) of the recovered source signal by the proposed demodulator is significantly reduced, especially for the SS signal with a higher signal-to-noise ratio (SNR).**

***Index Terms*—Adaptive demodulator, chaos, RBF neural network, spread spectrum.**

I. Introduction

Amongst the different strategies able to guarantee multiple access to a channel, increasing attention has been brought to spread spectrum (SS) and code division multiple access (CDMA) techniques. The main characteristic of SS/CDMA techniques is the spreading of the information signal over a bandwidth much larger than the original [1], [2]. With the recent progress in the theory of nonlinear dynamics and chaos, there has been increasing interest in applying chaos into an SS/CDMA communication system [3]–[6]. Of the different approaches to realize chaotic SS/CDMA communications, chaotic modulation is an important technology which employs a chaotic dynamical system to modulate the transmitted source signal to achieve the purpose of SS/CDMA communication [7]–[9]. More precisely, the transmitted signal is stored in a bifurcation parameter of the chaotic dynamical system. By keeping this bifurcation parameter in the chaotic regime, the modulated broadband signal may be used for the transmitted signal. At a receiver, the source information can be recovered by a special demodulation technology. The main advantage of the chaotic modulation technique is that it does not require any code synchronization. The crucial factor to realize this approach in a noise channel is, however, the evaluation of the bifurcation parameter for the chaotic dynamical system. Several demodulators with a simple inversion procedure for the logistic map transmitter have been proposed in [10] and [11]. These approaches operate very well when the environment is completely noise free. There is no doubt that the effectiveness of the inversion approaches degrade when channel noise exists. A different approach was developed to estimate the parameters of a chaotic dynamical system in the noise case [12]. The method was developed for off-line processing and usually requires a very long data sequence for a reliable noise reduction. All of these methods were designed for a constant parameter chaotic system and do not possess the ability to track a time-varying parameter, as

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