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Analysis and Design of VCO-Based Phase-Domain ΣΔ Modulators

Uğur Sönmez, *Member, IEEE,* Fabio Sebastiano, *Member, IEEE,* and Kofi A. A. Makinwa, *Fellow, IEEE*

Abstract— VCO-based phase-domain ΣΔ modulators employ the combination of a voltage-controlled-oscillator (VCO) and an up/down counter to replace the analog loop filter used in conventional ΣΔ modulators. Thanks to this highly digital architecture, they can be quite compact, and are expected to shrink even further with CMOS scaling. This paper describes the analysis and design of such converters. Trade-offs between design parameters and the impact of non-idealities, such as finite counter length and VCO non-linearity, are assessed through both theoretical analysis and behavioral simulations. The proposed design methodology is applied to the design of a phase-to-digital converter in a 40-nm CMOS process, which is used to digitize the output of a thermal-diffusivity temperature sensor, achieving ±0.2° (3σ) phase inaccuracy from -40 to 125 °C and a sensor-limited resolution of 57 m° (RMS) within a 500-Hz bandwidth. Measurements on the prototype agree quite well with theoretical predictions, thus demonstrating the validity of the proposed design methodology.

Index Terms— VCO-based Sigma-Delta modulator, Time-to-digital converter, Phase-to-digital converter, Quantization noise

I. Introduction

In recent years, time-to-digital converters (TDCs) have found many applications, especially in digital PLLs and instrumentation applications [1][2]. One specific class of TDCs, known as phase-to-digital converters, can be used to digitize the phase of a periodic input signal. Phase-to-digital converters based on the ΣΔ ADC architecture, i.e. phase-domain ΣΔ modulators (PDΣΔMs), have been used in readout circuits for single-photon avalanche diodes (SPADs) [3], wireless receivers [4], resistor-based temperature sensors [5], and thermal-diffusivity-based (TD) temperature sensors [6].

Fig. 1 shows a simplified block diagram of a PDΣΔM. Here, an input signal (V_{IN}) at frequency F_{IN} and with a phase shift Φ_{IN} is multiplied by the clock signal V_{DEM}, which is at the same carrier frequency as V_{IN} ($F_{DEM} = F_{IN}$). This results in a DC component proportional to their phase difference, as well as higher order components. The multiplier's output is applied to a loop filter, which in the case of a 1st-order modulator is an integrator [7]. The loop filter drives an M bit quantizer, which, in turn, drives an M bit phase DAC that adjusts the phase of V_{DEM}. The loop attempts to minimize the DC component at the integrator input in a ΣΔ manner, and as a result, the output bit-stream is a digital representation of the signal phase Φ_{IN}.

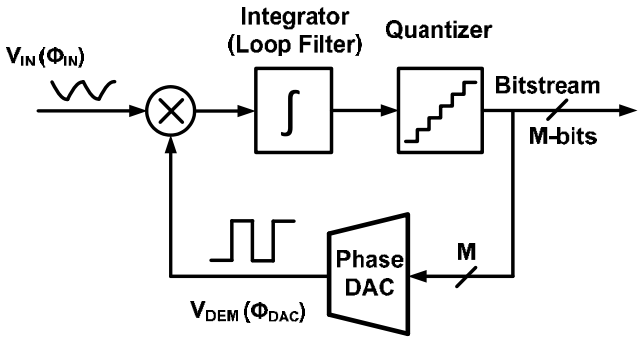

Fig. 1. Block diagram of an analog PDΣΔM.

The architecture of a PDΣΔM is similar to that of an analog PLL, and as such it is capable of rejecting wide-band noise while detecting the phase of an input signal relative to that of a reference. This property has been exploited for the readout of temperature sensors based on the thermal diffusivity (TD) of silicon [6]-[8]. Such TD sensors output a small (millivolt-level) signal, whose phase-shift is a function of temperature, but which is accompanied by relatively large amounts of wide-band noise. Since their accuracy improves with process scaling, smart TD sensors, i.e. TD sensors with a digital output, are well suited for the thermal management of SoCs. In such applications, however, area is at a premium, and so most published designs occupy less than 10,000 μm^2 [10][11]. This in turn puts pressure on the area of the PDΣΔM, which currently dominates the area of smart TD sensors.

This issue has been addressed by the adoption of a highly digital PDΣΔM based on a voltage-controlled oscillator (VCO), first implemented in a mature 0.16-µm CMOS process [8], and later shown to scale in a more advanced 40-nm CMOS process [9]. Inspired by compact VCO-based ADCs [12][13], a VCO translates the input signal into the frequency domain. The phase-shift of this frequency-domain signal is then digitized by an all-digital phase-domain ADC based on an up/down counter,

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which acts as an integrator. Thanks to this highly digital architecture, such VCO-based PDΣΔMs take full advantage of technology scaling, as proven by a x3 smaller area and x2 less supply voltage requirement when ported from 0.16-µm to 40-nm CMOS [8][9]. However, an analysis of this architecture discussing potential drawbacks and design trade-offs, has not yet been reported.

This paper will analyze the unique features of VCO-based PDΣΔMs that differentiate them from VCO-based ADCs and analog-based PDΣΔMs. Section II will describe the operation of a general multi-bit VCO-based PDΣΔM. The quantization error associated with its digital counter is discussed in section III. Section IV discusses the design of the digital counter, based on counter wrap-around constraints. The effect of non-linearity is tackled in section V. A second order modulator with potentially higher SNR is presented in section VI. In section VII, the developed models will be used to go through the design procedure of a prototype first-order PDΣΔM and expected performance will be compared to experimental results. Finally, the conclusions highlights how the proposed design procedure can lead to area-efficient VCO-based PDΣΔMs with performance comparable to analog-based designs.

II. VCO-Based PDΣΔM Architecture

The VCO-based version of this architecture is shown in Fig. 2(a). V_{IN} is converted into variations of the VCO's output frequency. The counter acts like an integrator, while its up-down input (*DEM*) facilitates chopper demodulation, i.e. multiplication by a square wave, since it determines whether the counter's state is either incremented or decremented. The value accumulated by the counter after one cycle of *DEM* will then be proportional to the integrated phase-shift between *DEM* and the VCO's output frequency, thus emulating the function of an integrator.

This highly digital implementation avoids the need for the large capacitors usually employed in analog loop filters and enables an efficient implementation of the *M* bit quantizer, which can be realized by sampling the *M* MSB's of the digital integrator output.

For maximum accuracy, both analog and VCO-based modulators are usually operated as incremental converters, in which the integrator is reset before each conversion [14]. A sinc filter (implemented by a simple counter) can then be used to decimate the converter's output [14].An implementation of the first order VCO-based PDΣΔM is shown in Fig. 2 (b). An *S* bit up/down counter is used to combine demodulation and integration, while an *M* bit register acts as the quantizer. The quantizer sampling clock (F_S) is typically chosen at the same frequency as F_{DEM} [7].

In order to prevent meta-stability problems in the counter, a flip-flop is used to synchronize the up/down signal to the next edge of F_{VCO}. This is similar to the clock re-synchronization [15] required when two clock domains cross each other. This re-synchronization clock is shown as F_{SYNC} in Fig. 2(b).

III. Noise Analysis And Counter Quantization

The VCO-based PDΣΔM has three major noise sources: ΣΔ quantization noise, up/down counter's quantization error and VCO's phase noise. As is well-known, the ΣΔ's quantization noise can be reduced by increasing *M*, its order or sampling rate [18].

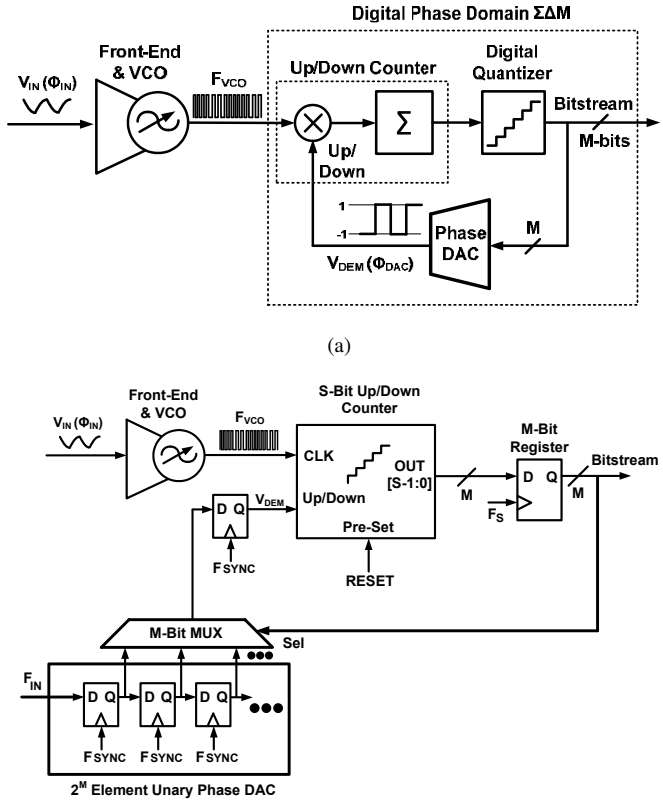

Fig. 2. (a) Block diagram, and (b) circuit-level implementation of the VCO-based PDΣΔM architecture.

The second noise source, due to up/down counter's quantization, is unique to VCO and counter based ΣΔ modulators. Unlike an analog integrator, an up/down counter can only count integer values and hence imposes rounding on its input. In the following, a simple expression for the quantization noise associated with the operation of the up/down counter will be derived.

For this analysis, we will model the counter as an ideal discrete-time integrator that introduces some input-referred quantization error at the end of every up/down cycle. The timing diagram in Fig. 3 shows how this simplification can be made. Here, we are also assuming that the input carrier signal is a sinusoid with frequency F_{IN} and a signal phase shift Φ_{IN} with respect to the reference square-wave up/down signal with $\Phi_{DAC} = 0$.

The frequency of the VCO (F_{VCO}) can be expressed as:

$$F_{VCO}(t) = K_{VCO}V_A \cos(2\pi F_{IN}t + \Phi_{IN}) + F_{NOM} \qquad (1)$$

where K_{VCO} is the VCO gain, V_A is the amplitude of the input carrier and F_{NOM} is the nominal VCO output frequency. After integrating F_{VCO} for each full up period (τ_{UP}) and a full down period (τ_{DOWN}), an ideal counter, i.e. a counter without any quantization error, would compute the residual count *C* given by:

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$$C = \int_0^{\tau_{UP}} F_{VCO}(\mathrm{t})\,\mathrm{dt} - \int_{\tau_{UP}}^{\tau_{UP}+\tau_{DOWN}} F_{VCO}(\mathrm{t})\,\mathrm{dt} \qquad (3)$$

Every period, C is computed and then accumulated with the previous result. For an up/down signal with a duty cycle of 50% ($\tau_{UP} = \tau_{DOWN} = 0.5/F_{IN}$), C becomes:

$$C = \frac{2K_{VCO}V_A}{\pi F_{IN}}\sin(\Phi_{IN}) \qquad (4)$$

It should be noted that while an exact 50% duty cycle can be guaranteed by a fully digital chopper, the mismatch or duty-cycle errors of an analog chopper will result in residual offset [16]. The absence of residual chopper offset is a distinct advantage of this architecture.

Shifting the phase of the up/down signal by Φ_{DAC} (due to the phase DAC action) is equivalent to shifting the input signal by -Φ_{DAC}; thus a more general form of (4) is:

$$C = \frac{2K_{VCO}V_A}{\pi F_{IN}}\sin(\Phi_{IN} - \Phi_{DAC}) \qquad (5)$$

During regular ΣΔ operation, the feedback loop ensures that on average $\sin(\Phi_{IN}-\Phi_{DAC}) = 0$. Since $\sin(\Phi_{IN} - \Phi_{DAC}) \approx \Phi_{IN} - \Phi_{DAC}$ for small phase differences, we can model the relationship between C and phase as a gain factor K (Fig. 4). The phase-to-count gain K can be readily defined from (5) as:

$$K = \frac{2K_{VCO}V_A}{\pi F_{IN}} \qquad (6)$$

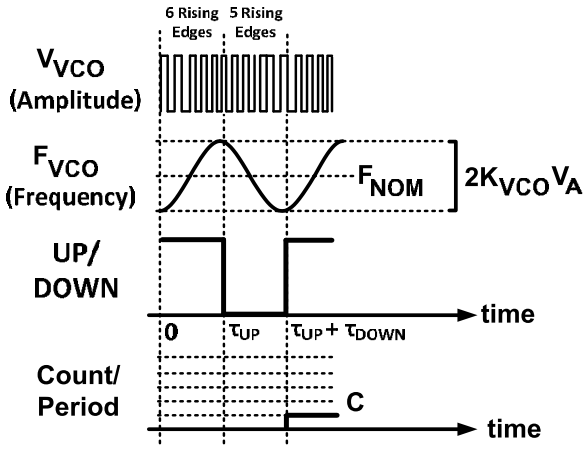

Fig. 3 Timing diagram demonstrating how up/down counting can be modeled as a combination of chopping and discrete-time integration.

However, a digital counter can only accumulate integer values because it only responds to the edges of F_{VCO}, which is equivalent to rounding C to an integer before the accumulation operation. Fig. 5 demonstrates the timing diagram resulting from such synchronization. With this additional synchronization step, the quantization is in essence a "round up" operation, where the counter is able to round up the fractional count at its input before integration. The errors $\Delta Q_U(N)$ and $\Delta Q_D(N)$ denote the fractional count error at the N^{th} cycle in the up and down period, respectively, and as round-up errors, they are bounded by [0 1] (Fig. 5).

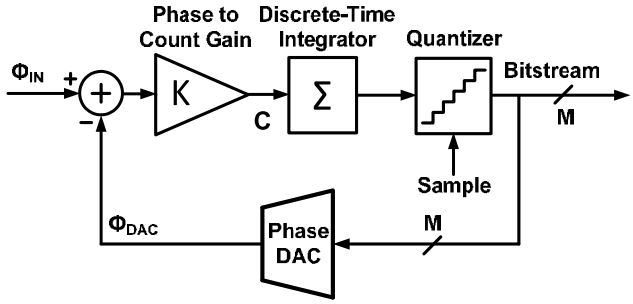

Fig. 4. Block diagram of the ideal discrete-time PDΣΔM with a discrete-time integrator.

$\Delta Q_U(N)$ and $\Delta Q_D(N)$ are deterministic for a given F_{VCO} and up/down signal. As will be shown later, VCO's accumulated jitter at the N[th] cycle will randomize the timing and duration of events $\Delta Q_U(N)$ and $\Delta Q_D(N)$. Thus, the VCO will introduce significant dithering, and the quantization error can be assumed to be uniformly and randomly distributed on the [0 1] interval and uncorrelated in time.

This is analogous to approximating as white noise the quantization error introduced by the comparator of a ΣΔ modulator [17]. Noting that the average quantization error is 0.5, the variance of $\Delta Q_U(N)$ and $\Delta Q_D(N)$ can then be computed as [18]:

$$\sigma_Q^2 = \int_0^1 (q-0.5)^2 dq = \frac{1}{12} \qquad (7)$$

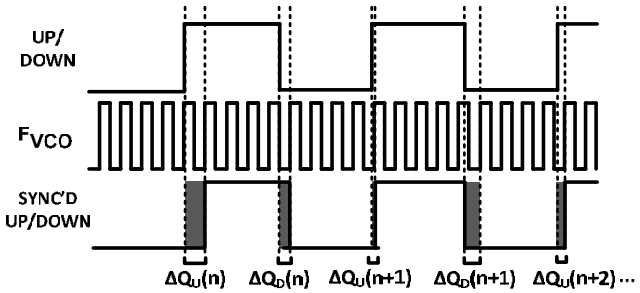

Fig. 5. Timing diagram demonstrating the error introduced by metastability synchronization of up/down signal to F_{VCO}.

As can be seen on Fig. 5, the total error for the N^{th} cycle [$\Delta Q_T(N)$] is given by the error on the up period minus the error on the down period

$$\begin{aligned}\Delta Q_T(N) &= [\Delta Q_U(N) - \Delta Q_D(N)] - [\Delta Q_D(N) - \Delta Q_U(N+1)\\ &= \Delta Q_U(N) - 2\,\Delta Q_D(N) + \Delta Q_U(N+1)\end{aligned} \qquad (8)$$

The total error after N up/down cycles can be written as the sum of the following series:

$$\sum_{k=1}^{N} \Delta Q_T(k) = \Delta Q_U(1) - 2\Delta Q_D(1) + 2\Delta Q_U(2) - 2\Delta Q_D(2) + \cdots + \Delta Q_U(N+1) \qquad (9)$$

Since each element in the series has a variance of σ_Q^2, and is assumed to be uncorrelated from the others, the variance of the total error is equal to the sum of all component variances:

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$$\sigma^2\left(\sum_{k=1}^{N}\Delta Q_T(k)\right) = (8N-2)\,\sigma_Q^2 \qquad (10)$$

while the mean of the total error is zero. When $N \gg 1$, this error converges to $8N\sigma_Q^2$. The bandwidth of this error is $F_{IN}/2$, since it manifests every time an up/down count period is completed. Using (7), we get the total power of the error in fractional counts (σ_{TOTAL}^2) for a bandwidth F_{BW}:

$$\sigma_{TOTAL}^2 = \frac{4}{3}\frac{F_{BW}}{F_{IN}} \qquad (11)$$

If the sampling rate (F_S) of the PDΣΔM is chosen equal to F_{IN}, then the ratio $F_S/2F_{BW}$ is also known as the oversampling ratio (OSR) of the ΣΔ modulator.

Now, we can replace the discrete-time block in Fig. 4 with an integrator and an additive white noise source (ΔQ_{ERR}) with a power of σ_{TOTAL}^2, as shown in Fig. 6.

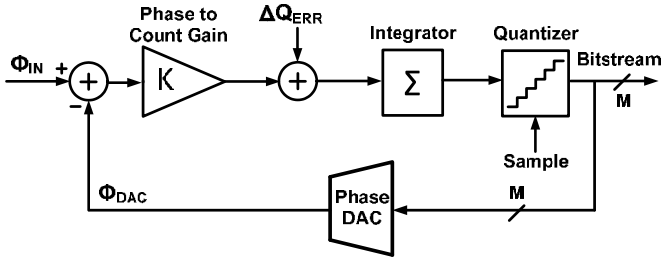

Fig. 6. Block diagram of the PDΣΔM with white additive noise source modelling the counter quantization noise.

The error in fractional counts can be directly converted into phase, which results in an input-referred phase error with an in-band power of σ_P^2, where:

$$\sigma_P^2 = \frac{2}{3\cdot OSR\cdot K^2} \qquad (12)$$

By using (6), the RMS in-band error in radians ($\sigma_{P,r}$) is:

$$\sigma_{P,r}(\text{in}-\text{band}) = \sqrt{\frac{1}{6OSR}}\cdot\frac{\pi\,F_{IN}}{K_{VCO}V_A} \qquad (13)$$

Looking at (13), we can make an important conclusion: the input-referred quantization noise due to the digital counter scales inversely with the product of signal amplitude and VCO gain, i.e. the frequency swing at the VCO output. For a given F_{IN} and V_A, K_{VCO} or OSR must be increased to suppress such quantization noise. Since a larger OSR implies a lower conversion speed, increasing K_{VCO} is more desirable.

This analysis has been also confirmed by system-level simulations, i.e. the simulation of an ideal ΣΔ modulator with additive noise (to breakup strong idle tones) as shown in Fig. 6 (simulated in Matlab), and a mixed-signal simulation in CppSim [19].

In both models, $K_{VCO}V_A$ = 70 MHz, $F_{IN} = F_S$ = 1.17 MHz, F_{NOM} = 600 MHz, S = 8 and M = 3. The phase DAC spans 78.75° with steps of 11.25°. A block diagram of the mixed-signal CppSim model is shown in Fig. 7. A high-frequency clock (F_{SYNC}) is used to generate the 3-bit phase DAC values ranging from 11.25° to 90°. The up/down counter was compiled as a Verilog block, and is hence ideal. Standard D flip-flop, VCO and multiplexer elements were used from CppSim's standard libraries.

Fig. 8 shows the power spectral density (PSD) simulated in the two models together with the quantization noise floor calculated from (13) (dashed blue line). Good agreement is achieved at low frequencies between both models and the theoretical prediction. The quantization noise is predicted to be 38 m° for OSR = 1024, which corresponds to ~1 ms conversion time. The idle tone around 400 kHz for the CppSim model results is attributed to the limited accuracy of the time-domain model (100 ps). The idle tone is not observed in measurement results. Although low-frequency idle tones are a typical issue for 1st-order modulator, they do not appear in the simulation shown in Fig. 8 because of the dithering action of the thermal noise superimposed on the input signal. In typical sensing applications of the phase-domain read-out, such as those shown in section VII, the input signal is characterized by a small amplitude and relatively large noise that is enough to dither the modulator.

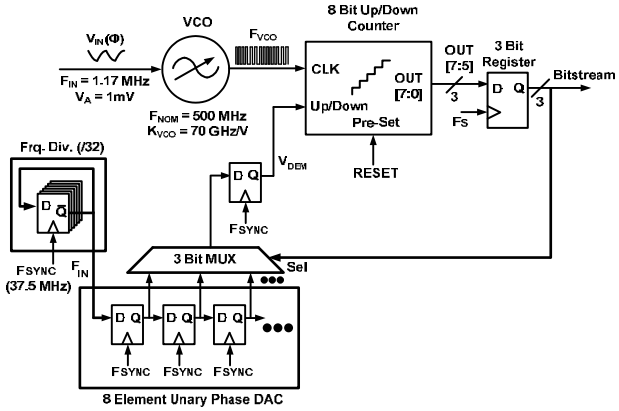

Fig. 7. Block diagram of the implemented CppSim model.

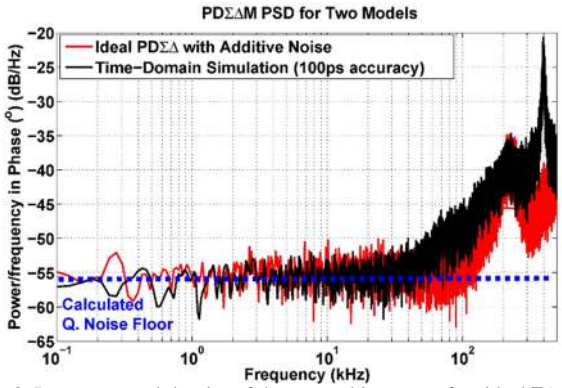

Fig. 8. Power spectral density of the output bitstream of an ideal ΣΔ model with additive noise and of a transient simulation.

The agreement of the two models with (13) means that long time-domain simulations can be avoided when only the in-band behavior of the counter's quantization noise is of interest, since

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a simple noise source at the input of the discrete-time integrator is sufficient to capture its low-frequency noise behavior.

Once the counter quantization noise is calculated, we can determine the VCO's phase noise requirement. For this analysis we assume that thermal noise dominates the VCO phase noise. In order to make the analysis consistent with the model in Fig. (6), we first derive the effect of phase noise in terms of fractional counts and then refer the error back to phase.

First, we assume a fractional frequency power spectral density (PSD) $S_Y(f)$ due to phase noise. For simplicity, we also assume $F_{VCO} = F_{NOM}$.

From (3), we can convert $S_Y(f)$ into fractional count PSD $S_C(f)$. Up/down modulation acts as a chopper, or a mixer, and down-modulates to DC the frequency noise spectrum around F_{IN}, where F_{IN} is the modulation frequency [16]. Without up/down operation, counter output is simply F_{NOM} times the count period of $2\tau_{UP}$, so:

$$S_C(f) = 4\tau_{UP}^2 F_{NOM}^2 S_Y(f + F_{IN}) \tag{14}$$

We can relate $S_Y(f)$ to VCO's phase noise $\mathcal{L}_\Phi(f)$ [26]:

$$S_Y(f) = 2\mathcal{L}_\Phi(f)\,\frac{f^2}{F_{NOM}^2} \tag{15}$$

By combining (14) with (5) and (15), we get the PSD of the input-referred noise as:

$$S_{\Phi IN}(f) = \frac{\pi^2}{2K_{VCO}^2 V_A^2}\,\mathcal{L}_\Phi(f + F_{IN})(f + F_{IN})^2 \tag{16}$$

Note that $S_{\Phi IN}(f)$ is the equivalent noise on the input phase signal and it is different from the VCO phase noise $\mathcal{L}_\Phi(f)$. The variance due to $S_{\Phi IN}(f)$ can be obtained by integrating $S_{\Phi IN}(f)$ over the bandwidth of interest from DC up to F_{BW}. As expected, only the VCO phase noise at an offset F_{IN} from the carrier contributes to the output. Noise at lower frequencies (such as flicker noise) is suppressed because it will be up-modulated around F_{IN} by the up/down modulation and filtered by the decimation filter, which is analogous to the flicker-noise suppression in chopper amplifiers [16]. However, most practical VCOs can still exhibit flicker noise at an offset frequency form the carrier around and above F_{IN}. In that case, the flicker noise corner can be reduced by a wide-band low-noise amplifier that precedes the VCO [8]. If the system allows it, the carrier frequency F_{IN} can also be increased to avoid flicker noise, at the cost of additional quantization noise.

For K_{VCO}=*140* MHz/V and V_A = 0.5 mV, the phase-noise-induced output noise will be below the quantization-noise-induced output noise if the VCO phase noise is below -65 dBc/Hz for offset frequencies above 1.17 MHz, which is easily attainable by low-power VCO's [20].

IV. Counter Size and Wrap-Around

Due to practical limitations, the maximum counter output in a VCO-based PDΣΔM is limited, especially in compact readouts where the area of the counter must be minimized [9]. A possible issue is counter wrap-around, i.e. when the counter overflows. In order to design the size of the counter, we will first investigate wrap-around.

A straightforward solution would be to design the counter with overflow protection. Here, we will first observe what happens when both the input and the DAC phase are fixed, i.e. without any ΣΔ feedback. From (2) and (3), assuming equal up and down periods, the minimum size of a non-wrapping counter ($C_{SIZE,non-wrap}$) is:

$$C_{SIZE,non-wrap} > \int_0^{\tau_{UP}} F_{VCO}(t)\,\mathrm{dt} \tag{17}$$

Note that $C_{SIZE,non-wrap}$ in this case must be at least larger than $F_{NOM}\tau_{UP}$, which is large (~8 bits) for typical values (F_{NOM} > 500 MHz, τ_{UP} > 100 ns). A similar constraint also exists for the down-counting phase.

If the counter is allowed to wrap-around (or overload) between up/down counts, this limitation is relaxed because only the remainder after a sequence of up and down counts must be smaller than the counter size. This can be simply expressed as:

$$C_{SIZE,wrap} > C \tag{18}$$

where C is defined in (5), and does not depend on F_{NOM}. Wrap-around in this case simply means allowing the counter output to overflow, as shown in Fig. 9. Intuitively, (20) means that the ΣΔ still operates correctly if the counter wraps around, as long as the output sampled by the quantizer is correct. This can be observed from Fig. 9, which shows how wrapping does not affect the latched counter result. Since a wrapping counter can be of smaller length and does not need any additional logic for overload detection, it is simpler and hence occupies less silicon area. Thus, we will assume the use of a wrapping counter in the following.

The problem in a wrapping counter occurs when the counter value wraps around at, or just before a sampling moment, as illustrated in Fig. 10. Since the error ruins the integrated history of the signal, it is not shaped by the ΣΔ loop and introduces a significant error. The erroneous bits generated during the recovery process will corrupt the output and influence both the decimated output (i.e. the accuracy) and the resolution. The wrap-around can be avoided by limiting the counter's output swing, which is analogous to limiting the output swing of integrators in a regular ΣΔ modulator to avoid amplifier saturation [21].

For a single-bit PDΣΔM, wrap-around can be avoided if the peak-to-peak swing of the latched counter value is less than half the counter length. In that case, the ΣΔ output bit-stream is the sampled counter MSB, and we have:

$$C_{SIZE,wrap} = 2^S > 2(C_{MAX} - C_{MIN}) = 2C_{PP}\,; \quad S > \log_2(2C_{PP}) \tag{19}$$

Where C_{PP} is the peak-to-peak swing of the counter and S is the number of bits of the counter. Since C_{PP} is dependent on the input signal amplitude (V_{IN}) and VCO gain (K_{VCO}), an interesting trade-off exists between counter size and quantization noise. For low quantization noise, V_{IN} and K_{VCO} need to be high [from (13)], which means a larger counter is necessary to avoid wrap-around.

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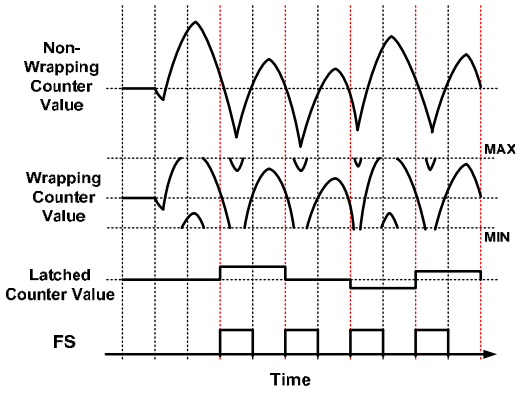

Fig. 9. Timing diagram showing how a wrapping counter can tolerate a smaller swing and counter size.

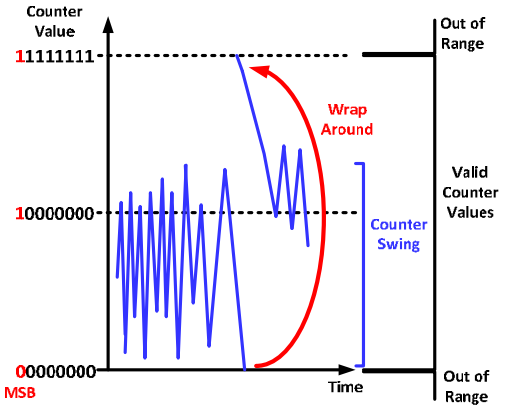

Fig. 10. Latched counter values of a single-bit PDΣΔM with an 8-bit counter over time. If the counter wraps around, the output is corrupted for several successive samples.

C_{PP} is bounded for a first-order modulator and is approximately constant over a bounded range of DC inputs [18]. A similar analysis can be made for an M-bit PDΣΔM, as shown in Fig. 11. Counter wrap-around can be prevented if the peak-to-peak swing of the counter is guaranteed to be less than 2^{S-M}. Therefore, for a general multi-bit case, we have:

$$C_{SIZE,wrap} = 2^{S-M} > C_{PP}, \text{when } M > 1; \qquad S > log_2(C_{PP}) + M \tag{20}$$

As a convenient reliability measure, the input phase range can be restricted to be between the second highest and second lowest phase DAC steps, which relaxes (22) to $S > log_2(C_{PP}) + M - 1$. An example of a PDΣΔM used in a temperature sensor will demonstrate a typical C_{PP} value in section VII.

Another case where the counter can wrap-around is at the start of the conversion. This first count value can be very large and can cause a wrap-around. We will assume that the counter is reset to its median value (2^{S-1}) and that the input phase is bounded within [0 Δ], where 0 and Δ are the minimum and maximum value of the phase DAC (Φ_{DAC}), respectively. In this case, maximum value of $|\Phi_{IN} - \Phi_{DAC}| \leq \Delta/2$, and from (5), we find the maximum count (C_{MAX}) to be:

$$C_{MAX} = \pm \frac{2K_{VCO}V_A}{\pi F_{IN}} \sin(\Delta/2) \tag{21}$$

To avoid wrap around, the following condition must hold:

$$S > log_2\left(\frac{2K_{VCO}V_A}{\pi F_{IN}} \sin(\Delta/2)\right) + 1 \tag{22}$$

Note that (21) and (22) hold for a multi-bit PDΣΔM where $|\Phi_{IN} - \Phi_{DAC}| \leq \Delta/2$. For a single-bit modulator, $\Phi_{IN} - \Phi_{DAC}$ can assume values up to ±Δ, and hence (21) and (22) must be modified by changing Δ/2 with Δ.

The constraint imposed by (22) is different from (19) or (20), since it is not dependent on signal statistics. It is instead dependent on Δ, i.e. the span of the phase DAC. Resetting the counter to 2^{S-1} instead of another arbitrary value also helps minimizing the counter size.

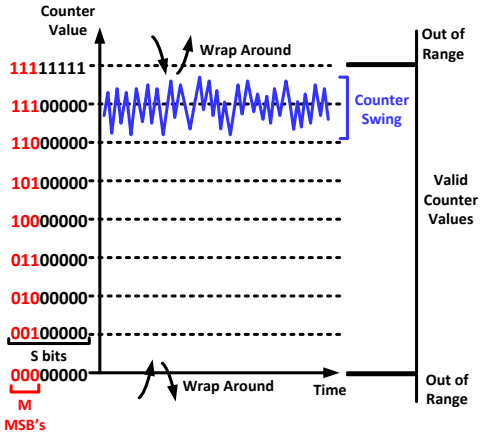

Fig. 11. Counter output of a 3-bit PDΣΔM with an 8-bit counter over time.

V. Non-Linearity

Because of the sine term in (5), the PDΣΔM exhibits a systematic non-linearity. This non-linearity can either be corrected during digital post-processing [6], or by using small range(s) for Φ_{DAC} [22], thus linearizing the sine term.

The non-linear relation between the average of the output bitstream (μ) and the input and DAC phase is described by the following equation for a single-bit PDΣΔM:

$$\mu = \frac{\sin(\Phi_{IN} - \Phi_{DAC,1})}{\sin(\Phi_{IN} - \Phi_{DAC,1}) - \sin(\Phi_{IN} - \Phi_{DAC,0})} \tag{23}$$

where $\Phi_{DAC,1}$ and $\Phi_{DAC,0}$ are the DAC phases for a feedback values of 0 and 1. For multi-bit operation, $\Phi_{DAC,1}$ and $\Phi_{DAC,0}$ can be replaced with the exercised phase levels of the DAC. Note that although μ itself is a non-linear function of Φ_{IN}, it is independent of any circuit parameters, i.e. its non-linearity is systematic. However, additional non-linearities can shift this systematic curve, and add inaccuracy to the design.

From literature, VCOs are known to be highly non-linear with respect to the amplitude of their frequency-controlling input signal. For this reason, many techniques to improve VCO non-linearity have been adopted in VCO-based ADCs [23-25]. However, since the information in a PDΣΔM is encoded in the

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phase of the input signal, VCO non-linearity will have a smaller effect in the proposed read-out, as demonstrated in the following.

For a sinusoidal input as in (1), the VCO's amplitude non-linearity will produce tones at harmonics of F_{IN}. Considering only second and third harmonic of F_{IN}, the VCO output frequency can be expressed as:

$$F_{VCO}(t) = A_1\cos(2\pi F_{IN}t + \Phi_{IN}) + A_2\cos(4\pi F_{IN}t + 2\Phi_{IN}) + A_3\cos(6\pi F_{IN}t + 3\Phi_{IN}) + F_{NOM} \quad (24)$$

where A_N is the amplitude of the N-th harmonic component. Combining (5) and (24), we get the total count after up/down periods as:

$$C = -\frac{2}{\pi F_{IN}}\left[A_1\sin(\Phi_{IN} - \Phi_{DAC}) + \frac{A_3}{3}\sin(3\Phi_{IN} - 3\Phi_{DAC})\right] \quad (25)$$

Due to the up/down operation, the second harmonic cancels out and third harmonic only adds a gain error as long as $3\Phi_{IN} - 3\Phi_{DAC}$ is small, since $\sin(3\Phi_{IN} - 3\Phi_{DAC})/3 \approx \Phi_{IN} - \Phi_{DAC}$. This means that the linearity can be improved if $\Phi_{IN} - \Phi_{DAC}$ is made smaller, as will be demonstrated by simulation in the following. However, in the general case, (27) is modified to:

$$\mu = \frac{A_1\sin(\Delta\Phi_1) + \frac{A_3}{3}\sin(3\Delta\Phi_1)}{A_1(\sin(\Delta\Phi_1) - \sin(\Delta\Phi_0)) + \frac{A_3}{3}(\sin(3\Delta\Phi_1) - \sin(3\Delta\Phi_0))} \quad (26)$$

where $\Delta\Phi_1$ is $\Phi_{IN} - \Phi_{DAC,1}$ and $\Delta\Phi_0$ is $\Phi_{IN} - \Phi_{DAC,0}$. In this case, the systematic non-linearity is a function of the ratio A_3/A_1, which strongly depends on the VCO circuit parameters. If A_3/A_1 is fixed, the error can be eliminated by batch trimming but any spread will add inaccuracy.

From (26), we can make an important conclusion: First order errors in absolute values of A_1 or A_3 do not influence μ. This is important in sensor applications, where changes in A_1 (via K_{VCO}) over temperature and other environmental effects are rejected by the system.

Any non-linearity in the VCO adds harmonic components of the input signal but does not cause any non-linear distortion in the phase of the fundamental tone. Since an ideal phase read-out is sensitive only to the phase of the fundamental, it is not affected by the VCO's amplitude distortion. Therefore, as the PDΣΔM behaves more closely to an ideal phase detector, for example using a smaller DAC phase range, it rejects VCO non-linearity better.As an example, we analyze the case where A_1/A_3 = 40 dB for a single-bit modulator spanning a 90°-range ($\Phi_{DAC,0}$ = 0°, $\Phi_{DAC,0}$ = 90°). A_1/A_3 = 40 dB was chosen as a realistic third-order non-linearity of a typical VCO [12]. The non-linear error of such a PDΣΔM over the full range is shown in Fig. 14 (a) as the red curve. The blue curve shows the case where A_3 = 0, and the black curve shows the difference between the two cases. The VCO non-linearity causes a ±0.5° error.

When the phase range, i.e. the maximum $\Phi_{IN} - \Phi_{DAC}$, is changed to 11.25°, as shown in Fig. 14 (b), the error then reduces to less than 2 m°. A reduction in the phase range can be easily achieved in multi-bit PDΣΔMs or two-step PDΣΔMs [7], thus making such architectures robust to the non-linearity of typical VCO's, which show third-harmonic distortion ranging from -40 to -60 dB.It must be again highlighted that the high tolerance to distortion of the proposed read-out is an inherent property of phase-domain read-outs. Even a large distortion in the amplitude domain at the system input does not significantly affect the phase of the signal, which is the parameter carrying the information to be detected and converted.

However, the VCO's phase distortion or its signal-dependent delay will impact non-linearity. This necessitates the use of fast response VCO's or constant-bandwidth gain stages to drive the VCO, in order to control its delay. As an example, for a temperature sensor application [8], the gm-stage that drives the VCO needs to be biased with a PTAT current to improve linearity.

Current-starved inverters or simply current-controlled oscillators (CCO) are a good candidate for implementation of VCOs in PDΣΔMs [8] because a CCO can respond very quickly to changes in its biasing current. If this CCO is driven by a gm-stage [8], that gm-stage dominates the VCO's delay. A gm-stage can be designed to have a relatively signal-independent bandwidth and thus the VCO's delay is only a weak function of the input signal.

VI. Second-Order Modulator

It is well known that first order ΣΔ modulators are affected by idle tones if the input signal does not have enough white noise content [18][21]. In sensor applications working with small signals, the 1st-order system in Fig. 2(a) is sufficiently dithered for achieving proper quantization noise behavior. For higher resolution systems, input noise may not provide sufficient dithering and higher-order PDΣΔM may be required.

Fig. 15 shows the block diagram of a second-order fully-digital PDΣΔM, where the quantizer in Fig. 2 (a) has been replaced by a digital ΣΔ modulator. A linear-feedback shift register (LFSR) can be used to add dither to the quantizer.

Secondary feedback is applied via the digital gain term G. The digital ΣΔM itself can be operated at the relatively low sampling rate of the quantizer (F_S). This results in a minimal power penalty when increasing the modulation order.

The system in Fig. 15 has been simulated in CppSim environment to observe the system's performance for a large input carrier amplitude V_A. Thus, the following values were chosen: V_A = 200 mV, K_{VCO} = 5 MHz/mV, F_{IN} = F_S = 1.17 MHz, F_{NOM} = 1.5 GHz, S = 12, G = 512 and M = 3. The phase DAC spans 78.75° with steps of 11.25°. The second counter was sized as 16-bits, and is clocked at a rate of F_S.

Fig. 16 shows the simulated power spectral density (PSD) of the second-order PDΣΔM with the chosen variables. When compared to the first-order modulator in Fig. 8, this modulator is able to accommodate a much larger input voltage swing and thus has 23 dB better SNR due to 14x increase in $K_{VCO}V_A$.This improvement in SNR comes at a cost of larger area, higher VCO frequency, and requirement for higher V_A and better VCO phase noise and linearity specs. In modern digital processes, the impact of additional area and higher VCO frequency can be negligible for applications requiring high-resolution from the PDΣΔM.

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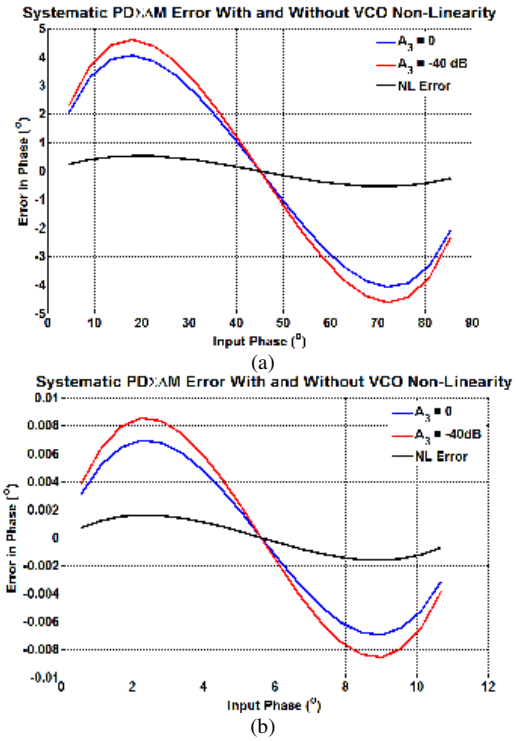

Fig. 14. Non-linearity error of a PDΣΔM with and without the third order non-linearity from the VCO; with a phase DAC range of (a) 90° and (b) 11.25°

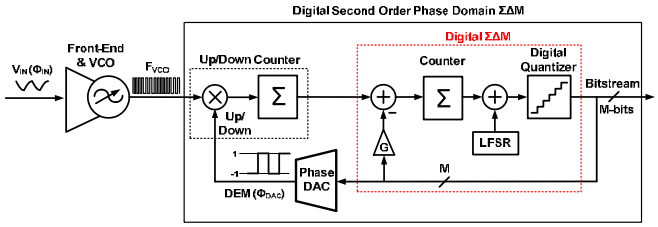

Fig. 15. Block diagram of a second-order VCO-based PDΣΔM

As the amplitude of the input signal increases, VCO linearity becomes a critical practical problem. Larger input amplitude implies that both quantization and VCO phase noise contributes less, but the VCO will exhibit more distortion. This can be tackled using the techniques discussed in Section V.

VII. An Example Design: PDΣΔM for TD Temperature Sensor

In order to confirm the theoretical analysis presented in this work, we will consider the design and analysis of the multi-bit PDΣΔM used to read out a thermal-diffusivity-based temperature sensor in a 40-nm CMOS process [9]. Specifications of the PDΣΔM can be directly derived from the specifications of the temperature sensor. The input signal from the sensor is a filtered square-wave at F_{IN}=1.17 MHz with roughly 1.3 mVpp amplitude, and a phase resolution of 47 m° (~0.8 mrad in radians) in a bandwidth of 500 Hz. This resolution includes the thermal noise generated by the sensor and also by the front-end amplifier. By choosing $F_S = F_{IN} = 1.17$ MHz, an $OSR > 1024$ is obtained for a 500-Hz bandwidth. The output phase from the sensor ranges from 11.25° to 90°, thus $\Delta = 78.75°$.

In order not to degrade the sensor's resolution, we need to derive the K_{VCO} value that sufficiently suppresses the counter's quantization noise. We choose $\sigma_{P,r}$ = 23 m° [0.4 mrad in (13)], i.e. equal to half of the signal noise, which results in a 12% SNR degradation. From (13), K_{VCO} is then found to be 180 MHz/mV. In practice, since K_{VCO} can change dramatically due to process spread and temperature, we chose K_{VCO} = 200 MHz/mV in the nominal case with worst-case of K_{VCO}=160 MHz/mV. Since we want to observe the worst cases for both resolution and wrap-around, we assume K_{VCO} = 160 MHz/mV for quantization-noise calculation and 200 MHz/mV for wrap-around estimation.

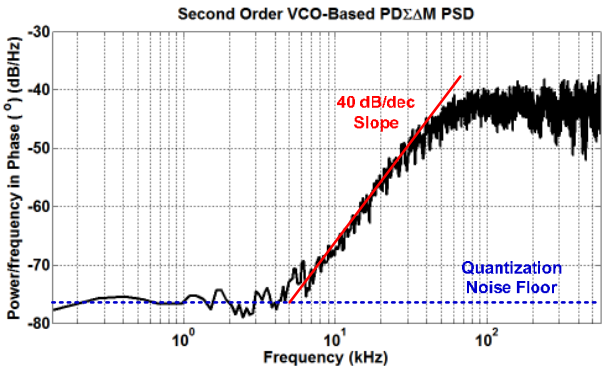

Fig. 16. Simulated PSD of the 2nd Order PDΣΔM's output bitstream, generated via a transient simulation.

Experimental results also confirm this analysis. Fig. 17 shows the power spectral density (PSD) of the prototype sensor [9] as well as calculated counter quantization, thermal and combined noise densities. The sensors exhibit an RMS resolution of 1 mrad (0.36 °C for the temperature reading) within 500 Hz, which agrees well with a total computed RMS resolution of 0.95 mrad [0.8 mrad due to sensor noise; 0.45 mrad due to counter quantization noise according to (13)].

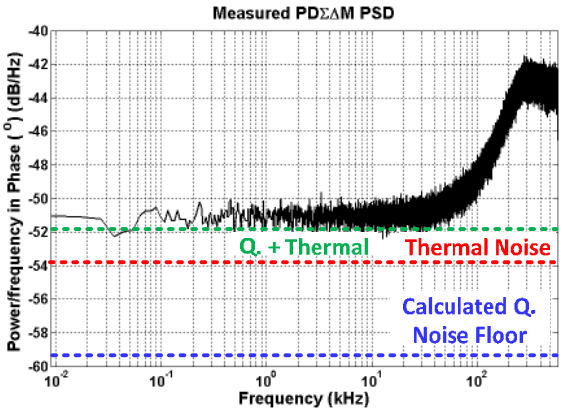

Fig. 17. Measured PSD of the prototype PDΣΔM (8 million samples, averaged 8192 times); with expected noise densities.

The next step is determining the counter size (S) from (20) and (22). The modulator is designed to span Δ = 78.75°, with a phase DAC range from 11.25° to 90°, resulting in $S > 6.12$ from (24). For (20), we need to fix M, or the number of ΣΔ modulator bits. M = 3 was chosen as a good trade-off between phase DAC area and quantization noise suppression. The mixed-signal model in Fig. 7 for K_{VCO} = 200 MHz/mV and Φ_{IN} = 47° was used to obtain a histogram of the counter output swing in Fig.

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18 (a). In this model, thermal noise floor shown in Fig. 17 was added to the input. The peak-to-peak swing is 18 count values for 8192 samples. According to (20), $2^{S-M} > 18$ to avoid wrap-around, which implies $S \geq 8$. This satisfies the requirement from (22) as well.

The simulated counter swing was compared to the measurement results in order to validate the simulation model. For this, the measured 3-bit MSBs of the counter (bit-stream) was compared to the 3-bit representation of the counter swing, shown on a histogram plot in Fig. 18 (b). For the measurement, 8192 samples were obtained also at $\Phi_{IN} = 47°$. The measured and simulated histograms align, and the small difference between them is within the thermal noise budget.

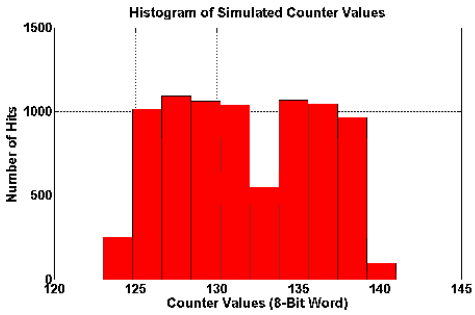

Fig. 18. (a) Histogram of simulated counter values for 8192 samples, showing the counter swing (b) Comparative 3-bit histogram of measured and simulated counter values

VIII. Conclusions

This paper presents the first theoretical analysis of the operation of a VCO-based PDΣΔM. The derived theoretical model is shown to be in good agreement with both simulation and experimental results.

Quantization noise, counter wrap-around and settling time can add additional errors and design constraints in VCO-based PDΣΔMs with respect to fully analog PDΣΔMs. However, with enough VCO gain and a sufficient number of counter bits, the performance gap between analog and VCO-based modulators can be abridged. In addition, it has also been shown that the high non-linearity of practical VCO's can be tolerated by PDΣΔMs. This allows the implementation of compact, scalable, mostly digital and accurate PDΣΔMs, thus making them ideal for implementation in nanometer CMOS technologies.

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