Analysis and Evaluation of Interleaving Techniques in Forward Converters

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***Abstract*— Analysis, design, and evaluation of different interleaving techniques for the forward converter are presented. Specifically, the performance of the one-choke interleaving approach is compared with the two-choke interleaving approach. The results of the analysis are verified experimentally on two 5-V/20-A interleaved dc/dc converters. The analysis, design, and evaluation results can be extended to any number of interleaved converters.**

***Index Terms*—Forward converter, interleaving.**

I. Introduction

PARALLELING of converter power stages is a well-known technique that is often used in high-power applications to achieve the desired output power with smaller size power transformers and inductors [1], [2]. In addition to physically distributing the magnetics and their power losses and thermal stresses, paralleling also distributes power losses and thermal stresses of the semiconductors due to a smaller power processed through the individual paralleled power stages. As a result, paralleling is a popular approach to eliminating "hot spots" in power supplies. Besides, the switching frequencies of paralleled lower power power stages may be higher than the switching frequency of the corresponding single high-power processing stage because lower power faster semiconductor switches can be used in implementing the individual power stages. Consequently, paralleling also offers an opportunity to reduce the size of the magnetic components.

The interleaving technique can be viewed as a variation of the paralleling technique, where the switching instants are phase shifted over a switching period [3]. By introducing an equal phase shift between the paralleled power stages, the output-filter-capacitor ripple is lowered due to the ripple cancellation effect [3]. As a result, the size of the output-filter capacitance can be minimized. Generally, the interleaving in topologies with inductive output filters can be implemented in two ways. One interleaving approach is to directly parallel the outputs of the individual power stages so that they share a common output-filter capacitor (the two-choke approach) [4]. The other approach is to parallel the power stages at the input of a common LC output filter (the one-choke approach). The former approach distributes the transformer and output-filter magnetics, while the latter approach distributes only the transformer magnetics [4], [5]. Due to its distributed magnetics structure and minimum-size output filter, the interleaving approach is especially attractive in high-power applications that call for high-power density and low-profile packaging, for example, distributed power modules (both front-end and load converters).

In this paper, the analysis, design, and evaluation of one- and two-choke approaches of two interleaved forward converters are presented. While the operation of the interleaved forward converter with two chokes is well understood [5]–[7], since it is identical to the operation of the single converter, the operation of the interleaved forward converter with one choke has never been presented, although it was used in practical applications [4]. The results of the analysis are verified on two experimental 5-V/20-A interleaved forward converters. The analysis, design, and evaluation results can be extended to any number of interleaved forward converters.

II. Analysis of Operation of Interleaved Forward Converters

A. Two-Choke Approach

Two interleaved forward converters that utilize two complete forward converter modules (the two-choke approach) are shown in Fig. 1, while the key waveforms are given in Fig. 2. In the implementation in Fig. 1, the reset of the transformers is accomplished by the resonance between the magnetizing inductance of the transformers and the output capacitance of the MOSFET's (including external capacitance) [6], or by a resistor-capacitor-diode (RCD) clamp reset circuit [7], shown in dotted lines in Fig. 1. Since the two modules operate in antiphase with duty cycles less than 50%, the current sharing among the modules is ensured by employing the current-mode control. The operation principle of the interleaved converters in Fig. 1 is identical to that of the single-resonant reset or RCD clamp reset forward converter. As can be seen from Fig. 3, the interleaving reduces the ripple current through the common output-filter capacitor.

B. One-Choke Approach

The one-choke approach, shown in Fig. 3, uses only one output inductor for the purpose of saving a magnetic compo-

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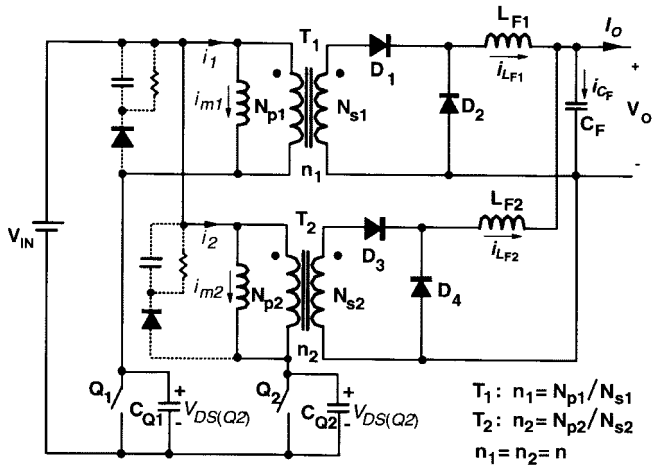


Fig. 1. Two-choke interleaved forward converter.

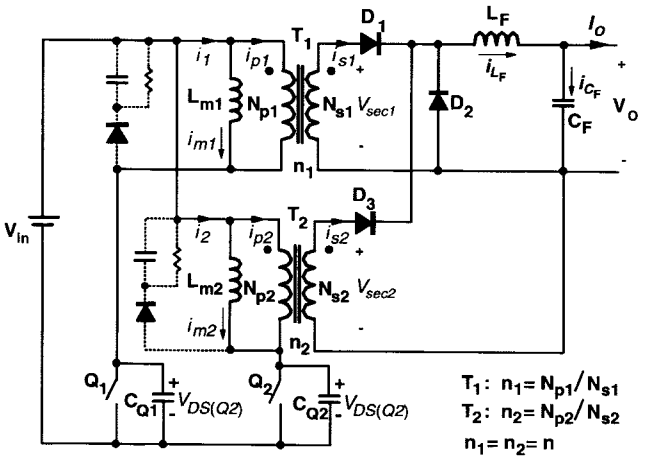


Fig. 3. One-choke interleaved forward converter.

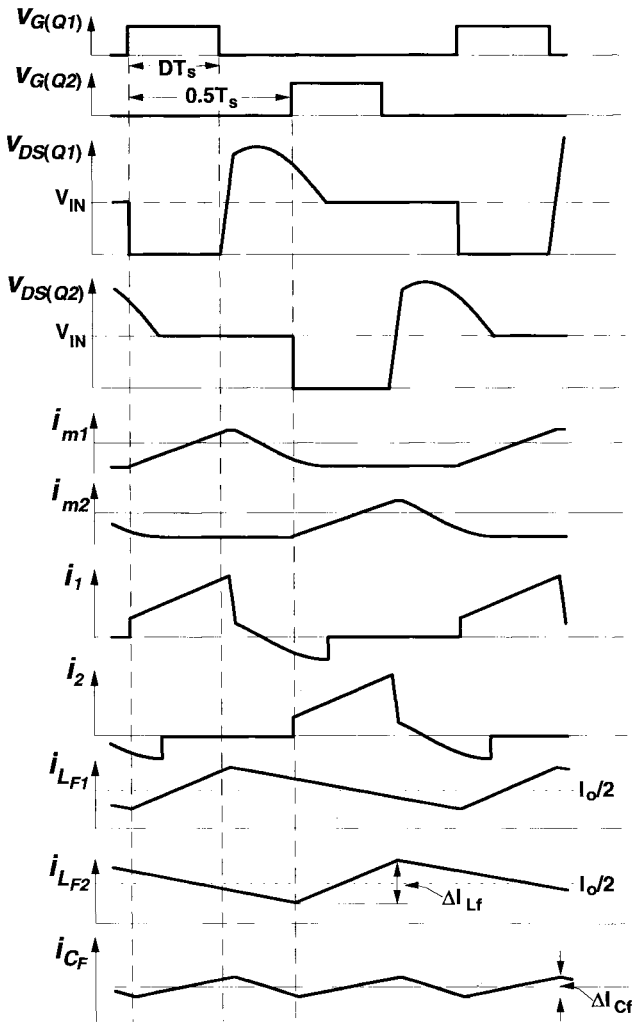


Fig. 2. Key waveforms of two-choke interleaved forward converter.

nent. Because in the one-choke interleaved forward converter the two modules share the same freewheeling diode and output filter, these two modules do not work independently. In fact, the operation of two interleaved forward converters with one choke is quite different from that of the two-choke interleaved converters. To facilitate the analysis of operation of the circuit in Fig. 3, the key waveforms of the one-choke interleaved forward converters with resonant reset are shown in Fig. 4.

To simplify the analysis, it is assumed that all semiconductor devices are ideal, i.e., they represent short circuits in their on states and open circuits in their off states. In addition, the transformers are modeled as ideal transformers with added magnetizing and leakage inductances. Finally, capacitors C_{Q1} and C_{Q2} shown in parallel with switches Q_1 and Q_2 represent the total capacitance connected between the drain-to-source terminals of the switches. Generally, C_{Q1} and C_{Q2} consist of a sum of the switch output capacitance ($C_{\rm oss}$) and the externally added capacitance, if any.

In steady state, during a switching cycle, the circuit in Fig. 3 goes through five topological stages shown in Fig. 5(a)–(e). Immediately before switch Q_1 is turned on at $t = t_0$, filter inductor current i_{Lf} flows through freewheeling diode D_2. At the same time, diode D_3 is reverse biased because the core of transformer T_2 is being reset and, consequently, $V_{\rm sec2}$ is negative.

1) Topological Stage A [t_0-t_1]: When switch Q_1 turns on at $t = t_0$, filter inductor current i_{Lf} commutates from freewheeling diode D_2 to forward diode D_1, as shown in Fig. 5(a). The commutation of i_{Lf} from D_2 to D_1 does not affect the conduction state of forward diode D_3, i.e., D_3 stays off. However, when D_1 starts conducting at $t = t_0$, the potential of the cathode of D_3 increases from 0 V (which is set by conducting D_2 prior to $t = t_0$) to $V_{\rm sec1} = V_{\rm IN}/n$. As a result, to turn D_3 on, it is necessary that the potential of the D_3 anode reaches $V_{\rm sec2} \geq V_{\rm IN}/n$.

Due to antiphase operation, prior to switch Q_1 turn on at $t = t_0$, transformer T_2 is in its reset phase, i.e., a negative voltage is applied to the primary of the transformer because $V_{\rm DS(Q2)} > V_{\rm IN}$. The reset of the core of transformer T_2 continues after switch Q_1 is turned on, and $V_{\rm DS(Q2)}$ continues to decrease in a resonant fashion (determined by L_{m2} and C_{Q2} resonance) toward $V_{\rm IN}$. In a single resonant-reset forward converter, or in interleaved forward converters with multiple chokes as in Fig. 3, the drain-to-source voltage of the switch $V_{\rm DS(Q)}$ cannot fall below the level of input voltage

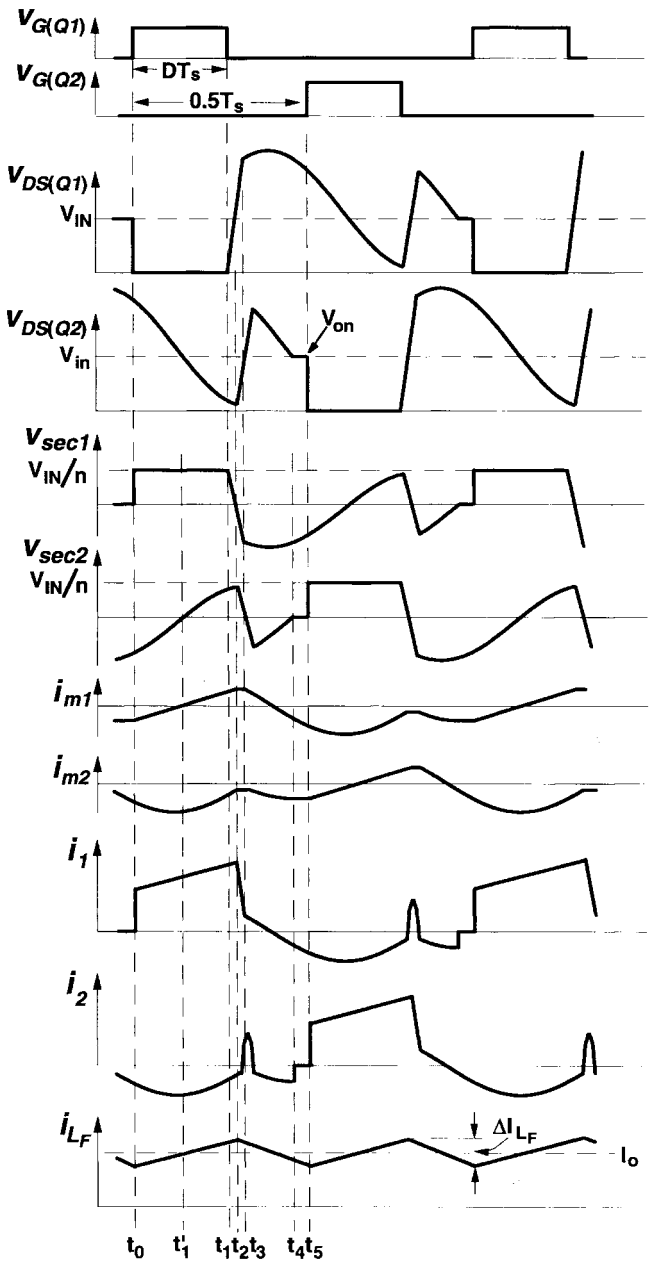


Fig. 4. Key waveforms of one-choke interleaved forward converter.

V_{IN} because of the clamping action of the forward diode [7]. Namely, when $V_{DS(Q)}$ reaches V_{IN}, the forward diode becomes forward biased and starts conducting the secondary-side-reflected magnetizing current. Due to the simultaneous conduction of the forward diode and freewheeling diode (which carries the load current), the secondary winding is shorted and $V_{DS(Q)}$ is clamped to V_{IN}. However, in the circuit in Fig. 5(a), switch voltage $V_{DS(Q2)}$ during the transformer reset period can decrease below V_{IN} because the potential of the cathode of D_3 is raised to $V_{sec1} = V_{IN}/n$ by the conduction of D_1 so that D_3 is reverse biased even when $V_{DS(Q2)} < V_{IN}$. As can be seen from Fig. 5, after reaching V_{IN} at $t = t_1'$ in Fig. 4, switch voltage $V_{DS(Q2)}$ continues to decrease below V_{IN} until topological state A ends at $t = t_1$ when switch Q_1 is turned off.

2) Topological Stage B [t_1-t_2]*:* After switch Q_1 is turned off at $t = t_1$, voltage $V_{DS(Q1)}$ starts resonating because capacitor C_{Q1} is charged by the sum of the magnetizing current and the reflected output-filter inductor current, i.e., $i_1 = i_{m1} + i_{Lf}/n$, as shown in Fig. 5(b). At the same time, $V_{DS(Q2)}$ continues to decrease below V_{IN} because transformer T_2 is still in the reset phase. This topological stage ends at $t = t_2$ when $V_{DS(Q1)}$ ramps up to V_{IN}.

3) Topological Stage C [t_2-t_3]*:* When $V_{DS(Q1)}$ reaches V_{IN} at $t = t_2$, freewheeling diode D_2 becomes forward biased, and it starts conducting a part of the output-filter-inductor current i_{Lf}. Since during this interval both diodes D_1 and D_2 conduct simultaneously, as shown in Fig. 5(c), the secondary of transformer T_1 is shorted. As a result, leakage inductance L_{lk1} and capacitance C_{Q1} start resonating, which increases voltage $V_{DS(Q1)}$ above V_{IN}, as shown in Fig. 4. At the same time, the conduction of D_2 makes D_3 forward biased because it lowers the potential of the cathode of D_3 to 0 V, while secondary voltage $V_{sec2} = [V_{IN} - V_{DS(Q2)}]/n$ is positive because at $t = t_2$, $V_{DS(Q2)} < V_{IN}$. Due to the conduction of D_3, the secondary of transformer T_2 is also shorted, and voltage $V_{DS(Q2)}$ increases at a fast rate because of the resonance between L_{lk2} and C_{Q2}, as shown in Fig. 4. This topological stage terminates at $t = t_3$ when the leakage-inductance current of T_1 becomes equal to the magnetizing current, i.e., $i_{lk1} = i_1 = i_{m1}$, causing diode D_1 to turn off.

4) Topological Stage D [t_3-t_4]*:* During this stage, both forward diodes D_1 and D_3 are off, and i_{Lf} is carried by freewheeling diode D_2, as shown in Fig. 5(d). As a result, transformer T_1 starts to reset through the L_{m1}-C_{Q1} resonance, while the L_{m2}-C_{Q2} resonance discharges C_{Q2}, forcing $V_{DS(Q2)}$ to decrease toward V_{IN}. This topological stage ends naturally at $t = t_4$ when $V_{DS(Q2)}$ decreases to V_{IN}. However, it should be noted that this stage may also end before $V_{DS(Q2)}$ reaches V_{IN} by the turn on of switch Q_2, as illustrated in Fig. 7(a). In this case, a half-cycle operation is completed without the existence of topological stage E.

5) Topological Stage E [t_4-t_5]*:* When $V_{DS(Q2)}$ becomes equal to V_{IN} at $t = t_4$, diode D_3 becomes forward biased and magnetizing current $n \cdot i_{m2}$ starts flowing through D_3, as shown in Fig. 5(e). Due to the shorted secondary of T_2, i_{m2} stays constant during the entire duration of topological stage E. Also, during this stage, the core of transformer T_1 continues to reset. Topological stage E terminates at $t = t_5$ when Q_2 is turned on, and the other half of the switching cycle is initiated. During this half cycle, the operation is identical to the above-described operation, except that the roles of switches Q_1 and Q_2 are exchanged.

The above analysis of the operation of the single-choke interleaved forward converter with the resonant resets can be directly extended to the single-choke interleaved forward converters with the RCD clamp reset. In fact, the only difference between the two reset schemes is seen during the initial phase of the transformer core reset after the primary switch is turned off. Specifically, with the RCD clamp reset, primary switch voltage waveforms $V_{DS(Q)}$, immediately after the switch is turned off (e.g., $t = t_4$ in Fig. 4), have a flat top (because of the clamping action of the RCD clamp circuit) instead of a

resonating waveform, as shown in Fig. 4. The clamping action lasts until the magnetizing current of the transformer falls to zero. After that instant, the RCD clamp reset circuit completes the core reset in the same fashion as the resonant-reset circuit.

Finally, it should be noted that the operation of the single-choke interleaved converter with the active clamp reset is identical to the operation of a single converter because for the active clamp reset forward converter the reset voltage is present during the entire off period. As a result, during the transformer reset period, the primary switch voltage is never lower than $V_{\rm IN}$, which eliminates topological stage C, shown in Fig. 5(c), that makes the operation of one- and two-choke approaches very much different.

III. Size, Cost, Power Density, and Loss Comparisons

A. Magnetic Component Size Comparisons

From the preceding analysis of operation and key waveforms shown in Fig. 4, it can be seen that during the on time of the primary switch, the output-filter inductor current (whose average is load current I_o) of two interleaved forward converters with one choke flows through the module with the conducting switch. On the other hand, in the two-choke interleaved circuit, only one half of the load current flows through each module. Nevertheless, the primary-switch currents in both implementations are the same because the turns ratio of the transformers in the one-choke implementation can be twice as high as that in the two-choke implementation. Namely, in the one-choke implementation, the input of the output filter "sees" the voltage waveform which has the frequency that is twice the switching frequency. As a result of doubled volt-second product at the input of the output filter, the turns ratio of the transformers in the one-choke implementation can be doubled compared to that of the two-choke implementation with the same duty cycle.

Finally, it should be noted that the transformer flux excitation is different in the one- and two-choke approaches. Specifically, as can be seen from $V_{\rm sec1}$ and $V_{\rm sec2}$ waveforms in Fig. 4, the transformer in the one-choke implementation exhibits two periods with positive volt-second product during a switching cycle. Therefore, the operating point of the transformer core goes through two minor B-H loops, which create a small additional core loss.

To compare the sizes of the output inductors in the two interleaved approaches, the inductor current ripples need to be determined first. For the two-choke approach, the current ripple in each inductor shown in Fig. 3 is

$$\Delta I_{Lf(2L)} = \frac{V_o(1-D)}{L_{f(2L)} \cdot f_s} \tag{1}$$

where V_o is the output voltage, $L_{f(2L)}$ is the output-filter inductance, and f_s is the switching frequency. With the inductor current ripple cancellation, the ripple current of the output-filter capacitor becomes

$$\Delta I_{Cf(2L)} = \frac{V_o(1-2D)}{L_{f(2L)} \cdot f_s} \tag{2}$$

which is lower than that in (1).

Since the size of an inductor is proportional to its stored energy, the combined volume of the two output-filter inductors is proportional to the total stored energy

$$E_{(2L)} = 2\left[\frac{1}{2}L_{f(2L)}\left(\frac{I_o}{2}\right)^2\right] \tag{3}$$

where I_o is the output current. Calculating $L_{f(2L)}$ from (2) and substituting it in (3) yield

$$E_{(2L)} = \frac{V_o I_o^2}{4\Delta I_{Cf(2L)} f_s}(I-2D). \tag{4}$$

Since in the one-choke approach, the effective frequency "seen" by the output LC filter is twice the switching frequency, the output-filter-inductor current ripple, shown in Fig. 4, is

$$\Delta I_{Lf(1L)} = \frac{V_o(1/2-D)}{L_{f(1L)} \cdot f_s}. \tag{5}$$

Because no ripple-cancellation effect is present in the one-choke approach, the output-filter capacitor current is also given by (5), i.e.,

$$\Delta I_{Lf(1L)} = \Delta I_{Cf(1L)} = \frac{V_o(1-2D)}{2L_{f(1L)} \cdot f_s}. \tag{6}$$

Finally, the filter-inductor size of the one-choke implementation is proportional to

$$E_{(1L)} = \frac{V_o I_o^2}{4\Delta I_{Cf(1L)} f_s}(1-2D). \tag{7}$$

Comparing (4) and (7), it can be seen that with the same specifications and the same duty cycle, the two implementations will have the output inductors of the same size, provided that both implementations are designed to have the same capacitor ripple currents ΔI_C.

As explained earlier, the turns ratio of the transformers in the one-choke implementation is double that in the two-choke approach $(n_{(1L)} = 2 \cdot n_{(2L)})$, while the primary currents in both implementations are the same. As a result, if the same size core and the same number of secondary turns are used in both implementations, the one-choke implementation has flux excursion which is only one half of that in the two-choke approach. Consequently, the core loss of the one-choke approach is lower. Also, the smaller flux excursion in the one-choke approach creates an opportunity to reduce the size of the transformer by having a tradeoff between the size and core loss. However, the size reduction of the transformer in the one-choke approach is limited by the available winding area to fit the increased number of primary turns.

B. Cost and Power Density Comparisons

The costs of the two implementations are expected to be similar. Namely, both implementations have identical primary circuits, where as their secondary sides are slightly different. Specifically, the two-choke implementation has one more rectifier and one more inductor compared to the one-choke implementation. However, since in the two-choke implementation each rectifier conducts one half of the current conducted

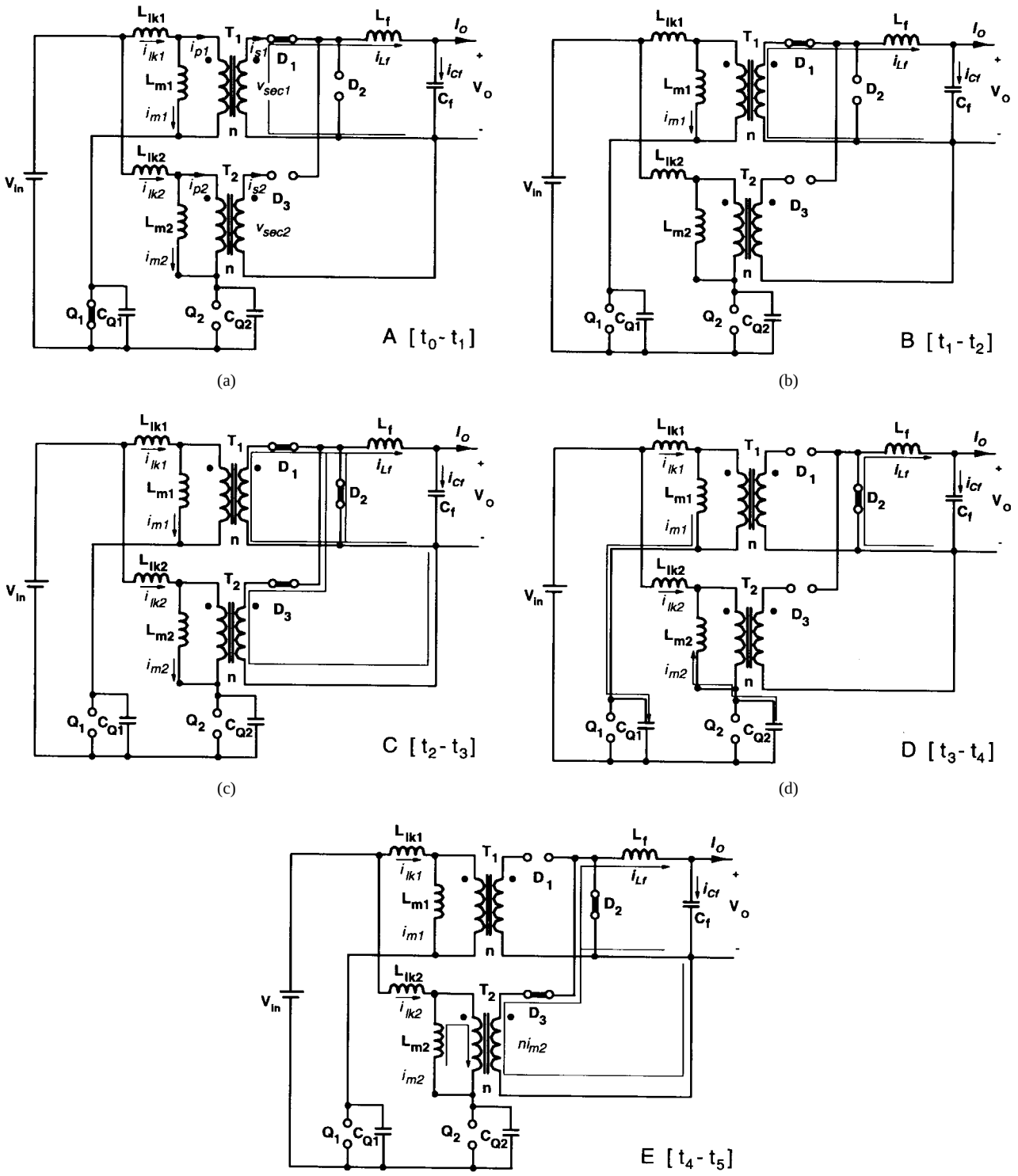


Fig. 5. Equivalent topological stages (TS's): (a) $A[t_0 - t_1]$, (b) $B[t_1 - t_2]$, (c) $C[t_2 - t_3]$, (d) $D[t_3 - t_4]$, and (e) $E[t_4 - t_5]$.

by the corresponding rectifier in the one-choke implementation, the silicon area and, therefore, the total cost of the rectifiers in both implementations is similar. In addition, because the combined size (volume and weight) of the cores of the two inductors in the two-choke implementation is similar to the core size of the inductor in the one-choke approach (if both circuit are designed with the same current-ripple in the output-filter capacitor), the cost of the chokes in both approaches is similar. Finally, for the same ripple in the output-filter capacitance, the size and cost of the output-filter capacitors are identical.

The power density of the one-choke implementation is expected to be higher than that of the two-choke implementation. Although the two-choke implementation has more components

TABLE I
COMPONENT LIST OF POWER STAGES OF TWO- AND ONE-CHOKE IMPLEMENTATIONS

		Two-Choke Implementation	One-Choke Implementation
Q_1, Q_2		IRF640 (International Rectifier)	
D_1, D_2		82CNQ30 (International Rectifier)	
T_1, T_2	core:	TDK PC30LP23/8Z-12	
	primary	9 turns of 4 strands of #26 wire	12 turns of 3 strands of #26 wire
	secondary	3 turns of 3 mils Cu foil	2 turns of 3 mils Cu foil
	Lm	108 μH	214 μH
	L_{lk}	200 nH	325 nH
	R_{sec}	6.7 mΩ	3.4 mΩ
C_{Q1}, C_{Q2}		1 nH ceramic	3.3 nH ceramic
L_{F1}, L_{F2}	core	Magnetics MPP55304	Magnetics Kool Mμ^{TR} 77310
	winding	10 turns of 2 strands of #17 wire	4 turns of 5 strands of #17 wire
	inductance	10.5 μH	3.85 μH
C_F		4400 μF electrolytic	

on the secondary side than the one-choke implementation and, therefore, requires a slightly larger board area, the one-choke approach has significantly lower minimum full-load efficiency (4% difference), which requires a larger heat sink to maintain similar junction temperatures of the semiconductor components as in the two-choke implementation.

C. Loss Comparisons

Because the output power in the two-choke approach is evenly distributed between the two interleaved modules, the total conduction losses of the transformers, primary switches, and rectifiers are

$$P_{(2L)}^{\text{cond}} = 2\left\{\left[\left(\frac{I_o}{2n_{(2L)}}\right)^2 R_{\text{pri}(2L)} + \left(\frac{I_o}{2}\right)^2 R_{\text{sec}(2L)} + \left(\frac{I_o}{2n_{(2L)}}\right)^2 R_{\text{DS(on)}}\right] D + V_F \frac{I_o}{2}\right\} \quad (8)$$

where $R_{\text{pri}(2L)}$ and $R_{\text{sec}(2L)}$ are the primary- and secondary-winding resistances of the transformers, respectively, $R_{\text{DS(on)}}$ is the on resistance of the primary switches, and V_F is the forward voltage drop of the rectifiers.

Similarly, because the output current in the one-choke implementation flows through only one module during the on time, the conduction losses are given by

$$P_{(1L)}^{\text{cond}} = 2\left[\left(\frac{I_o}{n_{(1L)}}\right)^2 R_{\text{pri}(1L)} + I_o^2 R_{\text{sec}(1L)} + \left(\frac{I_o}{n_{(1L)}}\right)^2 R_{\text{DS(on)}}\right] D + V_F I_o \quad (9)$$

where $R_{\text{pri}(1L)}$ and $R_{\text{sec}(1L)}$ are the primary- and secondary-winding resistances of the transformers, respectively. If the two converters are designed to have the same duty cycles and $n_{(1L)} = 2 \cdot n_{(2L)}$, the conduction losses on the primary side, i.e., the primary switch and primary winding losses, are the same. Assuming that rectifier-loss difference between the one- and two-choke implementations is small, the conduction loss difference for $n_{(1L)} = 2 \cdot n_{(2L)}$ can be calculated from (8) and (9) as

$$\Delta P^{\text{cond}} = \left(2R_{\text{sec}(1L)} - \frac{1}{2}R_{\text{sec}(2L)}\right) I_o^2 D. \quad (10)$$

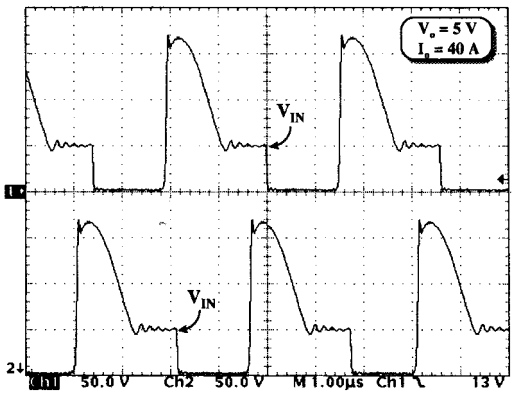
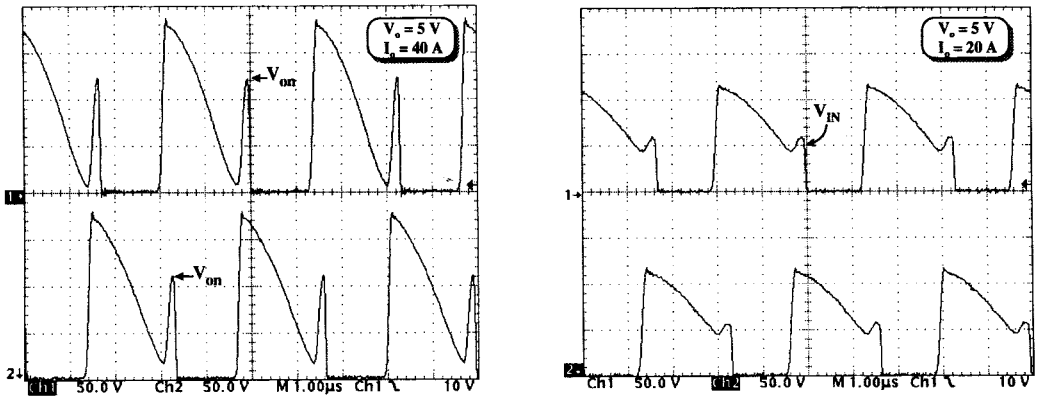


Fig. 6. Experimental $V_{\text{DS}(Q1)}$ and $V_{\text{DS}(Q2)}$ waveforms of two-choke implementation for $V_{\text{IN}} = 50$ V. Scales: $V_{\text{DS}(Q1)} = 50$ V/div., $V_{\text{DS}(Q2)} = 50$ V/div., and time = 1 s/div.

Generally, the difference between the switching losses of the primary switches in the one- and two-choke implementations is caused by the differences in the capacitive turn-on switching losses. Namely, the turn-on and turn-off switching losses due to the overlapping primary-switch voltages and currents are the same in both implementations because in both implementations the primary switches conduct the same current and block the same voltages if $n_{(1L)} = 2 \cdot n_{(2L)}$. However, the capacitive



(a) (b)

Fig. 7. Experimental $V_{\mathrm{DS}(Q1)}$ and $V_{\mathrm{DS}(Q2)}$ waveforms of one-choke implementation for $V_{\mathrm{IN}} = 50$ V. (a) At full load, $I_o = 40$ A. (b) At 50% of full load, $I_o = 20$ A. Scales: $V_{\mathrm{DS}(Q1)} = 50$ V/div., $V_{\mathrm{DS}(Q2)} = 50$ V/div., and time $= 1$ s/div.

TABLE II
COMPARISON OF TWO- AND ONE-CHOKE IMPLEMENTATIONS AT NOMINAL INPUT VOLTAGE (50 V) AND FULL-LOAD CURRENT (20 A)

	Two-Choke Implementation	One-Choke Implementation
Duty Cycle	30%	30%
Turn-On Voltage (V_{on})	50 V	122 V
Efficiency (V_{on})	81.5%	76.8%

turn-on switching losses may be different because the primary switches in the two implementations may be turned on while having different voltages across them.

In fact, according to Fig. 2, the primary switches in the two-choke implementation always turn on with the voltage across the switch equal to input voltage V_{IN}. As a result, the total capacitive turn-on switching loss of two interleaved modules is given by

$$P_{(2L)}^{\mathrm{sw}} = 2\left(\frac{1}{2}C_Q V_{\mathrm{IN}}^2\right) f_s. \tag{11}$$

In the one-choke implementation, the primary switches may turn on when their voltages are larger than V_{IN}, generating the capacitive turn-on switching loss

$$P_{(1L)}^{\mathrm{sw}} = 2\left(\frac{1}{2}C_Q V_{\mathrm{on}}^2\right) f_s, \qquad V_{\mathrm{on}} \geq V_{\mathrm{IN}} \tag{12}$$

where V_{on} is the voltage across the switches at the moment of turn-on. Therefore, the difference in the switching losses of the two interleaving implementations is

$$\Delta P^{\mathrm{sw}} = \left(C_{Q(1L)} V_{\mathrm{on}}^2 - C_{Q(2L)} V_{\mathrm{in}}^2\right) f_s, \qquad V_{\mathrm{on}} \geq V_{\mathrm{IN}}. \tag{13}$$

From (13), it can be seen that if $C_{Q(1L)} = C_{Q(2L)}$ the capacitive turn-on switching loss of the one-choke implementation is higher than or equal to that of the two-choke implementation because $V_{\mathrm{on}} \geq V_{\mathrm{IN}}$.

IV. EXPERIMENTAL EVALUATIONS

Evaluations of the discussed one- and two-choke interleaved forward converters were performed on 300-kHz 5-V/40-A power stages designed to operate in the 40–60-V dc-input-voltage range. The components used in the implementations of the power stages of the two-choke implementation, shown in Fig. 1, and the one-choke implementation, shown in Fig. 2 are summarized in Table I. As can be seen from Table I, due to a larger number of primary turns, the leakage inductances of the transformers in the one-choke implementation are larger than those of the two-choke approach. As a result, to keep the same voltage stress on the primary switches in both implementations, larger resonant capacitances C_{Q1} and C_{Q2} are selected in the one-choke implementation.

Fig. 6 shows the oscillogram of the primary-switch voltages of the two-choke interleaved forward converters. As can be seen from Fig. 6, the switches always turn on when the voltage across them is equal to the input voltage, i.e., $V_{\mathrm{on}} = V_{\mathrm{IN}}$.

Fig. 7 shows the oscillograms of the primary-switch voltages of the one-choke implementation at full load and 50% of the full load. As can be seen from Fig. 7(a), at full load the primary switches turn on when the voltage across them is higher than V_{IN}. Specifically, the switches turn on with $V_{\mathrm{on}} \approx 122$ V, although $V_{\mathrm{IN}} = 50$ V. However, at the half of full load, the switches turn on with $V_{\mathrm{on}} \approx V_{\mathrm{IN}}$, as shown in Fig. 7(b). In addition, at half load, the resonance between L_m and C_Q never takes switch voltage $V_{\mathrm{DS}(Q)}$ significantly below V_{IN} because of insufficient energy stored in the L_{lk}, as seen in Fig. 7(a). On the other hand, at full load, the energy stored in L_{lk} is more than sufficient to resonate $V_{\mathrm{DS}(Q)}$ all the way down to 10–20 V, as shown in Fig. 7(a).

The measured full-load efficiencies of the one- and two-choke implementations as functions of the input voltage are

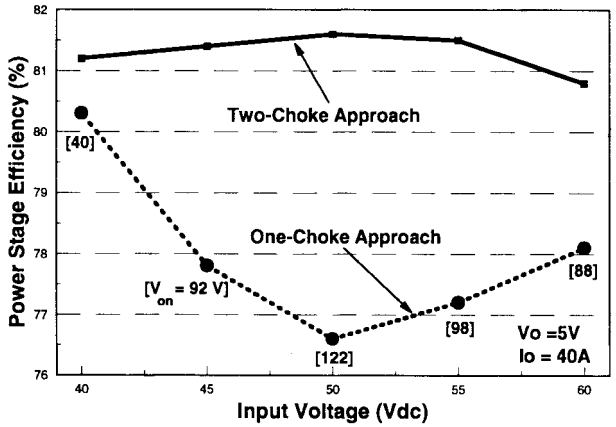


Fig. 8. Measured full-load efficiencies of one- and two-choke implementations as functions of input voltage. For one-choke implementation, $V_{\rm on}$ values for each measured point are indicated. For two-choke implementation, $V_{\rm on} = V_{\rm IN}$.

shown in Fig. 8. As can be seen, the efficiency of the two-choke implementation is higher than the efficiency of the one-choke implementation in the entire input-voltage range. Moreover, the efficiency of the one-choke implementation is a strong function of the input voltage, while the efficiency of the two-choke implementation is almost independent of the input voltage. In fact, according to Fig. 8, the two-choke circuit is around 1% more efficient than the one-choke circuit at $V_{\rm IN} = 40$ V and approximately 5% more efficient at $V_{\rm IN} = 50$ V. The input-voltage dependence of the efficiency of the one-choke implementation is caused by increased conduction and particularly switching losses compared to the corresponding losses in the two-choke circuit. The conduction loss difference is brought about by the secondary winding resistance difference between the transformers in the two implementations, while the switching loss difference is caused by the difference in the switch voltage at the turn on. For example, by using component values from Table I, the duty cycles of the primary switches (which are the same in both implementations) at $V_{\rm IN} = 50$ V can be calculated from

$$D = \frac{n_{(2L)} V_o}{V_{\rm IN}} = \frac{n_{1-L} V_o}{2 \cdot V_{\rm IN}} = \frac{3 \cdot 5}{50} = 30\%. \tag{14}$$

According to (10), the conduction loss increase of the one-choke implementation over the two-choke implementation at full load of 40 A can be calculated as

$$\Delta P^{\rm cond} = \left(2 \cdot 3.4 \cdot 10^{-3} - \frac{1}{2} \cdot 6.7 \cdot 10^{-3}\right) 40^2 \cdot 0.3 = 1.7 \text{ W}. \tag{15}$$

To calculate the capacitive turn-on switching loss difference of the two implementations, Fig. 8 also shows measured primary-switch voltages at turn-on, $V_{\rm on}$, for each measured point of the one-choke circuit. For example, for $V_{\rm IN} = 40$ V, $V_{\rm on} = 40$ V, i.e., $V_{\rm IN} = V_{\rm on}$. However, for $V_{\rm IN} = 50$ V, $V_{\rm on} = 122$ V $\gg V_{\rm IN}$. In fact, by applying (13), the increased switching loss of the one-choke approach is

$$\Delta P^{\rm sw} = (3.3 \cdot 10^{-9} \cdot 122^2 - 1 \cdot 10^{-9} \cdot 50^2) \cdot 300 \cdot 10^3 \approx 14.0 \text{ W} \tag{16}$$

at $V_{\rm IN} = 50$ V and $I_o = 40$ A. Therefore, the one-choke implementation dissipates approximately 15.7 W more than the two-choke implementation. The calculated power dissipation is in a very good agreement with the experiment data because at $V_{\rm IN} = 50$ V, the measured efficiencies are 81.5% and 76.8% for the one- and two-choke implementations, respectively. This efficiency difference corresponds to a 15.5-W power dissipation difference. The comparison of the one- and two-choke implementations at the nominal input voltage (50 V) and full load current (20 A) is summarized in Table II.

V. Summary

Analysis, design, and performance evaluations of two interleaved forward converters with common output-filter inductor (one-choke approach) and separate output-filter inductors (two-choke approach) are presented. It was shown that the operation of the one-choke implementation of the two interleaved forward converters with the resonant or RCD clamp resets is quite different from that of the corresponding one-choke implementation. In addition, the two interleaved approaches were compared with respect to their output-filter sizes and power losses. It was shown that the one-choke approach is less efficient than the two-choke approach. Finally, the analysis and evaluation results were verified experimentally.

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