Analysis and Implementation of High Gain Non-isolated DC-DC Boost Converter

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Abstract: High step-up dc-dc converters are increasingly required in many industrial applications. Conventional topologies operate at extreme duty cycle, high semiconductor voltage stress, switching loss, and diode reverse recovery problems. This paper presents a new non-isolated high gain, boost converter operating with a modest duty cycle by integrating a coupled inductor and switched capacitor technique. Importantly, the structure of the high voltage side, together with the switched capacitor, reduces the voltage stress of the power switch to less than one third of the output voltage, which in turn helps to reduce the conduction loss by using a low on-resistance switch. The diode voltage stress is less than the output voltage which facilitates faster recovery. Furthermore, the converter employs a passive clamp circuit to recycle the leakage energy. The main switch achieves zero current switching (ZCS) turn-on performance and all diodes achieve (ZCS) turn off reducing reverse recovery related losses. As a result, the circuit exhibits high efficiency performance; which is essential for most modern power electronic applications. In this paper, the operational principle and performance characteristics of the proposed converter is presented and validated experimentally with a 250 W, 20 V input voltage / 190 V output voltage prototype circuit.

1. Introduction

There is an increasing demand for high gain dc-dc converters in many applications, such as renewable energy, energy storage, and electric vehicle applications. Classical isolated power converters, such as the flyback or push-pull, can readily achieve the necessary high gain by adjusting the transformer turns ratio [1]. In addition, proper turns ratio design minimizes the voltage or current stress imposed on the power devices [2]. Unfortunately, a snubber circuit is necessary to overcome the problem of large voltage spikes suffered by the primary switch at turn-off (due to leakage inductance interaction with the parasitic capacitor of the power switch). Likewise, non-isolated topologies such as switched capacitors [3]; voltage multiplier cells [4],[5] and voltage lift circuits [6]; all require more elaborate control strategies and multiple cells to achieve high voltage conversion ratios. This typically results in complex structures.

A common alternative technique is to use a coupled inductor or transformer to provide another controllable degree of freedom rather than the duty cycle, to enlarge the voltage gain [7-10]. Coupled inductor boost converters can provide high voltage gain without extreme duty cycle operation, with a relatively simple topology and fewer components. Consequently, they can reduce the switch voltage stress and allow the use of low voltage rated, high

performance, semiconductor devices. However, the main drawbacks of coupled inductor converters include severe voltage spikes across the switch due to the leakage energy of the coupled inductor and the large input current ripple.

Beside capacitor charge transference methods [3-6] and magnetic coupling converters [7-9] one can find other promising hybrid topologies for high step-up dc-dc conversion integrating coupled inductors and switched capacitors mainly for high voltage gain [10-17]. This technique can achieve the voltage doubler, tripler and quadrapler and has been successfully applied in many converters to achieve good overall performance. As previously explained, an active clamp circuit (ACC) is usually employed in transformer based converters to limit the switch voltage excursion seen by the primary switch (as a result of leakage inductance interaction with parasitic capacitance of the switch), realizes zero voltage switching (ZVS) of the active switches and subsequent lowering of the output diode reverse recovery losses [1], [8], [14], [17]. However, the ACC increases the cost of the converter and additional conduction losses. Furthermore, an overlap in the circuit can lead to failure of the circuit, thereby reducing the reliability of the circuit. The limitation presented by the ACC can be overcome by passive clamp circuit (PCC) and improve the reliability of the circuits. The use of PCC to recycle the leakage inductor energy in magnetically coupled converters is well documented [10-12]. The PCC not only recycles the leakage inductance energy, but also takes a shorter period of time to discharge the leakage energy compared to the ACC. Therefore, the PCC has less circulating energy in the clamp circuit.

This paper proposes a new boost dc-dc converter topology integrating coupled inductor and switched capacitor to configure a voltage gain extension cell. The coupled inductor can be designed to extend the static gain and the switched capacitor offers additional voltage gain. Here, the two capacitors are charged in parallel by the coupled inductor and discharged in series to enlarge the voltage gain. Unlike the conventional boost converter, the energy is transferred to the load when the power switch conducts and the output capacitor supplies the load. In essence, the high voltage dc bus floats with respect to the input voltage source. A passive loss-less clamp circuit is employed to recycle the leakage inductance energy whilst minimizing the turn-off voltage spike across the main switch. Importantly, the clamp circuit provides a mechanism of achieving zero current switching (ZCS) for the main switch and subsequent reduction of the output and regenerative diodes current falling rate. Consequently, the diode switching losses and output switching noise are decreased. In addition, low rated semiconductor devices can be used, which in turn helps to reduce conduction losses. In the following, the operating principles of the proposed dc-dc converter are described in full

detail. Experimental results from a 250 W prototype circuit are then presented to validate the advantageous performance and operation of the high voltage gain circuit.

2. Converter Operational Analysis

2.1 Circuit Description

Fig. 1 shows the circuit configuration of the proposed high step-up boost converter. The converter employs one coupled inductor denoted as L. The primary and secondary windings of the coupled inductor are denoted as $L_a$and L_b respectively. The primary winding L_a serves as a filter inductor, similar to a conventional flyback converter, and is coupled to its corresponding secondary winding L_b. The primary and secondary windings of the coupled inductor is represented by n_1 and n_2, and the coupling reference denoted by ‘’*’’. The converter main switch is denoted by S. The passive clamp circuit consists of clamp diode D_C and the clamp capacitor C_C as shown in Fig. 1(a). The voltage extension cell consists of the secondary winding of the couple inductors L_b, the clamp diode D_C, clamp capacitor C_C, regenerative diode D_r and the switched capacitor C_m. D_O, C_O are the output diode and filter capacitor; R_O denotes the output resistive load.

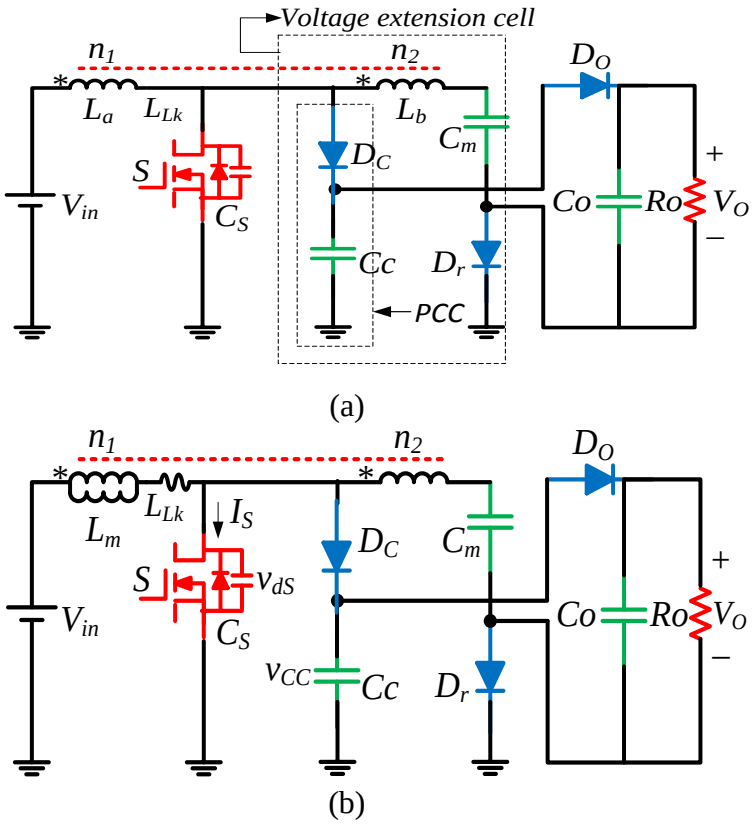


Fig. 1. *Circuit configuration of the proposed converter*
a) Circuit configuration
b) Equivalent circuit

Fig. 1(b) shows the equivalent circuit of the proposed high step-up boost converter. The coupled inductor can be modelled as an ideal transformer with defined turns ratio. The ideal transformer primary winding is in parallel with magnetizing inductor L_m and then in series with a leakage inductance [12], [14]. V_{in}, V_O are the input and output voltages of the converter respectively.

To simplify the converter analysis the following assumptions are made:

1) The power switch is ideal, but the parasitic capacitor is considered in the analysis.
2) Capacitors C_C, C_m and C_O are large enough. Thus, their voltages are constant in one switching cycle.
3) The turns ratio of the coupled inductor N is equal to n_2/n_1 and coupling coefficient k is expressed as $L_m/(L_{Lk} + L_m)$

2.2 Operational Modes

The following discussion is confined to continuous conduction mode (CCM) operation, since the converter design is based on CCM and the operation is guaranteed throughout the full range of the duty cycle variation with resistive loads. During steady state operation, the duty cycle D is higher than 0.5. The clamp diode D_C turns on and off naturally. Some typical steady state waveform of the proposed converter in CCM operation is shown in Fig. 2 There are five modes of operation in one switching cycle; the equivalent circuits and current flow path corresponding to each operational stage are shown in Fig. 3. The converter operation is analysed as follows:

Mode 1 $[t_0 - t_1]$ (Fig. 3a): Before time t_1, the main switch S is conducting. The clamp diode D_C and output diode D_O are reversed biased whilst the regenerative diode D_r is also conducting. The current through regenerative diode decreases linearly, and the current decrease rate is controlled by the leakage inductance L_{LK}. Magnetizing inductance L_m is charged by the input voltage V_{in}, whilst the switched capacitor is charged through the coupled inductor secondary winding. The load is supplied by the output capacitor. The voltage across the leakage and magnetizing inductors is denoted by

$$L_{Lk}\frac{d_{iLk}}{dt} = V_{in} - V_{Lm} \tag{1}$$

$$V_{Lm} = -\frac{V_{Cm}}{N} \tag{2}$$

Mode 2 $[t_1 - t_2]$ (Fig. 3b): The regenerative diode D_r turns off softly at time t_1 under ZCS, which minimizes the regenerative diode reverse recovery losses. The leakage inductor current

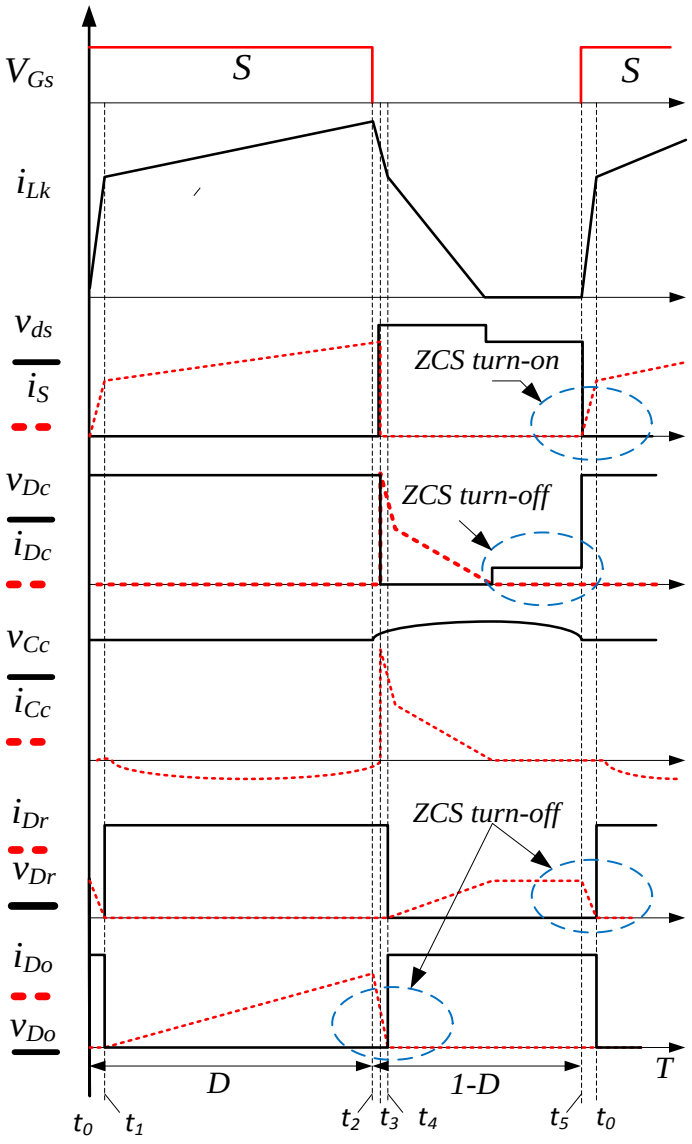


Fig. 2. *Key waveforms of the proposed converter*

increases linearly as a result of being charge by the input voltage. The output diode D_O becomes forward biased to deliver the input energy to the load. During this time the clamp capacitor C_C, the switched capacitor C_m and the coupled inductor secondary winding are in series to enlarge the voltage gain. Meanwhile, the converter operates in flyback mode to supply the load. The leakage inductor voltage is given by

$$L_{Lk}\frac{d_{iLk}}{dt} = V_{in} - \left(\frac{V_O - V_{Cc} - V_{Cm}}{N}\right) \tag{3}$$

Mode 3 $[t_2 - t_3]$ (Fig. 3c): At time t_2 the main switch S turns off. The clamp diode D_C , the regenerative diode D_r are still reversed biased whilst the output diode D_O is forward biased. The leakage inductor current charges the parasitic capacitor of the switch. This mode is very short and ended when $V_{Cc} \cong V_{ds}$.

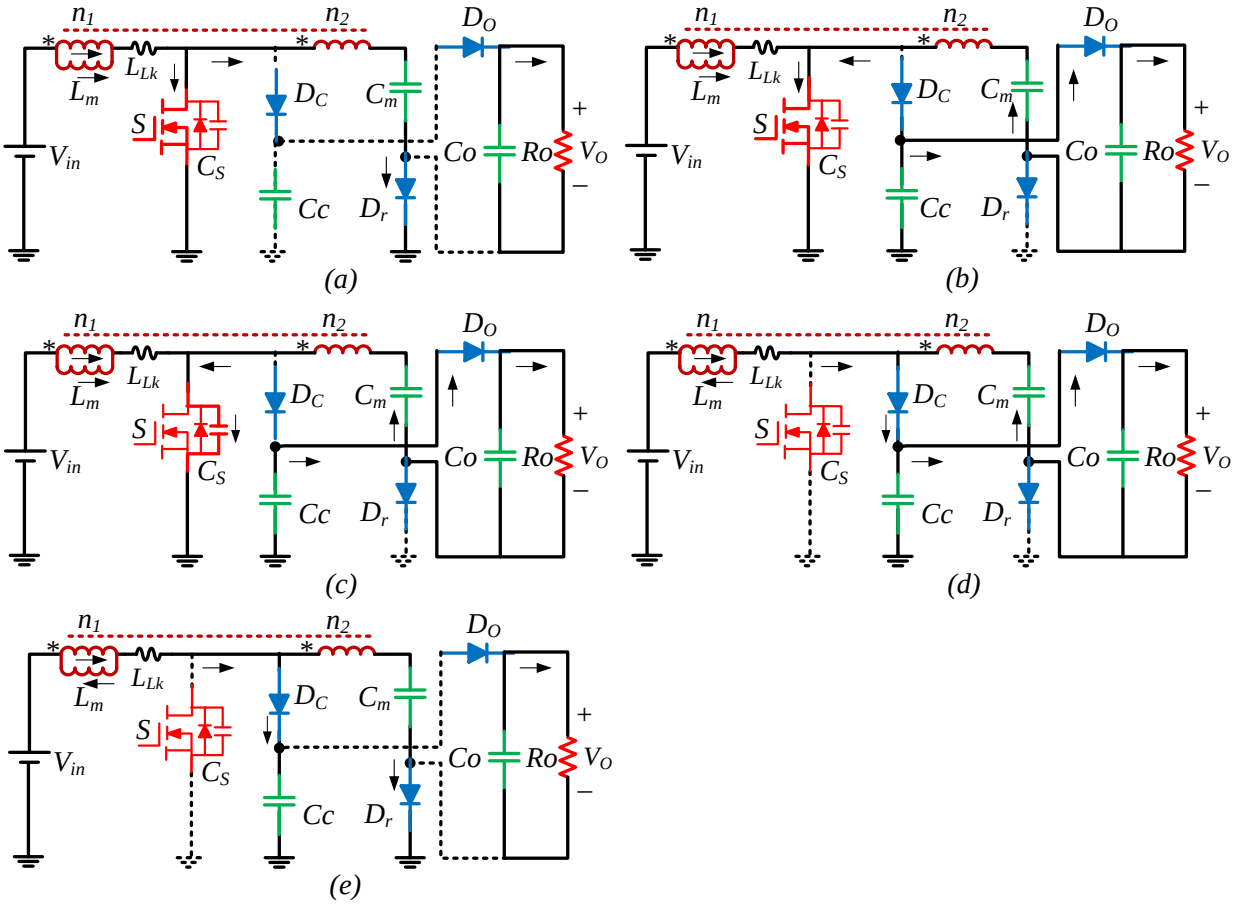


Fig. 3. *Operational modes equivalent circuit*
(a) Mode 1 $[t_0 - t_1]$, (b) Mode 2 $[t_1 - t_2]$, (c) Mode 3 $[t_2 - t_3]$,(d) Mode 4 $[t_3 - t_4]$, (e) Mode 5 $[t_4 - t_5]$

Mode 4 $[t_3 - t_4]$ (Fig. 3d): The voltage across the switch S rises to the clamp capacitor voltage and the clamp diode D_C becomes forward biased. The leakage inductor current i_{Lk} is commutated to the clamp diode and the leakage inductance energy is released to the clamp capacitor C_C. The voltage across the switch S is clamped to the clamp capacitor voltage V_{Cc}. During this time, the leakage inductor current and that of output diode D_O decreases linearly. The current decrease rate of the output diode is controlled by the inherent leakage inductance of the coupled inductor. The voltage across the leakage inductor V_{Lk} is given by

$$L_{Lk}\frac{d_{iLk}}{dt} = V_{in} - \left(\frac{V_O - V_{Cc} - V_{Cm}}{N}\right) - V_{Cc} \tag{4}$$

Mode 5 $[t_4 - t_5]$ (Fig. 3e): The output diode turns off softly under ZCS at the end of mode 4. The regenerative diode D_r begins to conduct, the diode current rises linearly and that of the leakage inductance decreases linearly. The clamp and switched capacitor are now charged in parallel by the input voltage source V_{in}. The load is supplied by the output capacitor during this time. At the end of this mode the clamp diode D_C turns off naturally at time t_5, and the main switch S turns on with ZCS performance minimizing the switching losses. The leakage inductor voltage during this time is

$$L_{Lk}\frac{d_{iLk}}{dt} = V_{Cm} - V_{Cc} \tag{5}$$

3. Circuit Analysis

3.1 Voltage Conversion Ratio

The parasitic parameters inherent in the power devices are not included in the analysis; this includes the leakage inductance of the coupled inductor. The magnetising inductor current is also considered to be linear. The switching period consists of the on and off period. When the power switch is in the on state, the magnetizing inductor is charged linearly by the input voltage. Applying KVL, the voltage across the magnetizing inductor is given by

$$V_{in} = V_{Lm} \tag{6}$$

During the same time instant, diode D_r is reversed blocking and the output diode D_O is forward conducting, the clamp capacitor and switched capacitor discharge in series and the power is transferred to the load; the output voltage can be described by

$$V_O = V_{Cm} + V_{Cc} + NV_{in} \tag{7}$$

By applying the inductor volt-second balance principle to the clamp capacitor, the voltage across the clamp capacitor can be expressed as

$$V_{Cc} = \frac{V_{in}}{(1-D)} \tag{8}$$

When the main switch *S* turns off, the clamp and regenerative diode turns on, the clamp and switched capacitors are charged in parallel by the input voltage, the voltage across the switched capacitor is derived as

$$V_{Cm} = N(V_{Cc} - V_{in}) + V_{Cc} \tag{9}$$

From (6)-(9), the ideal voltage gain is derived

$$M_{ideal} = \frac{V_O}{V_{in}} = \frac{N+2}{(1-D)} \tag{10}$$

The coupled inductor turns ratio N can be adjusted to achieve the desired voltage conversion ratio without resorting to extreme duty cycle operation. The relationship between the static gain, duty cycle and turns ratio is plotted in Fig. 4. When the coupled inductor turns ratio is zero, the voltage gain of the proposed circuit is higher than that of the conventional boost converter. The voltage gain increases significantly at higher turns ratio.

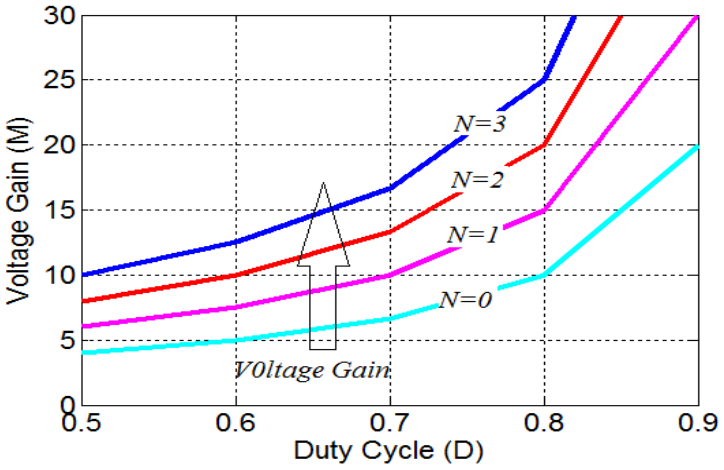


Fig. 4. *Voltage gain as a function of D and N values*

3.2 Leakage Inductance Effect

It is practically impossible to achieve hundred percent coupling between the primary and secondary windings of the coupled inductor. The passive clamp circuit is usually employed to limit the switch voltage excursion (due leakage inductance interaction with parasitic capacitance of the switch). The ZCS turn on performance of the switch is achieved due to leakage inductance. In addition, the leakage inductance controls the current falling rates of the diodes and effectively alleviates their reverse recovery problem. The voltage gain is derived easily by neglecting the short operating intervals and averaging the output voltage V_O during ON and OFF intervals. Therefore, during the switch ON instant one get the following equations

$$C_O \frac{dv_O}{dt} = \frac{v_O - v_{cm} - v_{Cc} - Nv_{in}}{NL_K} - \frac{v_O}{R_O} \tag{11}$$

And the OFF state equation is given by

$$C_O \frac{dv_O}{dt} = -\frac{v_O}{R_O} \tag{12}$$

Using the state space average method, the average equation that describe (11) and (12) is given by

$$\langle \frac{dv_O}{dt} \rangle = \frac{(NL_K f_s(N + dN) + dR_o)d'v_o}{NL_K C_o R_o d} - \frac{v_{in}(N+2)}{NL_K C_o} \tag{13}$$

Where $d' = (1 - d)$. The state space average DC model that describe the equilibrium point of the output voltage can be obtained by letting the left-hand side (LHS) of (13) equal to zero, from which

$$M = \frac{V_O}{V_{in}} = \frac{N+2}{(1-D)} \cdot \frac{DR_o}{(NL_K f_s(N + DN) + DR_o)} \tag{14}$$

From (14), it is reasonable to conclude that the voltage gain is a function of switching frequency, resistive load and leakage inductance other than the coupled inductor turns ratio. The relationship between the voltage gain, duty cycle, turns ratio and leakage inductance is plotted in Fig. 5. It is apparent that the leakage inductance degrades the voltage gain of the converter.

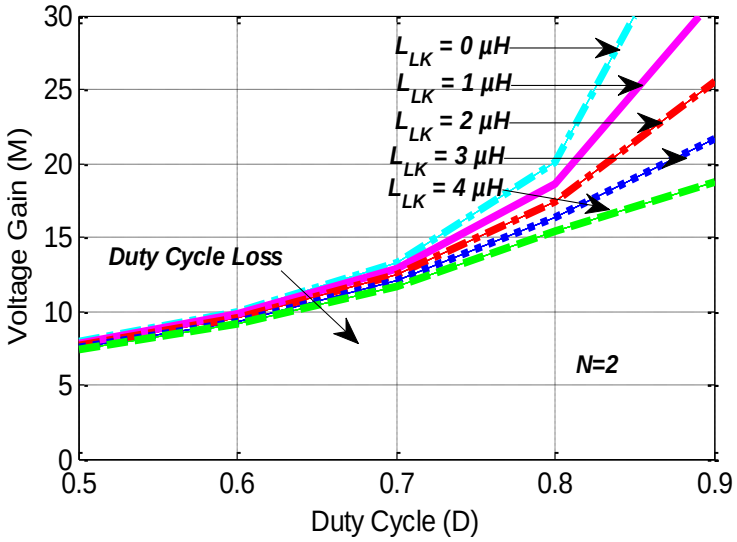


Fig. 5. *Voltage gain characteristic of the converter including the leakage inductance effect*

Based on the preceding analysis, it is fair to conclude that the leakage inductance causes duty cycle loss which leads to the static gain loss given by

$$\Delta D = \frac{2I_{in}L_{LK}f_S}{V_{in}D + NDV_O} \tag{15}$$

The duty cycle loss is proportional to the input current, leakage inductance and switching frequency

3.2 Power Devices Voltage Stress

By neglecting the voltage ripple on the clamp capacitor, the voltage stress of the switch S and clamp diode D_C are the same and are equal to the voltage on the clamp capacitor given by

$$V_S = V_{Dc} = \frac{V_{in}}{(1-D)} = \frac{V_O}{(N+2)} \tag{16}$$

The voltage stress of the switched capacitor is derived from (9) and is expressed as

$$V_{Cm} = \frac{(1+ND)V_{in}}{(1-D)} \tag{17}$$

The voltage stress of the output diode D_O is the same with that of the regenerative diode, which is equal to the difference between the output voltage and the clamp capacitor voltage. However, it is always lower than the output voltage and is expressed as

$$V_{DO} = V_{Dr} \cong V_O - V_{CC} = \frac{(N+1)V_{in}}{(1-D)} \tag{18}$$

The curve relating the normalized semiconductors devices voltage stress and the coupled inductor turns ratio is plotted in Fig. 6. When the turns ratio is zero, the switch voltage stress is equal to half of the output voltage. And the switch voltage stress decreases significantly when the turns ratio increases. Therefore, low-rated high-performance power device can be employed to improve the circuit efficiency. Likewise, the voltage stress of the regenerative and output diode increases as the turns ratio increases.

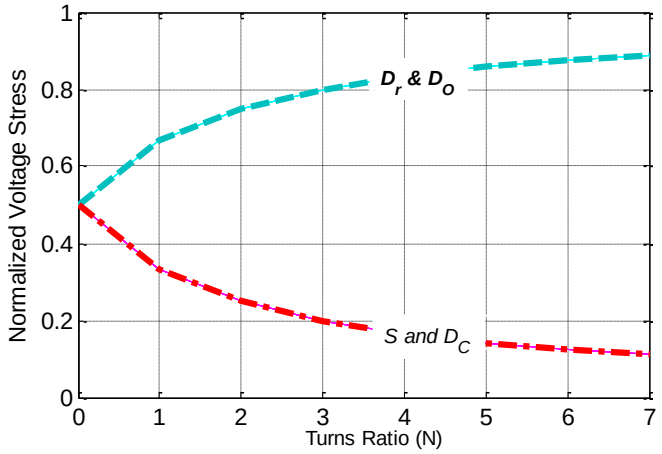


Fig. 6. *Power devices voltage stress reduction effect*

3.2 Current Stress

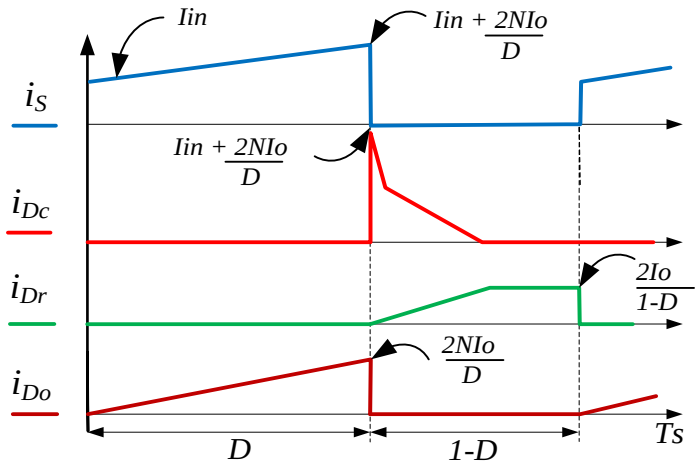


Fig. 7. *Ideal converter current waveforms*

Fig. 7 shows the ideal converter current waveforms for deriving the power devices current stress. Here the clamp diode current is assumed to be linear instead of quasi sinusoidal and all the short switching intervals are therefore neglected. By applying the principle of power balance to the converter, it can be drawn the average current of the regenerative and output diodes are equal to the output current:

$$I_{Do} = I_{Dr} = I_o \tag{19}$$

The peak current of the regenerative and output diodes are:

$$I_{Do\_pk} = \frac{2I_o}{D} \tag{20}$$

$$I_{Dr\_pk} = \frac{2I_o}{(1-D)} \tag{21}$$

During the switch turn on period the switch current is the magnetizing inductor current, and at turn off the current is the summation of magnetizing inductor current and reflected output diode current. Therefore, the switch current at turn off is:

$$I_{S_{turn-off}} = I_{in} + \frac{2NI_o}{D} \tag{22}$$

Considering the conversion efficiency to be 100%, the RMS current of the main switch is given by

$$I_{RMS-S} = I_{in}\sqrt{D + \frac{2N(1-D)}{(N+2)} + \frac{4N^2(1-D)^2}{3D(N+2)^2}} \tag{23}$$

The clamp diode current during turn-on is the same with the switch current during turn off. It is also assumed that the clamp diode will conduct the positive portion of the clamp current. With approximately linear clamp current, it implies that the diode will conduct for half of the switch off time period. As a result, the RMS current of the clamp diode is

$$I_{Dc\_RMS} = \left(\frac{1}{T_s}\int_0^{(1-D)T_s/2}\left(I_{in} + \frac{2NI_o}{D}\right)^2 (t)dt\right)^{1/2} \tag{24}$$

$$I_{Dc\_RMS} = I_{in}\sqrt{\frac{(1-D)}{6}} \tag{25}$$

3.3 ZCS Characteristic of the Switch

The ZCS turn-on characteristic of the power switch is achieved naturally due to the intrinsic leakage inductance of the coupled inductor. The switching loss regarding the converter power switch is calculated using (26)

$$P_{S\_(sw)} = \frac{f_s}{2}(t_r + t_f)\cdot I_{RMS\_S}\cdot V_S \tag{26}$$

Where t_r, t_f are is the power switch rise and fall time of the power switch respectively. During the switch turn-on instant under ZCS there is no overlap between the switch voltage and current, therefore the power loss can be ignored. However, at higher switching frequencies the charge in the internal capacitances is dissipated in the switch and the loss becomes significant [18].

3.3 Diodes Reverse Recovery Alleviation

From the steady state analysis, it can be seen that the clamp diode turns off naturally, which means that there is no reverse recovery related losses. However, the current falling rate of the output diode is controlled by the leakage inductance of the coupled inductor during Mode 3, and is given by:

$$\frac{di_{Do}}{dt} = \frac{V_O}{N(N+2)L_{Lk}} \tag{27}$$

For the regenerative diode, the rate of change of current is equally controlled by the leakage inductance at the end of Mode 4:

$$\frac{di_{Dr}}{dt} = \frac{(N+1)V_O}{N(N+2)L_{Lk}} \tag{28}$$

From (27) and (28), it is reasonable to conclude that the reverse recovery problem is alleviated by the inherent leakage inductance of the coupled inductor. Furthermore as the turns ratio increases, a small leakage inductance is sufficient to alleviate the reverse recovery problem.

3.5 Performance Comparison and With Other Topologies

The performance characteristics of the proposed converter, and other published converters with high gain performance, are analysed by numerical simulation. The characteristics considered include magnetic coupling, single stage and only one power switch. The main parameters taken into account are components count, static gain, duty cycle, turns ratio and power device voltage stress. The comparision can be seen in Table 1

The lowest static gain is obtained with the converter reported in [13]. To mitigate the extreme duty cycle operation and achieve similar output voltage, the turns ratio is slightly increased. However, higher turns ratio amounts to copper loss and the devices voltage stress is higher.

TABLE I POWER DEVICES CURRENT RATINGS OF THE PROPOSED CONVERTERS

Parameter	Topologies		
$V_{in} = 20\ V$ $V_O = 190\ V$	Converter in [13]	Converter in [14]	Proposed Converter
Coupled Inductor	1	1	1
switch	1	1	1
Diode	3	3	3
capacitor	3	3	3
Turns Ratio	1:2.3	1:2	1:1.8
Voltage gain	$\frac{(N+1)}{(1-D)}$	$\frac{(N+2)}{(1-D)}$	$\frac{(N+2)}{(1-D)}$
Switch voltage stress	$\frac{V_O}{N}$	$\frac{V_O}{(N+2)}$	$\frac{V_O}{(N+2)}$
Diodes voltage stress	$\frac{NV_O}{(N+1)}$	$\frac{(N+1)V_O}{(N+2)}$	$\frac{(N+1)V_O}{(N+2)}$
Soft switching performance	ZCS	Hard switching	ZCS
Duty cycle	0.7	0.64	0.64

In addition a start-up circuit is required to limit the inrush current. The highest voltage gain is obtained with the both converter in [14] and the proposed circuit in this paper. However, the converter in [14] operates under hard switching condition. It is worth noting that the proposed converter can realize the same or higher voltage conversion ratio with a lower coupled inductor turns ratio compared to the other two topologies, whilst retaining modest duty cycle performance. Finally, the device voltage stress is kept low, allowing the use of lower rated MOSFETs with low conduction losses and low rated power diodes which typically recover faster.

4. Design Consideration

In this section, a $250\ W$ high step-up boost converter system is adopted as an example to explore the main design consideration of proposed converter with $20\ V$ input voltage and $190\ V$ output voltage respectively.

4.1 Coupled Indutor Design

The coupled inductor turns ratio and nominal duty cycle of the switch is obtained from the ideal voltage conversion ratio in (10) given by

$$N = \frac{V_O}{V_{in}}(1-D) - 2 \tag{29}$$

$$D = 1 - \frac{V_{in}}{V_O}(N+2) \tag{30}$$

The key design step is to choose the coupled inductor turns ratio that gives a modest duty cycle of the power device. Since higher turns ratio results in increased current stress to the power device, a turns ratio of $N = 1.8$ is chosen which gives a corresponding duty cycle of 0.6. Once the coupled inductor turns ratio is selected, the leakage inductance of the coupled inductor is derived from (14) and should satisfy the following:

$$L_{LK} = \frac{R_0 D^2(1-D)[(N+1) - M(1-D)]}{2N^2 M f_s(1-2D+2D^2)} = 0.9\mu H \tag{31}$$

The magnetizing inductor L_m is determined by considering a current ripple ΔI_{Lm} of 25% in the magnetizing inductor current, given by

$$L_m = \frac{V_{in} \cdot D}{\Delta I_{Lm} \cdot f_S} = 77\mu H \tag{32}$$

When the power switch turns off, the voltage across the coupled inductor primary winding is obtained as:

$$V_{La} = \frac{V_O}{(N+2)} = n_1 \frac{\Delta B A_e}{(1-D)T_S} \tag{33}$$

Where ΔB is magnetic flux density variation and A_e is the equivalent area of the magnetic core. The primary winding rms current is obtained from (33)

$$I_{La\_RMS} = \left(\frac{\int_{t_0}^{t_5} i_{La}(t)^2}{T_S} \right)^{1/2} \tag{34}$$

Following this, the coupled inductor is assembled on an off-the-shelf Koolmu toroid magnetic core 077090A7. The primary winding has 32 turns and the secondary winding has 58 turns. The measured magnetizing inductance and the primary leakage inductance are 82 μH and 1.3 μH respectively.

4.2 Clamp and Switched Capacitors Selection

The clamp and switched capacitor serves as a voltage source in the converter, the key design parameter is to suppress the ripple voltage on both the clamp and the switched capacitor. The clamp capacitor value is selected based on [4], by allowing one half of the resonant period not to exceed the maximum turn off time of the main switch; given by

$$C_C = \frac{(1-D)^2}{\pi^2 L_{LK} {f_s}^2} \tag{35}$$

The relationship between the output current and the voltage ripple on the switched capacitor is given by

$$C_m = \frac{I_{out}}{\Delta v_C f_S} \tag{36}$$

Where Δv_C is the voltage ripple on the switched- capacitor.

4.3 Power Device Selection

The voltage and current stress of the power devices is given in (20)-(25), which can be used to determine the power devices selection by considering an acceptable voltage and current margins.

5. Experimental Validation

In order to verify the operation and evaluate the performance of the converter a 20V input, 190 V output 250 W prototype circuit is built and tested in the laboratory. The specification of the converter along with the component ratings are derived from the analysis in section 3. The specifications are listed in Table II.

TABLE II PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Components	Parameters
Dc input voltage V_{in}	20 V
Dc output voltage V_O	190 V
Output power P_O	250 W
Switching Frequency f_s	50 KHz
Coupled inductor	Magnetizing Inductance $L_m = 82\mu H$ Leakage Inductance $L_{Lk} = 1.3\mu H$ Turns ratio N=1:1.8
Power switch $S\ and S_C$	CSD19536KCS ($R_{DS\_on} = 2.3\ m\Omega. C_{0ss} = 2.3nF$)
Diodes $D_C, D_r\ and\ D_O$	MBR42050G
Capacitors	Clamp capacitor $C_C = 4.7\ \mu F$ Switched capacitor $C_m = 10\mu F$ Output capacitor $C_O = 50\mu F$

Fig. 8 shows the key experimental results of the converter. The following experimental results are measured at $250\ W$ full load conditions with $20\ V$ input voltage. The drain source voltage of the power switch V_{ds}, the switch current I_s , and the voltage and current of the clamp diode D_C are shown in Fig. 8(a). It can be seen that the maximum voltage across the devices is 60 V, which is far less than the output voltage. This feature permits low rated power devices with low R_{ds-on} to be employed which significantly reduces conduction loss. Besides, the drain source voltage of the switch falls to zero prior to the application of turn-on

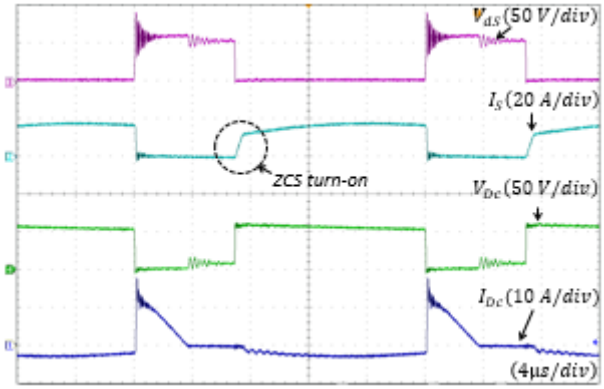
gate signal, so ZCS is achieved for the power switch. The clamp diode turns-off naturally, which means there is no reverse recovery problem. The ZCS performance of the main switch is shown in Fig. 8(b).

The clamp circuit performance along with the converter output voltage is demonstrated in Fig. 8(c). Note that the voltage stress of the clamp capacitor, and clamp diode are the same as that of the power switch. When the main switch turns-off the clamp diode conducts and the leakage inductor energy is transferred to the clamp capacitor. As can be seen the passive clamp circuit uses approximately half of the off time duration to reset the leakage energy to the output. The clamp diode turns off naturally with no reverse recovery related loss.

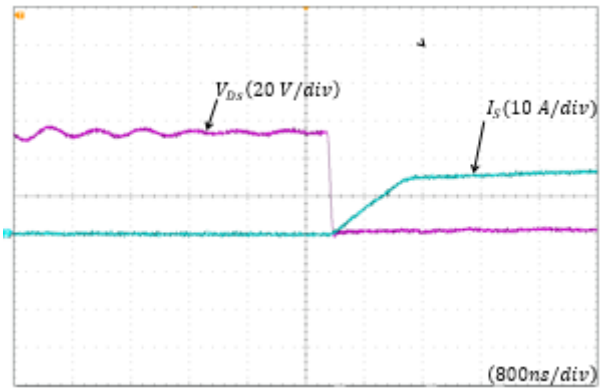
Fig. 8(d) illustrates the voltage across the capacitors (clamp, switched and the output capacitors) of the converter. The experimental result validates the initial assumption of considering the capacitors as constant voltage sources. Fig. 8(e) shows the voltage and current waveforms of the diodes. As can be seen, both the regenerative and output diodes turn off softly with ZCS, leading to much lower reverse recovery losses. Details of the ZCS turn off of the diodes is shown in Fig. 8(f). The current falling rate of the diode is controlled by the leakage inductance. Furthermore, no significant electromagnetic interference (EMI) or noise problems were noted whilst taking the results. The voltage across the diodes is 150 V which is also less than the converter output voltage of 190 V and lower rated power diodes typically recover faster. Fig. 8(g) illustrates the coupled inductor primary and secondary currents. The leakage inductor current is continuous over the entire switching cycle. However, the ripple magnitude of the leakage inductor current is large due to the magnetizing inductor and reflected secondary winding currents. Fig. 9 shows the measured efficiency of the converter under different load conditions. The efficiency is measured using Yokogawa WT310. The measured converter efficiency is 93.5% for a wide load range and the maximum efficiency is 92.5% at full load.

Fig. 10 shows the loss distribution of the converter according to different output power under 20 V input voltage. The dominant losses are the switch conduction and the coupled inductor cupper losses as a result of the high input current. As the load increases, these dominant losses increase and the total converter power loss is also increased. It is important to note that for mass production purposes the inductor losses can be further reduced through optimal material design. However, due to the prototype nature of the circuit an off-the-shelf solution had to be applied. Moreover, the reverse recovery losses of all the diodes are ignored, since the reverse recovery current is limited by the leakage inductance of the coupled inductor. Fig. 11 shows the photograph of the 250 W experimental prototype of the

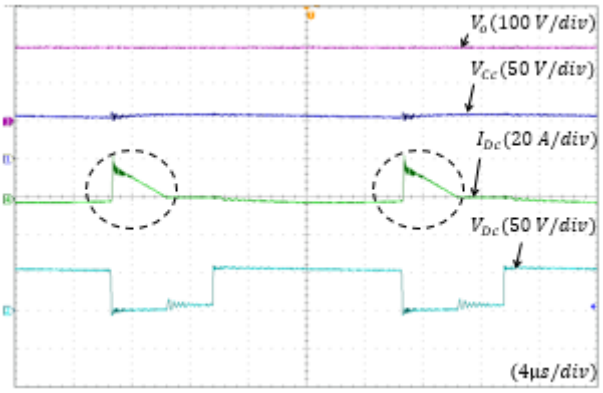
proposed converter.



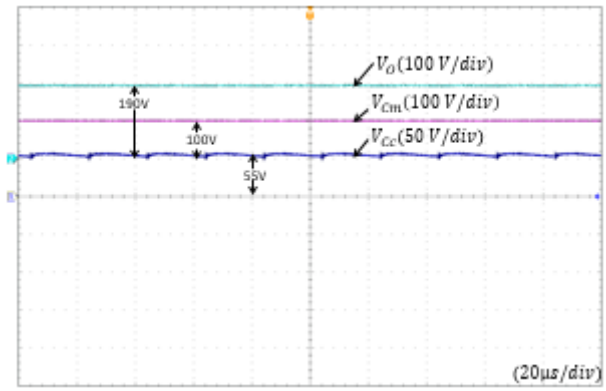
(a)



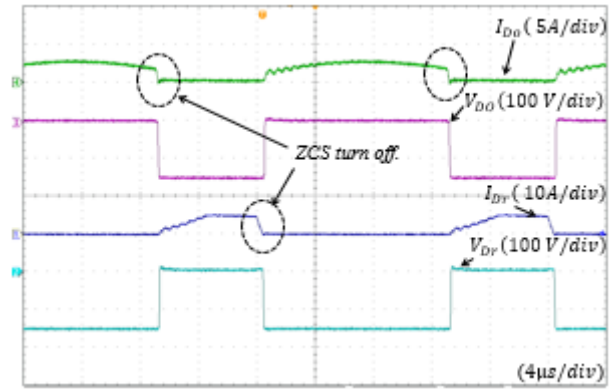
(b)



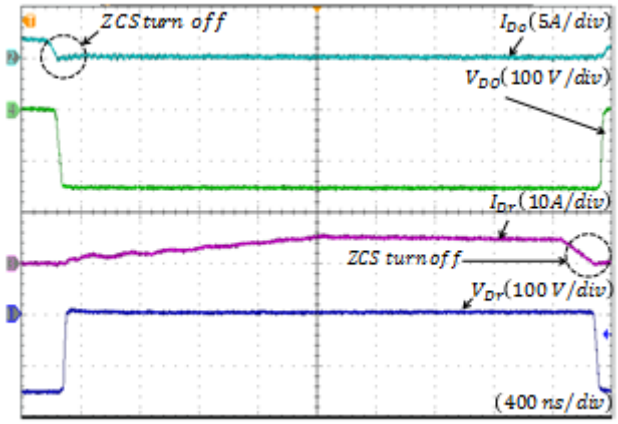
(c)



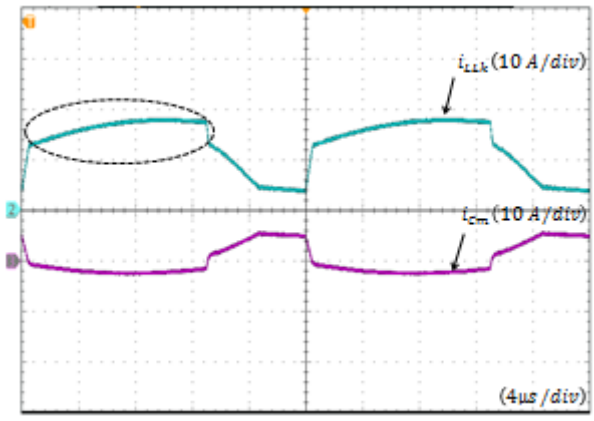
(d)



(e)



(f)



(g)

Fig. 8. *Experimental results*

a) Switch and clamp diode waveforms
b) ZCS details of the main switch
c) Passive clamp circuit performance
d) Capacitors voltage stress
e) Diodes ZCS turn off and reverse recovery alleviation
f) ZCS turn-off details of the diodes
g) Leakage inductor current waveform

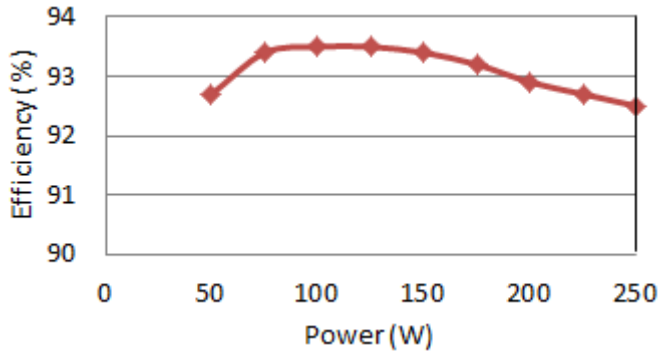


Fig. 9. *Measured efficiency at different loads*

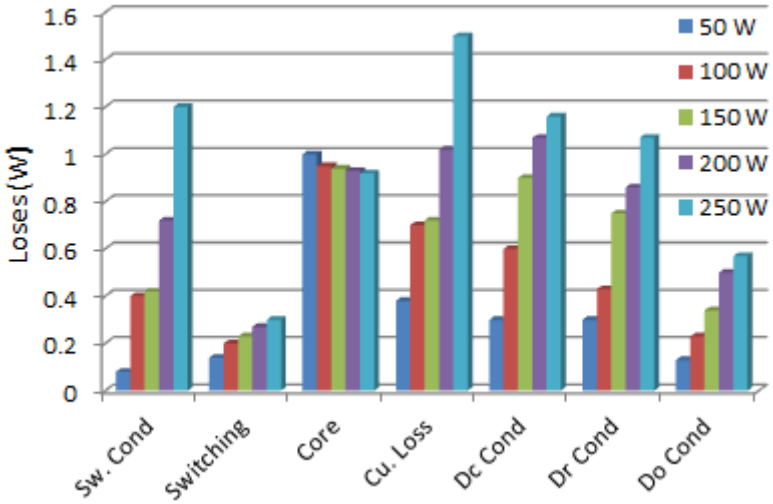


Fig. 10. *Loss breakdown under different load*

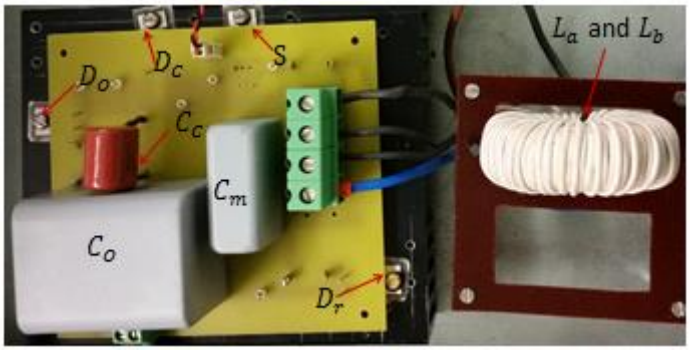


Fig. 11. *Photograph of the experimental prototype*

6. Conclusion

In this paper a new single phase, high gain, boost converter with coupled inductor and switched capacitor is proposed. Thorough theoretical analysis of the circuit's principle of operation and experimental results presented from a 250 W prototype demonstrate the effectiveness of the proposed topology as a non-isolated, high gain, step-up power converter.

The key advantages of the proposed converter are: i) The voltage gain is easily enlarged by selecting the turns ratio of the coupled inductor. ii) The semiconductor switch voltage stress is reduced; hence lower voltage rated devices can potentially be adopted to reduce conduction losses. iii) ZCS soft switching performance is readily achieved for the main switch and ZCS is achieved for the diodes - further reducing losses in the circuit and minimizing reverse recovery loss. iv) The leakage energy of the coupled inductor is recycled to the output.

References

[1] Watson, R., Lee F.C., and Hua G.C.: 'Utilization of an active-clamp circuit to achieve soft switching in flyback converters', IEEE Trans. Power Electron., 1996, 11, (1), pp. 162-169.

[2] Erickson R. W. and Maskimovic D.: 'Fundamentals of Power Electronics'. USA: Springer, 2000.

[3] Axelrod B., Berkovich Y., and Ioinovici A.: 'Switched- Capacitor/Switched-Inductor Structures for getting Transformerless Hybrid DC-DC PWM Converters', IEEE Trans. Circuit and Sys, 2008, 55, (2), pp. 687-696.

[4] Prudente M., Pfitscher L.L, Gustavo E., and Gules R.: 'Voltage Multiplier Cells Applied to Non-Isolated DC-DC Converters', IEEE Trans. Power Electrons, 2008, 23, (2), pp. 871-887.

[5] Zhou L. W., Zhu B. X. and Luo Q. M.: 'High step-up converter with capacity of multiple input', IET Power Electron., 2012, **5**, (5), pp. 524-531.

[6] Changchien S. K., Liang T. J., Chen J. F and Yang L. S.: 'Step-up DC-DC converter by coupled inductor and voltage lift technique', IET Power Electron., 2010, **3**, (3), pp. 131-142.

[7] Qun, Z. and Lee F.C.: 'High-efficiency, high step-up DC-DC converters'. IEEE Trans. Power Electron., 2003, 18, **(**1), pp. 65-73.

[8] Li W., Li W., He X., Lambert S. and Pickert V.: 'Performance analysis of ZVT interleaved high step-up converter with built-in transformer', In: 5th IET International Conference on Power Electronics, Machines and Drives, Brighton, UK, April 2010, pp. 1-6.

[9] Oliveira S. V. G. and Barbi I.: 'A three-phase step-up dc-dc converter with a three-phase high-frequency transformer for dc renewable power source applications', IEEE Trans. Ind. Electron., 2011, 58, (8), pp. 3567–3580.

[10] Zhangyong Chen; Jianping Xu,: 'High boost ratio DC-DC converter with ripple-free input current', Electronics Letters , 2014, 50, (5), pp.353,355.

[11] Yi Z, Li W, Deng Y., He X.: 'High step-up boost converter with passive lossless clamp circuit for non-isolated high step-up applications', IET Power Electron., 2011, **4**, (8), pp. 851- 859.

[12] Yi Z, Li W, He X., Yao Z, Hao M.: 'Performance Analysis of High Conversion Raito Converter with Switched Capacitor and Voltage Gain Extension Cell', in 37th Annual Conference on IEEE Industrial Electronics Society IECON, Melbourne. Australia, November 2011, pp 1-6.

[13] Hsieh Y., Chen J., Liang T. and Yang L.: 'Novel high-step up dc-dc converter with coupled inductor and switched-capacitor techniques', IEEE Trans. Ind. Electron., 2012, 59, (2), pp. 998–1007.

[14] Muhammad, M., Armstrong M., and Elgendy M.A.: 'Non-isolated, high gain, boost converter for power electronic applications', In: 8th IET International Conference on Power Electronics, Machines and Drives, Glagow, UK, April 2016, pp. 1-6.

[15] Berkovich Y., and Axelrod B.: 'Switched-coupled inductor cell for DC-DC converters with very large conversion ratio', IET Power Electron., 2011, 4, (3), pp. 309-315.

[16] Liu H., Hu H., Wu H., Xing Y. and Batarseh I.: 'Overview of High step-up Coupled-Inductor Boost Converter', Emerg. and select. Topics in Power Electron. IEEE Journal of , 2016, 4, (2), pp. 689-704.

[17] Gu, B.; Dominic, J.; Lai, J. S., Zhao Z., Liu, C.: 'Hybrid Transformer ZVS/ZCS DC–DC Converter With Optimized Magnetics and Improved Power Devices Utilization for Photovoltaic Module Applications', , IEEE Trans. Power Electron., 2015, 30, (4), pp.2127,2136.

[18] Schelecht M. F., Casey L. F.: 'Comparison of the square-wave and quasi-resonant topologies', IEEE Trans. Power Electron., 1988, 3, (1), pp. 83-92.