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Analysis and Implementation of High-Performance DC-DC Step-Up Converter for Multilevel Boost Structure

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The conventional DC-DC converters such as SEPIC, boost converter, etc. produces large voltage ripples in multilevel converter systems. For that reason, in this paper, a new DC-DC converter topology is proposed, and the performance is analyzed. Since the proposed converter delivers high conversion efficiency, it can be selected for multilevel boost DC-DC converters. The adverse effects such as inductor resistance and inductor size of the conventional converters are overcome by the proposed converter. The output voltage ripples are reduced in the proposed converter, i.e., the spikes in the converter output voltage are almost zero. The theoretical analysis is presented in this paper, which speaks about the advantage of the proposed converter. The converter operation is analyzed and discussed in continuous conduction mode (CCM). The voltage gain of the proposed converter is higher than the conventional boost converter. To validate the performance of the proposed converter, an experimental prototype is fabricated and tested in the laboratory. The performance of the converter is compared with the conventional boost and SEPIC converter. The experimental result confirms the theoretical analysis. The proposed converter can be extended by connecting more number of voltage multiplier (VM) cells to get the desired multilevel output voltage.

Keywords: boost, CCM, multilevel boost, voltage gain, voltage multiplier, voltage ripple

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INTRODUCTION

The conventional boost dc-dc converter has several issues such as power loss, the voltage drop across various devices, and the effects due to the inductor resistance when it tries to achieve the required voltage gain. The quality of operation and the conversion efficiency is affected by the high duty cycle of the semiconductor switch (Premkumar et al., 2018a; Premkumar and Sumithira, 2019a). These problems are solved by introducing the new converters such as Zeta, SEPIC, and Cuk converters (Banaei and Bonab, 2016). The various converters are reported in Amir et al. (2019), and these converters are differentiated based on the switching methods (switching between the capacitor and inductor), and boosting techniques such as voltage multiplier (VM), voltage doubler, cascade connections, etc (Chen et al., 2018; Pop-Calimanu et al., 2019). Each of the converters has its drawbacks, and these drawbacks motivate the researchers to work on the new converters for the multilevel boost structure. For instance, the multilevel converters with conventional boost, Cuk, and SEPIC have output voltage ripples (Babaei et al., 2013; Selwan et al., 2015; Premkumar et al., 2018b).

The conventional buck-boost and boost converters are frequently preferred in solar photovoltaic systems, and fuel-based energy systems (Divakar et al., 2008; Kaouane et al., 2015; Premkumar et al., 2018b; Rosas-Caro et al., 2018a,b; Premkumar and Sumithira, 2019b). The authors in Kaouane et al. (2015) and Premkumar and Sumithira (2019b) reported converters with two MOSFET switches and hybrid boost, respectively, for solar photovoltaic (PV) systems to improve the output voltage gain along with the proper tracking technique. The quadratic buck-boost converter was reported by Rosas-Caro et al. (2018b) with the conversion output voltage and continuous input current with positive polarity.

The authors in Divakar et al. (2008) reported soft switching techniques such as zero voltage switching and zero-current switching to decrease the switching losses in the traditional boost converter. The authors in Hegazy et al. (2012) and Rosas-Caro et al. (2018a) reported the converters with the interleaved structure to achieve the required output voltage with the continuous input current. However, the interleaved structure is complicated when compared to the conventional boost converter. Besides, the author in Zeng et al. (2019) reported that the interleaved structure also helps to increase the conversion efficiency, and reduce the output voltage ripple. When the conventional interleave based boost or buck-boost converters are chosen for multi-level boost converters, it introduces a heavy spike in inductor current and the output voltage. The same can be observed from the experimental waveforms of the literature reported in Rosas-Caro et al. (2018a) and Hegazy et al. (2012).

The SEPIC converter is one of the conventional dc-dc converter derived from the traditional boost converter. Related to conventional boost converter and Cuk converter, the SEPIC converter has few ripples in the output current since the second inductor in the SEPIC converter smooths the current spikes. The SEPIC converter can be preferred in different applications such as PV system, fuel cell-based systems, and also multi-port converters (Saravanan and Babu, 2015; Buticchi et al., 2019). As a result, the SEPIC converter can be used for most of the renewable energy systems. Though the SEPIC converter voltage gain is less, and it can be used for step-up applications (Kircioglu et al., 2016; Shamshuddin et al., 2017; Premkumar et al., 2018c; Natarajan et al., 2019; Yousri et al., 2019). The voltage gain of the SEPIC converter is less than the conventional boost converter per duty ratio. The voltage gain of the SEPIC converter and boost converter is equal to D/(1-D), and 1/(1-D), respectively (Park et al., 2010; Ansari and Moghani, 2019). If the structure of the SEPIC converter is slightly modified, it may step-up voltage than the conventional boost converter. Therefore, in this paper, a modified structure for the SEPIC converter with high-quality output is discussed and examined.

A new structure is proposed for the SEPIC converter is proposed in this paper, and the converter is based on the traditional SEPIC converter. The major highlight of the proposed SEPIC converter is not having an extra parasitic element compared to the traditional SEPIC converter. A new structure is derived in a way such that a reduction in output voltage ripple and an increase in conversion efficiency. Moreover, the voltage gain is equal as the traditional boost dc-dc converter and higher than the conventional SEPIC converter with less effect of the inductor resistance. Another notable highlight of the proposed converter is its spike-free voltage and current waveforms. The efficiency of the converter is >95% when the duty ratio of the switch is <60%, >92% when the duty cycle of the switch is between 60 and 80%, and this advantage makes the converter a decent choice for the multi-level boost structure powered by the PV modules and fuel cells. The converter can also be extended to achieve high voltage gain by using elements such as inductors, diodes, and capacitors. The structure of the paper is as follows. Section Operation of the Proposed SEPIC Converter for Multi-Level Structure presents the operation of the proposed converter. The steady-state analysis under continues conduction mode (CCM) is performed in section Steady-State Analysis and Converter Comparison. The experimental results and further discussion are given in section Results and Further Discussions. The paper is concluded in section Conclusion.

OPERATION OF THE PROPOSED SEPIC CONVERTER FOR MULTI-LEVEL STRUCTURE

The converter proposed in this paper has high-quality output and high gain by making a small modification in the conventional SEPIC converter, as shown in **Figure 1**. In the proposed converter, the charging capacitor is changed its position, and the gain equation is altered accordingly. The proposed converter comprises one MOSFET switch, two capacitors such as the coupling capacitor (C_s), and the output capacitor (C_{out}), two inductors, namely L_1 and L_2, and one diode. For simplified analysis, the converter operation in CCM is divided into two modes of operation. Theoretical waveform is depicted in **Figure 2**.

The following are the assumptions made to streamline the converter examination.

- The various apparatuses of the converter are ideal. The forward drops of the switch and diode, on-state resistance

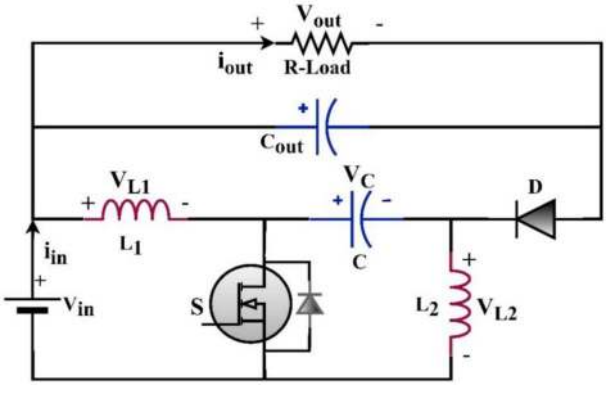

FIGURE 1 | Schematic of the proposed converter.

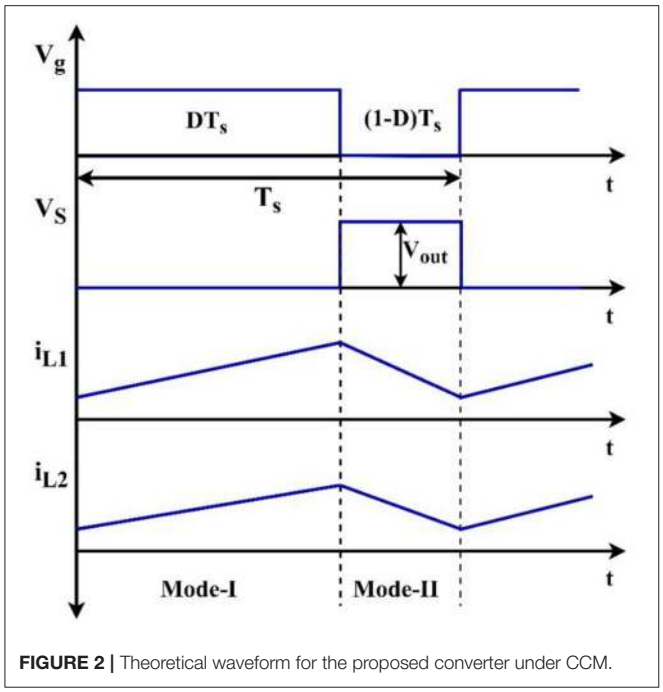

FIGURE 2 | Theoretical waveform for the proposed converter under CCM.

(R_{ds-ON}) of the MOSFET switch, the equivalent series resistance of the inductors, and capacitor are ignored.

- The capacitance values of the capacitors C_s and C_{out} are considered as high. Thus, the capacitor voltage is supposed to be constant during one switching cycle.

Mode-I

The current flow is depicted in **Figure 3A**. The analysis of the proposed converter is made by assuming the ideal components, and the converter is operated at CCM.

During this mode, the MOSFET switch is turned on by applying the pulse-width-modulated (PWM) signal to the gate terminal of the switch. When the switch is turned on, the current starts to flows the components such as C, L_1, and L_2. In **Figure 3**, the inductor currents are represented as i_{L1}, and i_{L2}, and the voltage across the coupling capacitor is represented by V_c. During mode-I, the diode is turned off due to the reverse voltage. There are three loops for energizing the storage components. The voltage across the inductor-1 (V_{L1}) is equal to the input source voltage (V_{in}) which rises the current in L_1. The source voltage also delivers the energy to the L_2 and the coupling capacitor (C) through the load. It is observed that the second and third loop is formed by the source voltage, C, and L_2. The voltage across the diode is equal to the voltage across the capacitor. The voltage across the inductor L_1 is presented in Equation (1), and other expressions are written as follows.

$$V_{L_1} = V_{in} = L_1 \frac{di_{L_1}}{dt} \tag{1}$$

$$V_c + V_{in} = L_2 \frac{di_{L_2}}{dt} + V_d + V_{out} \tag{2}$$

$$i_C = C \frac{dV_C}{dt} = i_{L_2} \tag{3}$$

$$i_{C_{out}} = C_{out} \frac{dV_{C_{out}}}{dt} = \frac{V_{out}}{R} - i_{L_2} \tag{4}$$

Mode-II

The current flow during this mode is depicted in **Figure 3B**. During this mode, the MOSFET switch is turned off. Due to this, there are two loops in the converter operation. The coupling capacitor is energized through the inductors L_1 and L_2. Both the inductors start to release the energy during this mode. The inductor L_2 also discharges, and the output capacitor delivers the load current. The voltage stress of the MOSFET switch is equal to the difference between the voltage across the inductor L_1, and the source voltage. Various output equations during mode-II are presented as follows.

$$V_{in} = L_1 \frac{di_{L_1}}{dt} + V_c + L_2 \frac{di_{L_2}}{dt} \tag{5}$$

$$L_2 \frac{di_{L_2}}{dt} = V_{in} - V_{out} \tag{6}$$

$$i_C = C \frac{dV_C}{dt} = i_{L_1} \tag{7}$$

$$i_{C_{out}} = C_{out} \frac{dV_{C_{out}}}{dt} = \frac{V_{out}}{R} - i_{L_2} \tag{8}$$

STEADY-STATE ANALYSIS AND CONVERTER COMPARISON

The steady-state analysis of the proposed converter is presented under the CCM operation. The voltage conversion of the proposed converter is the most significant parameter, and the same can be obtained from the above-two operating modes of the converter. The energy balance in the proposed converter is achieved by the charging and discharging cycle of the inductors L_1 and L_2. The average voltage of the inductors over one switching cycle is zero. The average voltage of the inductor is derived from the above-said equations. The average voltage equation is presented in Equations (9, 10).

$$DV_{in} + (1-D)(V_{in} - V_C) = 0 \tag{9}$$

$$D(V_{in} + V_C + V_{out}) + (1-D)(V_{in} - V_{out}) = 0 \tag{10}$$

From Equations (9, 10), the voltage across the capacitor, and the voltage gain of the converter being stated in Equations (11, 12).

$$V_C = \frac{1}{1-D} V_{in} \tag{11}$$

$$M = \frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{12}$$

As seen in Equation (12), the voltage gain of the proposed converter is similar to the traditional boost converter. Therefore, the proposed converter can be compared with conventional SEPIC and Cuk converters. The converters can be analyzed based on the current stress and voltage stress on the MOSFET switch under DCM and CCM operation, voltage gain, and the minimum inductance requirements. **Table 1** shows the essential parameters of the converter and the other conventional converters.

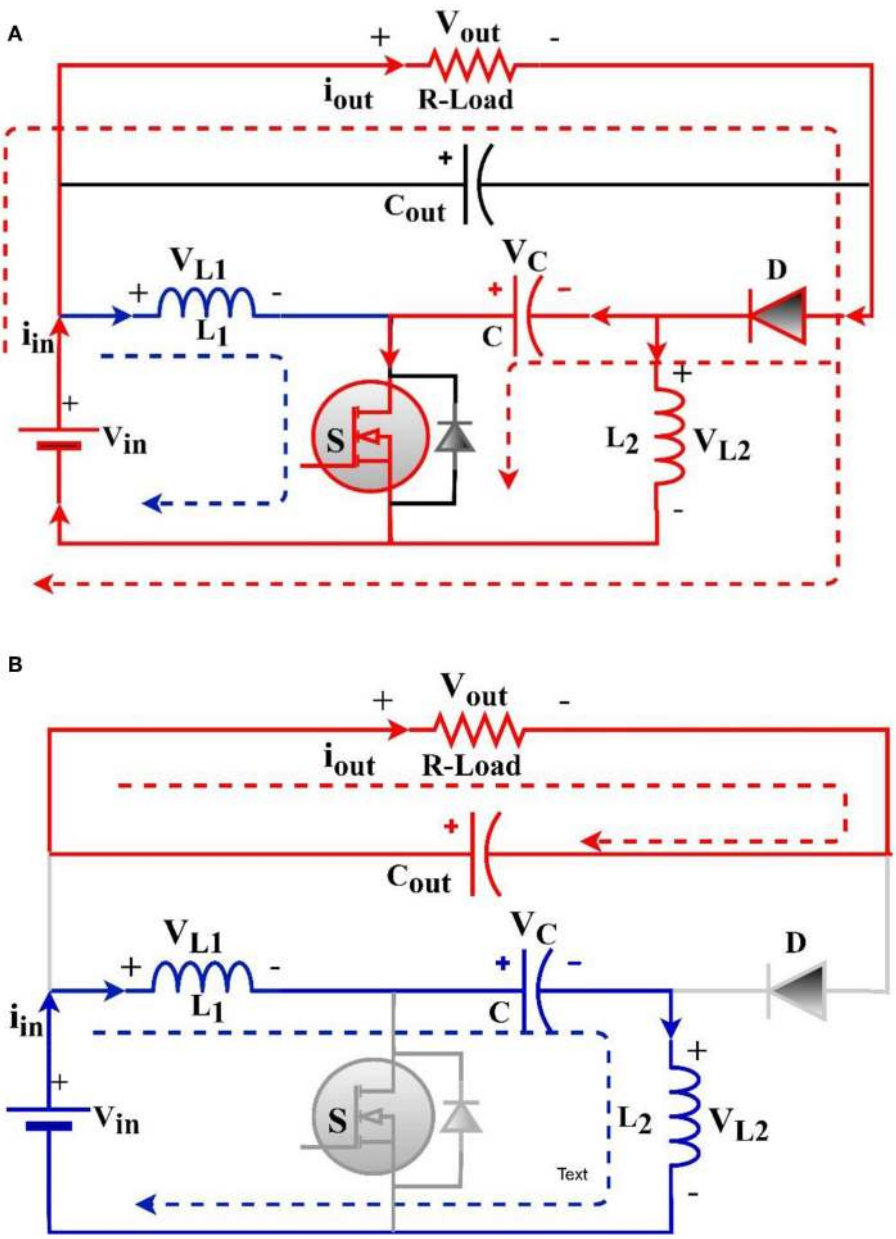

FIGURE 3 | Modes of operation; **(A)** Mode-I; **(B)** Mode-II.

The voltage stress on the MOSFET switch and the diode is obtained based on the modes of operation. The voltage stress on the diode is presented in Equation (13).

$$V_d = -V_C = -\frac{1}{1-D}V_{in} \tag{13}$$

During mode-II, the MOSFET switch is turned off. Thus, the voltage stress on the MOSFET switch is presented in Equation (14).

$$V_s = V_{in} - V_{L_1} = V_C = \frac{1}{1-D}V_{in} \tag{14}$$

The energy balance is obtained between the input and the output by the inductor elements. Based on the volt-second balance equation, the current through the inductors i_{L1} and i_{L2} are calculated as follows, and further, the current stress on the MOSFET switch is obtained.

$$V_{in}(i_{L_1} - i_{L_2}) = V_{out}I_{out} \tag{15}$$

From Equation (15), the current through the inductors are obtained as follows.

$$i_{L_1} = \frac{D}{1-D}i_{out} \tag{16}$$

$$i_{L_2} = i_{out} = \frac{V_{out}}{R} \tag{17}$$

Based on the above-said equations, the current stress on the diode and the MOSFET switch is obtained as follows.

$$i_d = i_{out} = \frac{V_{out}}{R} \tag{18}$$

$$i_s = \frac{D}{1-D} i_{out} \tag{19}$$

The inductor current oscillates between the minimum and maximum value depends on the inductance, and it is considered as the essential element in the converter design. Thus, the current ripple of the inductor and its respective inductance is calculated by considering the operating stages of the converter. The peak-peak ripple current over one switching period is calculated as follows.

$$\Delta i_{L_1} = \frac{DT_s}{L_1} V_{in} \tag{20}$$

$$\Delta i_{L_2} = \frac{DT_s}{L_2} V_{in} \tag{21}$$

The values of the inductances decide the boundary between DCM and CCM operation of the proposed converter. By assuming the minimum inductor current ($I_{L,min}$) is zero,

TABLE 1 | Assessment of the proposed modified SEPIC converter with the traditional converters.

Parameters	SEPIC converter	Cuk converter	Boost converter	Proposed modified SEPIC converter
M	$\frac{D}{1-D}$	$-\frac{D}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$
$L_{1,min}$	$\frac{(1-D)^2R}{2F_sD}$	$\frac{(1-D)^2R}{2F_sD}$	$\frac{D(1-D)^2R}{2F_s}$	$\frac{(1-D)^2R}{2F_s}$
$L_{2,min}$	$\frac{(1-D)R}{2F_s}$	$\frac{(1-D)R}{2F_s}$	-	$\frac{D(1-D)R}{2F_s}$
$\frac{\Delta V_{out}}{V_{out}}$	$\frac{D}{RC_{out}F_s}$	$\frac{(1-D)}{8L_2C_{out}F_s^2}$	$\frac{D}{RC_{out}F_s}$	$\frac{D(1-D)}{RC_{out}F_s}$

TABLE 2 | Specifications of the proposed SEPIC converter and other converters.

Parameters	Values		
	SEPIC converter	Cuk converter	Proposed converter
Input voltage, V_{in}	20 V	20 V	20 V
Inductors, L_1, L_2	1.4 mH	1.4 mH	1.4 mH
Coupling capacitor, C	10 μF	10 μF	10 μF
Output capacitor, C_{out}	220 μF	220 μF	220 μF
Load resistance, R	85 Ω	85 Ω	85 Ω
Switching frequency, F_s	20 kHz	20 kHz	20 kHz

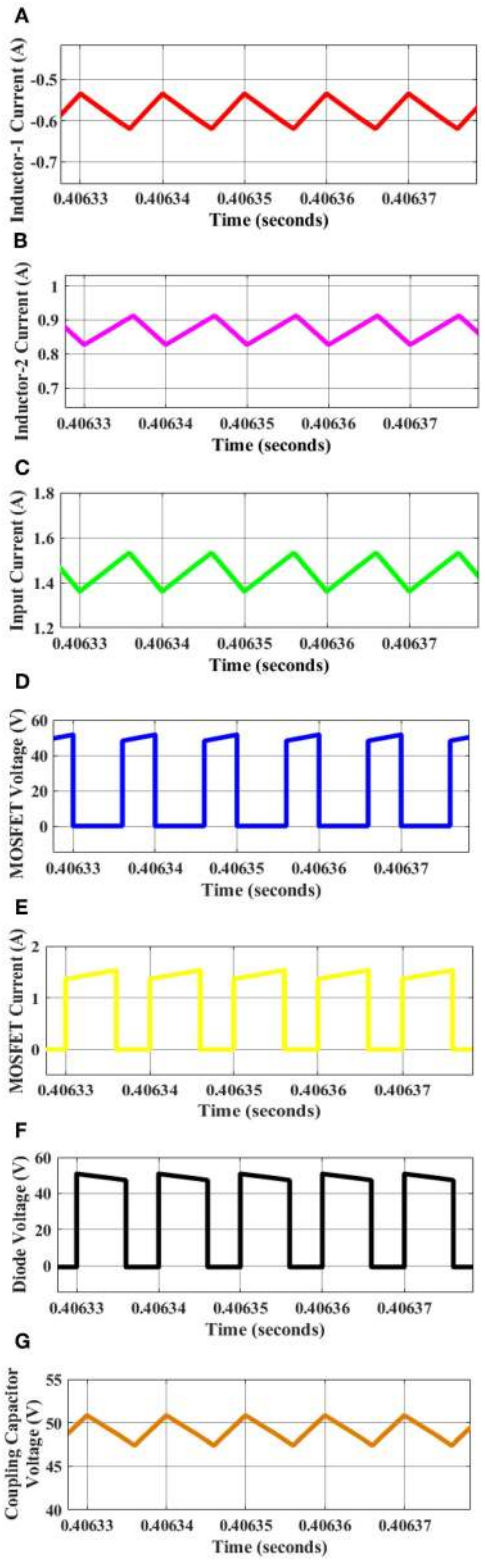

FIGURE 4 | Various simulation waveforms of the proposed converter; **(A)** Inductor current, i_{L1}, **(B)** Inductor current, i_{L2}, **(C)** Input current, I_{in}, **(D)** Voltage stress of the MOSFET, **(E)** Current stress of the MOSFET, **(F)** Voltage stress of the diode, **(G)** Voltage across coupling capacitor.

the minimum inductance of the inductors is calculated as follows.

$$I_{L,\min} = I_L - \frac{\Delta I_L}{2} \tag{22}$$

$$L_{1,\min} = \frac{(1-D)^2 R}{2F_s} \tag{23}$$

$$L_{2,\min} = \frac{D(1-D)R}{2F_s} \tag{24}$$

Where ΔI_L is the current ripples of both the inductors, and it is given by $(DT_s/L)V_s$. The peak-peak output voltage ripples of the proposed converter can be obtained by the differential equations. Since the proposed converter has two capacitors, the output voltage can be written as follows.

$$\frac{\Delta V_C}{V_c} = \frac{RC}{D} F_s \tag{25}$$

$$\Delta V_{C_{out}} = \Delta V_{out} \tag{26}$$

$$\frac{\Delta V_{out}}{V_{out}} = \frac{D(1-D)}{RC_{out}F_s} \tag{27}$$

RESULTS AND FURTHER DISCUSSIONS

The proposed converter, and the traditional converters such as SEPIC converter, and Cuk converters are simulated using MATLAB/Simulink software. To check the effectiveness of the proposed modified SEPIC converter, an experimental prototype is made, and the same is tested in the laboratory. The storage elements such as L_1, L_2, C, and C_{out} are selected as per the previous discussions. The inductors are chosen based on Equations (23, 24) by considering the CCM operation of the converter. Various parameters of the proposed modified SEPIC converter for both the simulation and experimental study are presented in **Table 2**. The simulation parameters of the SEPIC converter and Cuk converter, also listed in **Table 2**.

Simulation Study

As per the values presented in **Table 2**, the converters are designed and simulated using MATLAB/Simulink software. To check the performance of the proposed converter, the traditional converters such as Cuk and SEPIC converter also simulated. For the simplified analysis, the output voltage of the Cuk converter is assumed as a positive voltage; however, the actual output voltage of the Cuk converter is negative. First, the proposed converter is simulated with the duty cycle (D) of 0.6, and the results were depicted in **Figure 4**.

As seen in **Figure 4**, the proposed converter is operated at CCM operation. As shown in **Figures 4A,B**, the inductor currents (i_{L1} and i_{L2}) is oscillating between −0.55 A to −0.62 A, and 0.83 A to 0.91 A, respectively. This result proves that the proposed converter is operated under CCM operation. Another significant advantage of the proposed converter is continuous (constant) input current, and the same can be observed in **Figure 4C**. The input current is oscillating between 1.38 A and 1.52 A. Thus, the input ripple current of the proposed converter is observed as 0.14 A, which is less than the conventional SEPIC converter, and Cuk converter. **Figures 4D,E** shows the voltage and current stress of the MOSFET, respectively. The maximum voltage stress of the MOSFET switch is observed as 49.5 V, and the current stress is found as 1.5 A. **Figure 4F** depicts the voltage stress of the diode, and it is equal to the voltage across the coupling capacitor. **Figure 4G** illustrates the voltage across the capacitor, and the average voltage is observed as 49 V. Therefore, the diode voltage stress is equal to 49 V as shown in **Figure 4F**. As per the previous discussion, the proposed converter, and

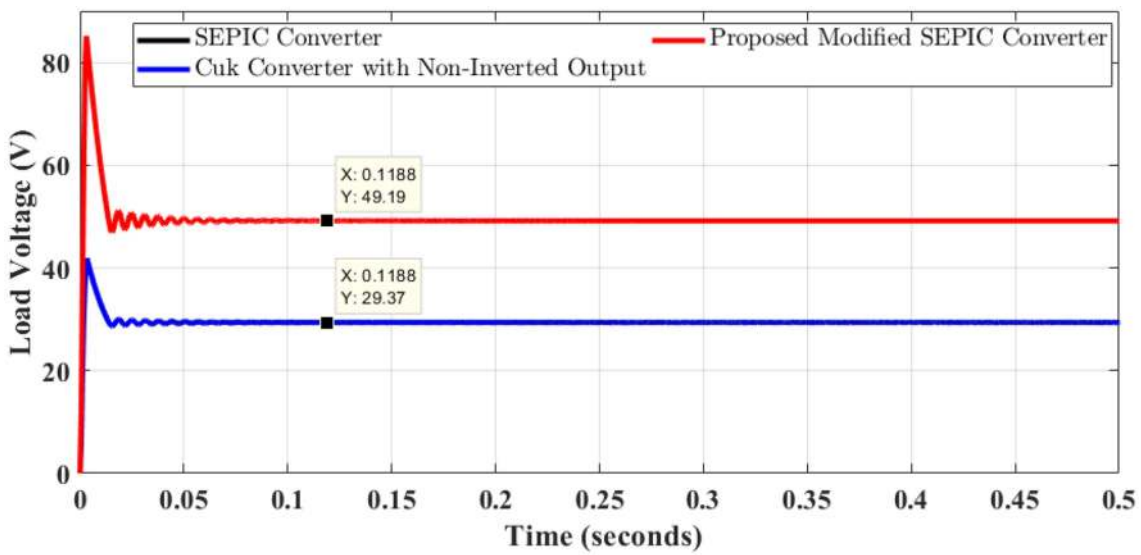

FIGURE 5 | Load output voltage waveform of all the converters at D = 0.6.

other traditional converters such as SEPIC converter, and Cuk converter also simulated for the duty cycle at 0.6. The load output voltage waveform of all the converters are depicted in **Figure 5**.

The load resistance of all the converter is kept constant at 85 Ω, and the output voltage of the SEPIC converter and Cuk converter is observed as 29.37 V (Cuk converter output voltage is assumed as positive). Whereas, the output load voltage of the proposed modified SEPIC converter is 49.19 V, which is 0.7 times higher than the conventional SEPIC converter. It is also observed that the settling time of all the converters is almost similar. It is concluded that the converter proposed in this paper is having more voltage gain than the traditional SEPIC converter with the same number of components. This high voltage gain is possible only by changing the connections of the conventional SEPIC converter, but not by increasing/decreasing the storage elements or switching devices. The proposed converter is also simulated for different duty cycles, such as 0.4, 0.5, 0.6, and 0.7. The converter switch duty is changed after 0.5 s, duration each. The output load voltage waveform is shown in **Figure 6**.

At the start, all the converters are operated with D=0.4, the output voltage of the SEPIC, Cuk, and proposed converter was observed as 13.57 V, 13.57 V, and 32.51 V, respectively. At t = 0.5 s, the duty cycle is changed to D = 0.5, and the output voltage is witnessed as 19.18 V, 19.18 V, and 39.17 V, respectively. At t = 1 s, the duty cycle is changed to D = 0.6, and the output voltage is observed as 29.38 V, 29.38 V, and 49.16 V, respectively. At t = 1.5 s, the duty cycle is changed to D = 0.7, and the output voltage is observed as 46.35 V, 46.35 V, and 65.72 V, respectively. It is observed and concluded that the duty up to D = 0.5, the SEPIC converter, and the Cuk converter acts as a buck converter, and after D = 0.5, the traditional converters act as a boost converter. Whereas, the proposed converter acts as the boost converter

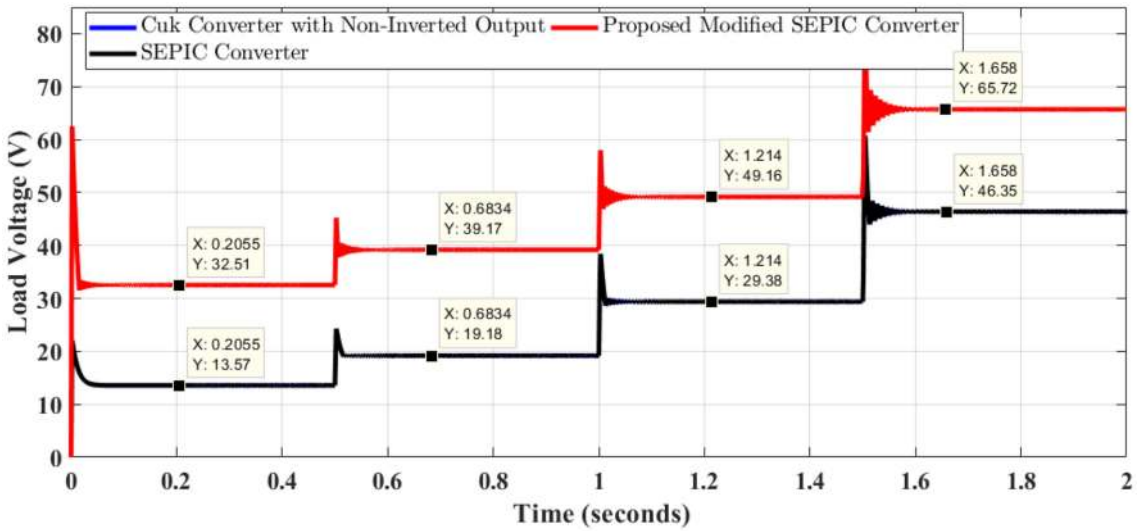

FIGURE 6 | Load output voltage waveform of all the converters at a various duty cycle.

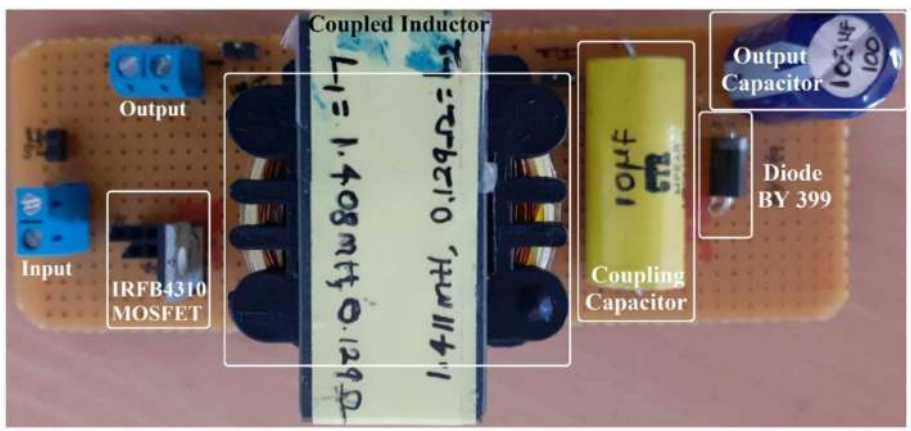

FIGURE 7 | Experimental prototype of the proposed converter.

irrespective of the duty cycle as similar to a conventional boost converter with constant input current capability.

Experimental Study

The experimental prototype of the converter is developed and verified in the laboratory environment as per the parameters are shown in **Table 2**. The experimental prototype is shown in **Figure 7**. Two inductors of the converter are selected as coupled inductors with EE33 ferrite core. Two strings of twisted copper wire (21 SWG) are wounded on the ferrite core to design the required value of inductance, and twisted pair can minimize the skin effect and coil resistance. The polypropylene metalized film capacitor is selected for a coupling capacitor, which has low ESR ($\approx$ 12.2 mΩ). A low on-state resistance N-Channel MOSFET switch is required for the converter operation, so IRFB4310 MOSFET is selected, which has 5.6 mΩ on-state resistance, and it can withstand up to 100 V, 140 A.

The converter requires a fast-acting diode to direct the current. Therefore, BY399 fast recovery diode is selected which has less forward voltage drop (<1.1 V) with less reverse recovery time (<500 ns). The PWM pulse is generated using the MSP430FR2355 Texas Instrument development board. A 20 kHz

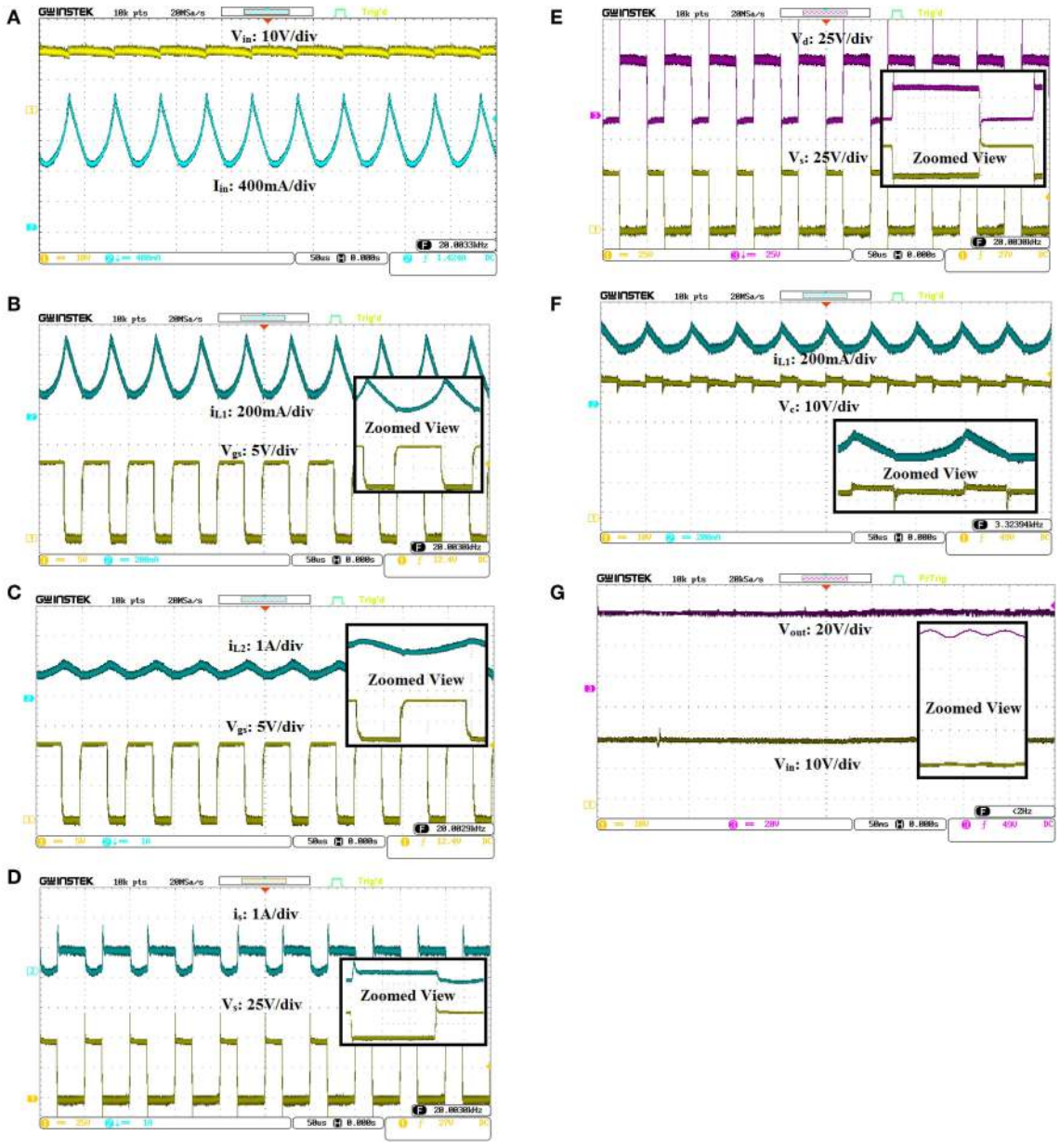

FIGURE 8 | Experimental waveforms of the converter for 60% duty cycle. **(A)** Input voltage, V_{in} and input current, I_{in}; **(B)** inductor current, i_{L1} and gate-source voltage, V_{gs}; **(C)** inductor current, i_{L2} and gate-source voltage, V_{gs}; **(D)** MOSFET current stress, is and MOSFET voltage stress, V_s; **(E)** MOSFET voltage stress, V_s and diode voltage stress, V_d; **(F)** Inductor current, i_{L1} and voltage across the capacitor, V_c, **(G)** Input voltage, V_i and output voltage, V_{out}.

PWM pulse with a 60% duty cycle is given to the MOSFET driver through the optoisolator. The MOSFET switch is driven with 4N25 optoisolator and IR2113 MOSFET driver. The proposed converter prototype is made for 50 W. The proposed converter rating can be extended using multiplier cell circuits if necessary. The adoption of the multiplier circuit is not discussed in this paper. The experimental waveforms are depicted in **Figure 8**.

Constant input current is one of the key objectives of this paper, and the same can be seen in **Figure 8A**. The input current at full load is 1.424 A (average). The input current oscillates between 0.9 A and 1.72 A, and it never reaches zero. The inductor currents such as i_{L1} and i_{L2} are depicted in **Figures 8B,C**, respectively. It is observed from **Figures 8B,C**, the converter is operated under CCM operation. The peak-peak inductor ripple current as per Equations 20, 21 is selected as 0.43 A. From **Figure 8B**, the ripple current (Δi_{L_1}) is observed as 0.45 A (oscillation between 0.56 A−0.11 A), and from **Figure 8C**, the ripple current (Δi_{L_2}) is observed as 0.44 A (oscillation between 0.71 A−1.15 A). This result displays good agreement between the theoretical analysis and the experimental setup. The MOSFET voltage stress and diode can be observed in **Figures 8D,E**, respectively. As per Equations 13, 14, the maximum voltage

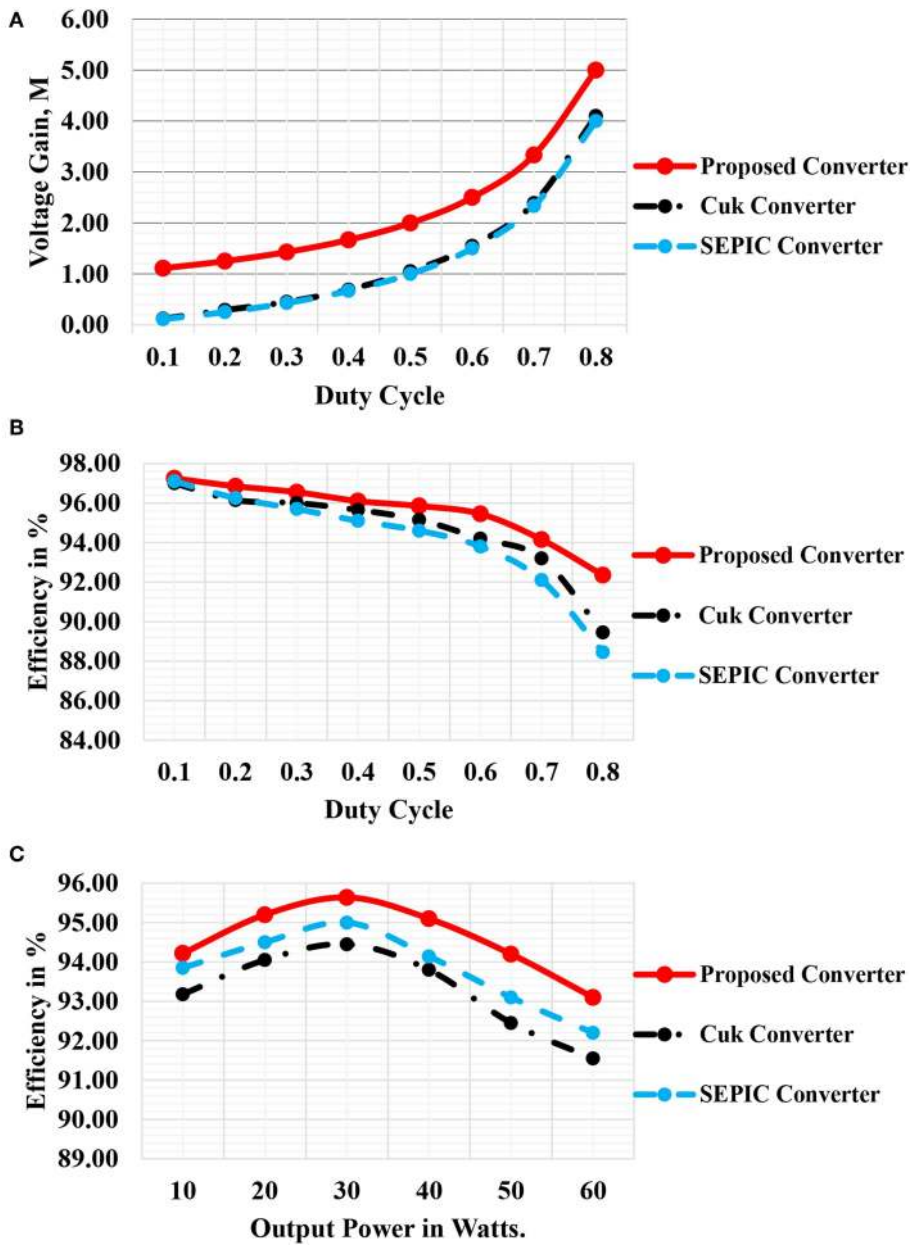

FIGURE 9 | Performance assessment of the proposed converter; **(A)** Voltage gain for several duty cycles, **(B)** Efficiency at various duty ratio, **(C)** Efficiency at different loading conditions.

stress of the MOSFET switch and the diode is equal to $\pm V_{out}$. Therefore, the voltage stress of the MOSFET and diode should be equal to 50 V when the duty cycle of the switch is 0.6. The same can be observed clearly in the waveforms as shown in **Figures 8D,E**. As per Equation 19, the current stress of the MOSFET switch is equal to 0.88 A. From **Figure 8D**, the current stress is observed as 0.84 A. As per Equation 11, the voltage across the coupling capacitor is equal to the output voltage of the converter which is equal to 50 V. The coupling capacitor voltage observed in **Figure 8F** is equal to 49 V. **Figure 8G** depicts the output voltage and the input voltage waveform. As per Equation 12, the output voltage of the converter for the duty cycle, D = 0.6, is equal to 50 V. The converter achieves 49 V experimentally, and this result displays good agreement between the theoretical analysis and the experimental setup. The difference in voltage ($\approx$ 1 V) can be ignored due to the voltage drop in other components. The proposed converter is compared with the other traditional converters in terms of voltage gain and efficiency. **Figure 9** shows the performance comparison of the proposed converter.

From the above discussions and the performance comparison presented in **Figure 9**, it is concluded that the proposed converter is superior in all aspects such as constant input current, high voltage gain, and high conversion efficiency without adding any extra components with the conventional SEPIC converter. The proposed converter is best suited for multi-level boost structure in solar photovoltaic systems or fuel-cell based energy systems instead of the traditional SEPIC converters. Finally, it is concluded that the proposed SEPIC converter can deliver the conversion efficiency at full load condition is equal to 94.2, and 95.64% maximum conversion efficiency.

CONCLUSION

The converter discussed in this paper improves the voltage conversion ratio than the other traditional dc-dc converters. The proposed SEPIC converter is analyzed in CCM operation, simulated, implemented, and compared with the traditional SEPIC, and Cuk converters. The analysis of various features such as inductor ripple current, voltage conversion, switch and diode voltage stress, and the converter efficiency is made for the proposed converter. The proposed converter is designed based on the theoretical discussions. The results obtained from the simulation, and experimentation is on par with the theoretical discussions. The conversion efficiency of the proposed converter is more than 92% for various duty cycle, and the maximum efficiency is equal to 95.64% at 30 W. This high conversion efficiency makes the proposed converter best suitable for the multilevel boost structure. The converter voltage gain can be further extended by adding the voltage multiplier circuits, and the same will be discussed and developed in future communications. The significant contribution in this paper is that the conventional SEPIC converter is extended without adding any additional equipment, and it behaves like a traditional boost converter with added features as following. (i) high voltage gain, (ii) high conversion efficiency, (iii) continuous input current, and (iv) less output voltage ripple.

DATA AVAILABILITY STATEMENT

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation, to any qualified researcher.

AUTHOR CONTRIBUTIONS

Research simulation, experimentation, analysis, revision, and overall layout formation were carried out by MP. Literature review, mathematical analysis, simulation, and proof-read was done by RS. Redesigning the hardware components, experimental testing, revised article, and final proof-read by CK.

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