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Analysis and Implementation of Multiphase Multilevel Hybrid Single Carrier Sinusoidal Modulation

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Abstract

This paper proposes a hybrid single carrier sinusoidal modulation suitable for multiphase multilevel inverters. Multiphase multilevel inverters are controlled by hybrid modulation to provide multiphase variable voltage and a variable frequency supply. The proposed modulation combines the benefits of fundamental frequency modulation and single carrier sinusoidal modulation (SC-SPWM) strategies. The main characteristics of hybrid modulation are a reduction in switching losses and improved harmonic performance. The proposed algorithm can be applied to cascaded multilevel inverter topologies. It has low computational complexity and it is suitable for hardware implementations. SC-SPWM and its base modulation design are implemented on a TMS320F2407 digital signal processor (DSP). A Complex Programmable Logic Device realizes the hybrid PWM algorithm and it is integrated with a DSP processor for hybrid SC-SPWM generation. The feasibility of this hybrid modulation is verified by spectral analysis, power loss analysis, simulation and experimental results.

Key Words: Digital signal processor, Hybrid modulation, Multiphase multilevel inverter, Power loss analysis, Single carrier sinusoidal modulation, weighted total harmonic distortion

I. INTRODUCTION

Multiphase machine drives have attracted considerable interest among researchers in recent years due to their inherent advantages. The major advantages of using a multiphase machine include improved reliability and increased fault tolerance, greater efficiency, higher torque density and reduced torque pulsations, lower per phase power handling requirements, enhanced modularity and improved noise characteristics [1]. Multilevel converter technology is based on the synthesis of voltage waveforms from several DC voltage levels. As the number of levels increases, the synthesized output voltage produces more steps and a waveform that approaches the reference more accurately. The major advantages of using multilevel inverters include high voltage capability with voltage limited devices, low harmonic distortion, reduced switching losses, increased efficiency, and good electromagnetic compatibility [2]. Various multilevel converter structures are reported in the literature. The cascaded multilevel inverter appears to be superior to other multilevel inverters in applications with a high power rating due to its modular nature of modulation as well as its control and protection requirements for each full bridge inverter [3].

The power circuit for the five-phase five-level cascaded inverter topology used to examine the proposed PWM technique is shown in fig.1. Modulation control of a multiphase multilevel inverter is quite challenging and much of the reported research is based on somewhat heuristic investigations [4], [5]. Most of the available works on PWM schemes for a multiphase voltage source inverter cover either carrier-based PWM or space vector PWM schemes.

A single carrier sinusoidal modulation strategy was proposed by Salam et al. [6] based on symmetric regular sampled unipolar PWM, with multiple modulating waveforms and a single carrier. The harmonic spectrum of this modulation is identical to the phase opposition disposition scheme for all major harmonics. M.S.A. Dahidah [7] used the concept of a single carrier modulation strategy to define a five level selective harmonic elimination PWM for a cascaded multilevel inverter.

Switching losses in high power high voltage converters pose a problem and any switching transitions that can be eliminated without compromising the harmonic content of the final waveform are considered advantageous [8]. This paper addresses a method to reduce the switching losses of a conventional single carrier sinusoidal PWM scheme with low computational overhead. The architecture for CPLD implementation with only logical elements is presented for adopting a hybrid PWM

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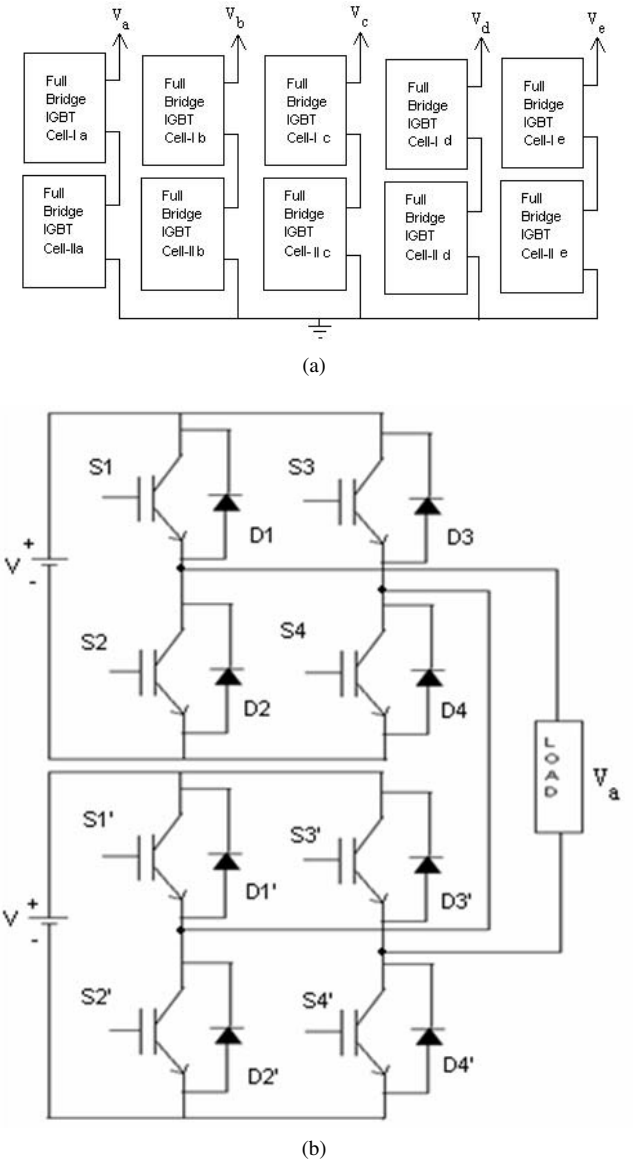


Fig. 1. (a) Schematic diagram of the five phase inverter topology used to verify the proposed five-level hybrid SC-SPWM technique (b) Power circuit configuration for one phase leg.

control algorithm. Although only a five phase five-level case is presented here, the proposed method can be applied to any number of phases, any number of voltage level and for any number of switching transitions.

This paper is organized in the following way. Section II describes the multiphase single carrier sinusoidal modulation and the development of hybrid modulation. Section III presents the harmonics and a power loss analysis of the multiphase multilevel inverter with the proposed modulation. Section IV illustrates the simulation and experimental results of the phase voltage and current waveforms including a discussion of the results. Finally, conclusions are presented in section V.

II. HYBRID PWM ALGORITHM DEVELOPMENT

A. Multiphase Single Carrier Sinusoidal Modulation

A five level single carrier sinusoidal PWM is the result of two sinusoidal modulating signals with a fundamental frequency of f_0, an amplitude of A_m, and one carrier signal. The carrier signal is a train of triangular waveforms with a frequency of f_c and amplitude of A_c. The number of full bridge inverter cells (K), depends on the number of levels (N) required, and can be defined as $K = (N-1)/2$. The N level single carrier sinusoidal modulation (SC-SPWM) needs K number of modulation signals per phase that have the same frequency of f_0, and an amplitude of A_m with a dc bias of A_c. The modulation index is defined as $M = \frac{A_m}{KA_c}$. The modulation frequency ratio m_f is given as $m_f = \frac{f_c}{f_0}$ p.u.

Fig.3(a) shows the modulation and carrier waveforms for a five-level SC-SPWM. The phase difference for other phase modulation signals are $360^\circ/n$, where n is number of phases. Intersection between the modulation signals and the carrier signal defines the switching instant of the PWM pulses.

In order to ensure quarter wave symmetry of the PWM output waveform, the starting point of the modulation signals ought to be phase shifted by one period of the carrier wave. The main advantage of SC-SPWM is its ability to define the location of the switching transitions that control or eliminate selected harmonics. This PWM technique is aimed at high power voltage source inverter systems in utility applications where the output frequency is fixed to the utility's grid frequency.

B. Proposed hybrid single carrier sinusoidal modulation

The principle behind this hybrid modulation is to mix fundamental frequency PWM and conventional SC-SPWM for each inverter module operation, so that the output contains the features of both. In this modulation technique, the four switches of each inverter module are operated at two different frequencies, two being commutated with fundamental frequency, while the other two switches are pulse width modulated with SC-SPWM. Unfortunately, this arrangement causes different switching losses and therefore differential heating among the switches. In order to overcome this problem, a sequential switching scheme is embedded into this hybrid modulation. Fig.2 shows the general structure of the proposed hybrid SC-SPWM scheme. It consists of a base PWM generator and a hybrid PWM controller to generate the new modulation pulses.

In this modulation strategy, three base PWM signals are required for each module operation in a cascaded multilevel inverter. A sequential signal (A) is a square wave signal with a 50% duty ratio and half the fundamental frequency. This signal makes every power switch operate with SC-SPWM and fundamental frequency PWM sequentially to equalize the power losses among the switches. Fundamental frequency PWM (B) is a square wave signal synchronized with a modulation waveform; $B = 1$ during the positive half cycle of the modulation signal, and $B = 0$ during negative half cycle.

A SC-SPWM signal is obtained by a comparison of the rectified modulation waveform of each module with the carrier waveform. The amplitude of the modulation waveform is defined as . A SC-SPWM pulse for inverter-I (C) is obtained by a comparison between the rectified modulation waveform and the carrier signal, while a SC-SPWM pulse for inverter-II (D) is obtained by a comparison between the rectified

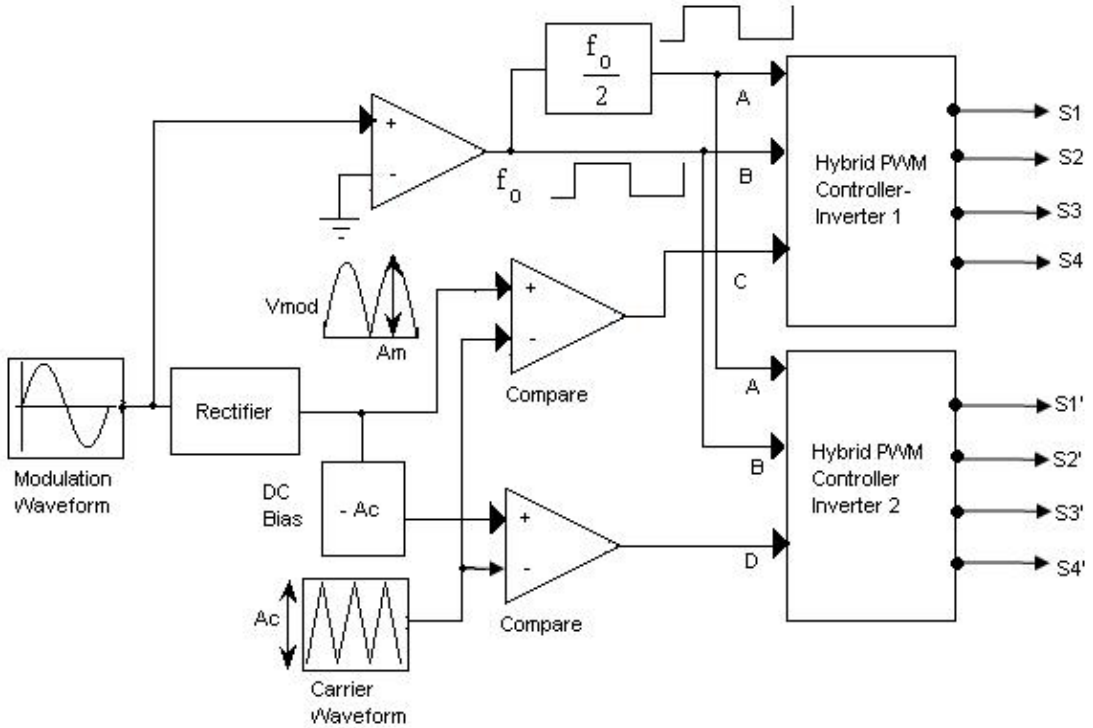


Fig. 2. Scheme of five level hybrid single carrier sinusoidal PWM (one phase leg).

modulation waveform with a bias of and the carrier waveform. The base modulation signals (A, B, C, and D) are shown in fig.3(b).

A hybrid PWM controller is designed using a simple combinational logic. The functions of the combinational logic for a five level hybrid SC-SPWM operation are expressed as:

$$\begin{array}{ll} S1 = ABC + \bar{A}B & \\ S2 = \bar{A}BC + \bar{A}\bar{B} & \\ S3 = \bar{A}\bar{B}C + A\bar{B} & \\ S4 = \bar{A}BC + AB & \end{array} \quad and \quad \begin{array}{l} S1' = ABD + \bar{A}B \\ S2' = \bar{A}BD + \bar{A}\bar{B} \\ S3' = \bar{A}\bar{B}D + A\bar{B} \\ S4' = \bar{A}BD + AB \end{array}$$

where A is the sequential signal, B is the fundamental frequency PWM, C is the SC-SPWM for inverter-I and D is the SC-SPWM for inverter-II. In fig.3(c), it is shown that each gate signal is composed of both low frequency PWM and SC-SPWM pulses. If the sequential switching signal $A = 1$, then $S1, S2, S1'$ and $S2'$ are operated with SC-SPWM, while $S3, S4, S3', S4'$ are operated with fundamental frequency PWM. If the sequential switching signal $A = 0$, then $S1, S2, S1'$ and $S2'$ are operated with fundamental frequency PWM, while $S3, S4, S3'$ and $S4'$ are operated with SC-SPWM. Since A is a sequential signal, the average switching frequency amongst the four switches is equalized. The voltage stress and current stress of the power switches in each inverter bridge is inherently equalized with this modulation.

C. Generalized Hybrid PWM Algorithm Formulation

For completeness, the generalized formulation that suits for an N level inverter and for any number of switching transitions is presented. The mathematical model of the N level SC-SPWM is required for on-line digital implementation. It is derived from the point of intersection between the single carrier and the sampled modulation signals. The modulation signals for the five-level SC-SPWM can be described as:

$$S_1(t) = A_m \sin[\omega t + \frac{\pi}{m_f}];$$
$$S_2(t) = A_m \sin[\omega t + \frac{\pi}{m_f}] - A_c$$

where the angular frequency $\omega = \frac{2\pi}{m_f}$.

The straight line equation for the carrier wave can be expressed as $C(t) = -2A_c f_c t + hA_c, h = 1, 2, 3 \ldots$ A generalized equation to generate the i^{th} SC-SPWM pulses for a cascaded inverter of any level N is given by $a_u(i) = \frac{1}{2f_c}[(2i + u - 2) - \frac{A_m}{A_c}\sin(\omega(i-1) + \frac{\pi}{m_f})]$, where i represents the position of each of the modulated pulses $(i = 1, 2, 3 \ldots\ldots m_f/2)$ and $u = 1, 2 \ldots K$ represents which full bridge inverter is being referred to. The sequential switching signal and the fundamental frequency PWM signals for each phase are same for all of the full bridge inverter modules.

The generalized formulation of a combinational logic that suits for each inverter module is given by:

$$S_{u1} = ABZ + \bar{A}B; S_{u2} = \bar{A}BZ + \bar{A}\bar{B};$$
$$S_{u3} = \bar{A}\bar{B}Z + A\bar{B}; S_{u4} = \bar{A}BZ + AB$$

where Z is the SC-SPWM for the K^{th} full bridge inverter. An independent hybrid PWM controller is used to mix a sequential switching signal, a low frequency PWM and its corresponding SC-SPWM for developing a hybrid SC-SPWM in the K^{th}

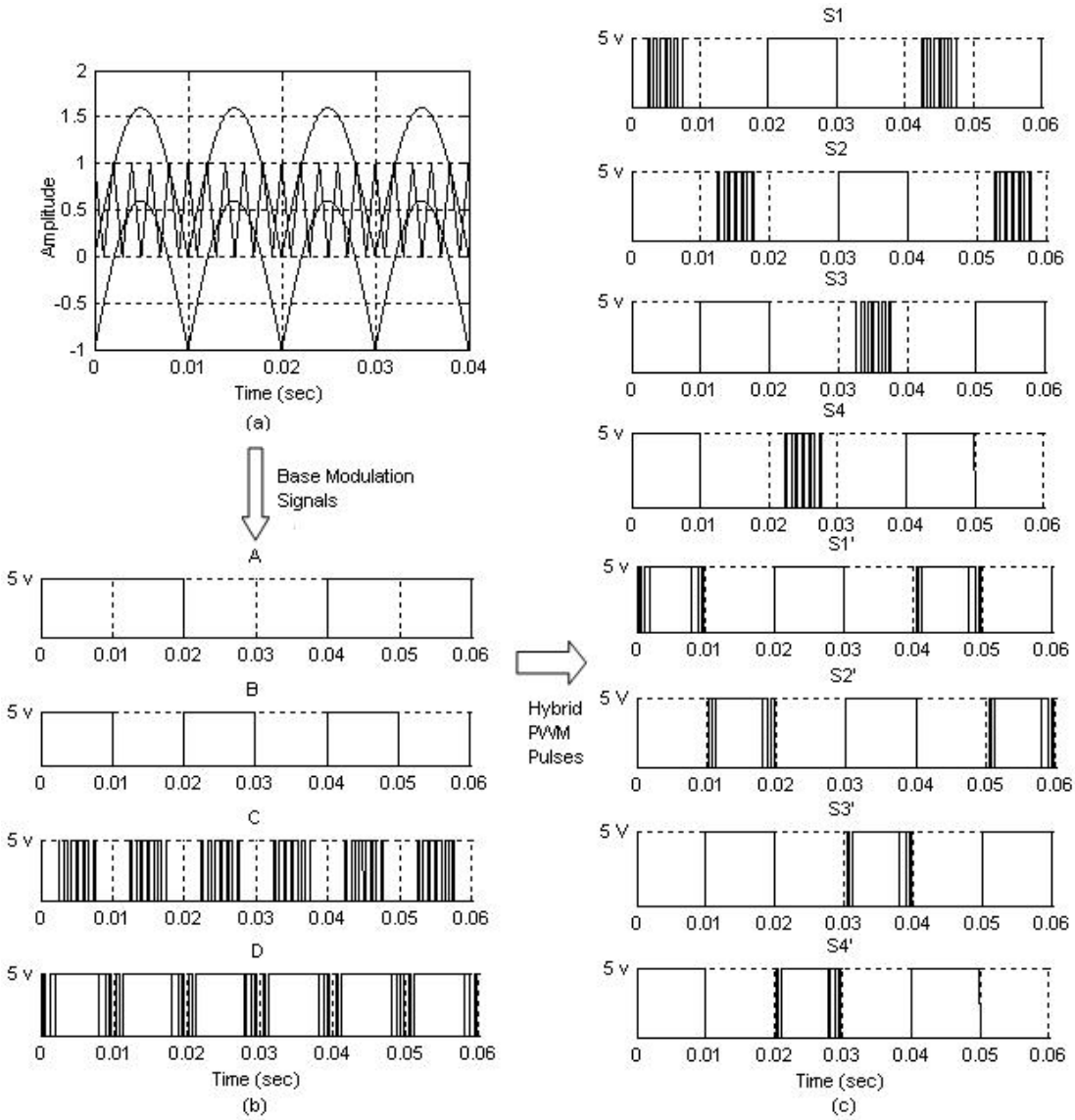


Fig. 3. (a) Carrier and modulation waveforms (b) Base modulation signals (c) Hybrid single carrier sinusoidal PWM pulse pattern for five level inverter.

inverter cell. Similarly, hybrid SC-SPWM pulses are developed for all of the inverter modules of the cascaded inverter. A total of $4K$ gate pulses per phase are developed to operate an N level multiphase multilevel inverter.

III. PERFORMANCE ANALYSIS

A. Spectral Analysis of the output voltage waveform

The quality of the output voltage waveforms from hybrid SC-SPWM operation is evaluated based on the performance indexes namely the total harmonic distortion (THD), and the weighted total harmonic distortion (WTHD). The total harmonic distortion of a signal is the ratio of the sum of the powers of all the harmonic frequencies above the fundamental frequency to the power of the fundamental frequency. The THD is calculated using $THD = \frac{\sqrt{\sum_{n=2}^{50} V_n^2}}{V_1}$ up to 50^{th} order of harmonics and is plotted in fig.4. The low pass filter and the nature of the highly inductive load will take care of the higher order of harmonics. It is found that the proposed PWM offers a lower THD when compared to the conventional one. Furthermore, it is noticed that the higher the value of the modulation index (M), the lower the value of the THD. This is also true for an increased frequency ratio.

The weighted total harmonic distortion (WTHD) is superior to the THD as a figure of merit for a non sinusoidal inverter waveform in which the lower portion of the frequency spectrum is weighted heavily. It more accurately portrays the expected harmonic current of an inductive load [9].

The WTHD uses a spectral weighting factor and it is calculated using $WTHD = \frac{\sqrt{\sum_{n=2}^{50} \left(\frac{V_n}{n}\right)^2}}{V_1}$ and plotted in fig.5. As expected, the WTHD values are lower when the modulation index is closer to unity and when the carrier frequency increases.

In the linear modulation range (0.5<M<1), the RMS value of the significant harmonic (23^{rd}) to the fundamental compo-

nent is within 20% and it is even less in over modulation (M>1) for a frequency ratio of 30. But the lower order harmonics 3^{rd}, 5^{th} and 7^{th} are present under 3% of the fundamental value in over modulation operation. When the inverter operates with an odd frequency ratio, it produces even side band harmonics and when it operates with an even frequency ratio, it produces odd side band harmonics. Furthermore, harmonics at the carrier frequency and its multiples do not exist at all. The switching function approach is used to analysis the inverter input current ripple which can be easily simulated in MATLAB. The switching functions are a Fourier series representation of the switching sequence used for PWM control of the inverter switching devices. The inverter is analysed with a balanced load in which the current ripple is at its mininum at a unity power factor and it is at its maximum at 0.3 as a power factor.

B. Power Loss Analysis

A MATLAB-Simulink model of a five level inverter has been developed to study the power loss. Only conduction and switching losses are considered for the analysis in this paper. The carrier frequency f_c is 2 kHz and each converter cell is connected to a 100V DC supply. The IGBTs selected (IRG4BC20SD) have maximum ratings that are a forward current of 19A and a direct voltage of 600V. The semiconductor power losses can be estimated from the curves $(V_{sat}(\theta) \times I_l(\theta))$ and $(E(\theta) \times I_l(\theta))$, presented in the datasheets of each

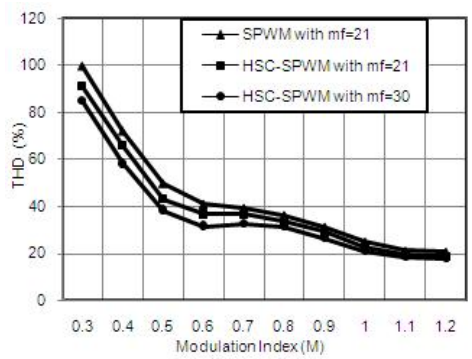


Fig. 4. THD comparsion of hybrid SC-SPWM with SPWM for five level inverter operation.

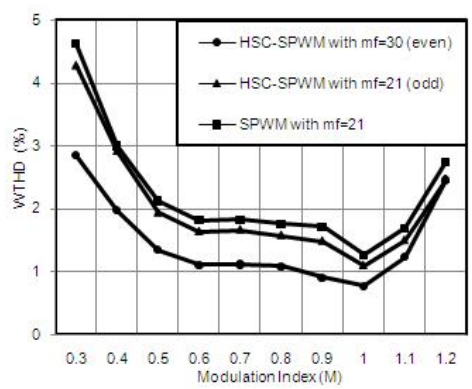
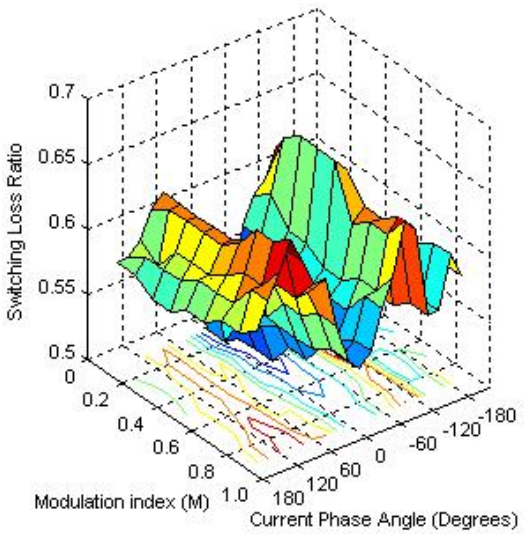
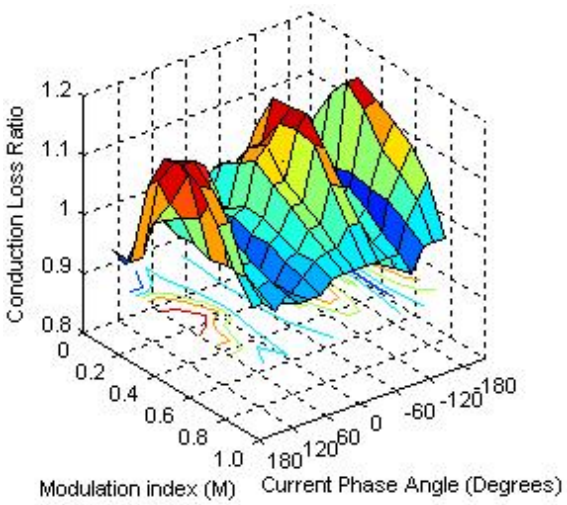


Fig. 5. WTHD comparsion of hybrid SC-SPWM with SPWM for five level inverter operation.



(a)



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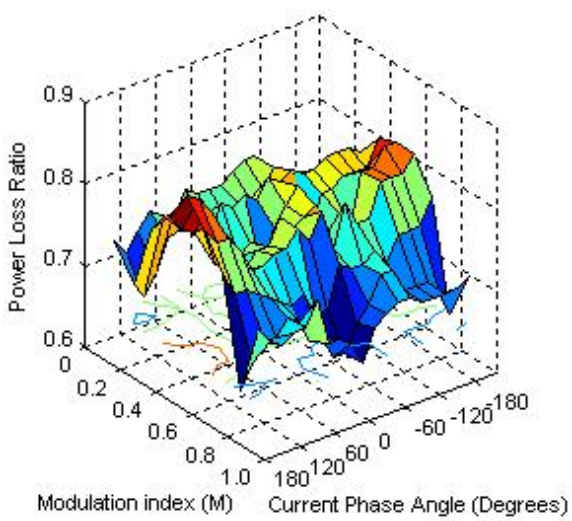
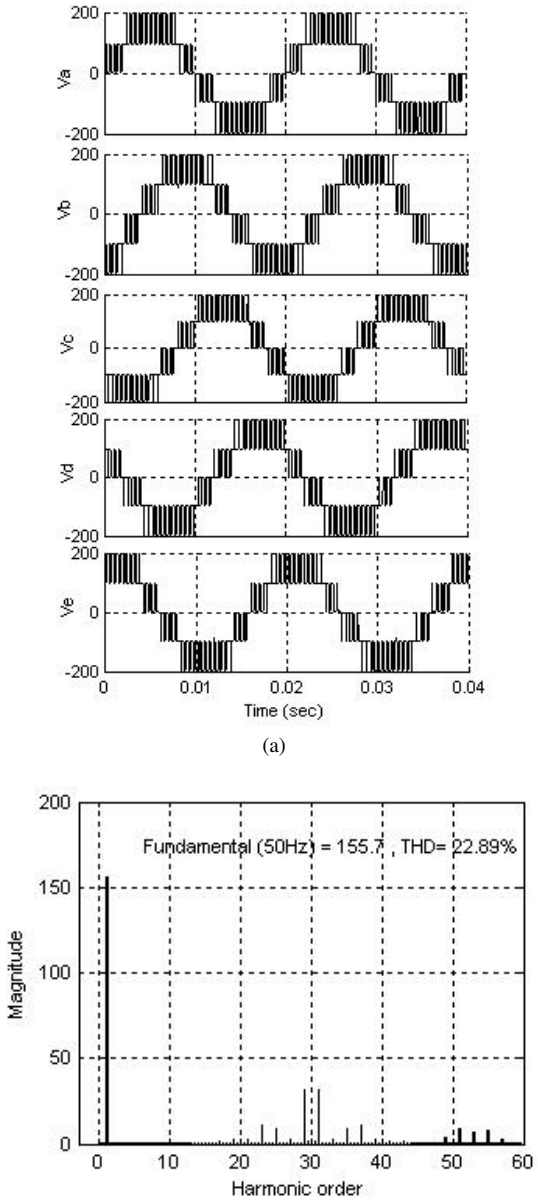


(c)

Fig. 6. Ratio of the losses of hybrid SC-SPWM and conventional SPWM fed five level cascaded inverters. (a) Switching losses. (b) Conduction losses. (c) Total power loss.

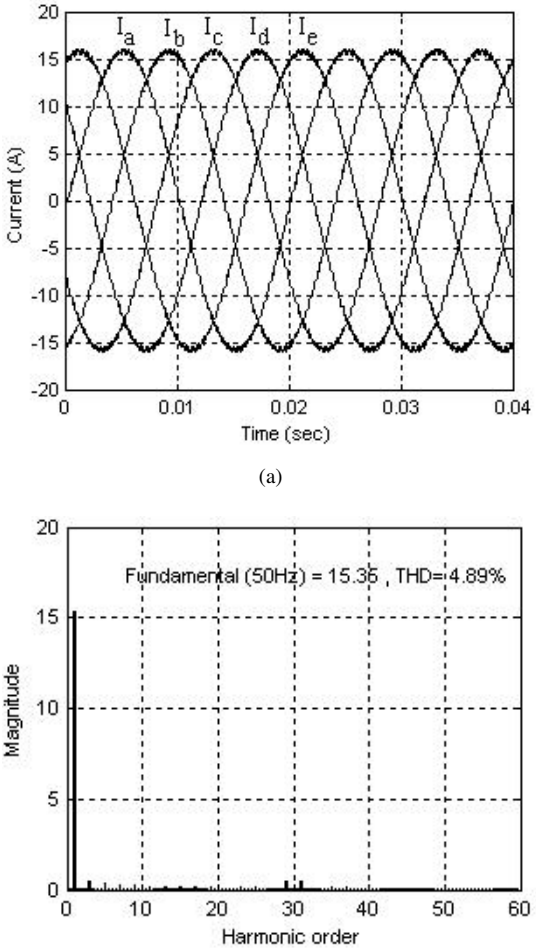


(a) (b)

Fig. 7. Simulation results for five phase five-level inverter with hybrid SC-SPWM operation in linear modulation for f_0 = 50Hz, and f_c = 1.5kHz (a) Output phase voltage waveforms. (b) Phase voltage spectrum (V_a).

device, where V_{sat} is the on-state saturation voltage ($V_{cs}(\theta)$ for the IGBT and $V_F(\theta)$ for the diode) and $E(\theta)$ represent the energy losses in one commutation ($E_{on}(\theta)$, if it is a turn-on commutation, ($E_{off}(\theta)$, if it is a turn-off commutation and ($E_{rec}(\theta)$, if it is a diode reverse recovery process). The mathematical models obtained for the IGBTs (IRG4BC20SD) are given by:

$$V_{ce} = 0.96e^{0.0016I_l(\theta)} - 0.4654e^{-0.044I_l(\theta)}$$
$$V_F = 0.6e^{0.002I_l(\theta)} - 0.4258e^{-0.0275I_l(\theta)}$$
$$E_{rec} = 0.00806e^{0.000322I_l(\theta)} - 0.0057e^{-0.00446I_l(\theta)}$$
$$E_{on} = 0.0041e^{0.0044I_l(\theta)} - 0.0037e^{-0.008I_l(\theta)}$$
$$E_{off} = 0.0443e^{0.00021I_l(\theta)} - 0.0547e^{-0.00107I_l(\theta)}$$



(a) (b)

Fig. 8. Simulation results for five phase five-level inverter with hybrid SC-SPWM for f_0 = 50Hz, f_c = 1.5kHz, and modulation index $M = 0.8$ (a) Phase current waveforms, (b) Phase current spectrum.

$$I_l(\theta) = M^* I_{max} \sin(\theta - \varphi)$$

where $I_l(\theta)$ is the load current, M is the modulation index, and φ is the load displacement angle.

Switching losses are generated during the turn-on and turn-off switching processes of the power devices [10]. The switching loss for every power device (P_{sw}) is obtained separately by identifying every turn-on and turn-off instant during one reference period using:

$$P_{sw} = \frac{1}{T}\Sigma(E_{on} + E_{off} + E_{rec})$$

where E_{on} is the turn on energy loss per commutation, E_{off} is the turn off energy loss per commutation and E_{rec} is the energy loss during the reverse recovery process. The total sum gives the switching loss P_{sw_T}.

Conduction losses are those that occur while the semiconductor device conducts current. The calculation of conduction losses for each semiconductor of the inverter is given by:

$$P_{cond\_IGBT} = \frac{1}{2\pi}\int_0^{2\pi} V_{ce}(\theta) * I_l(\theta) * V_{cmd}(\theta) d\theta$$

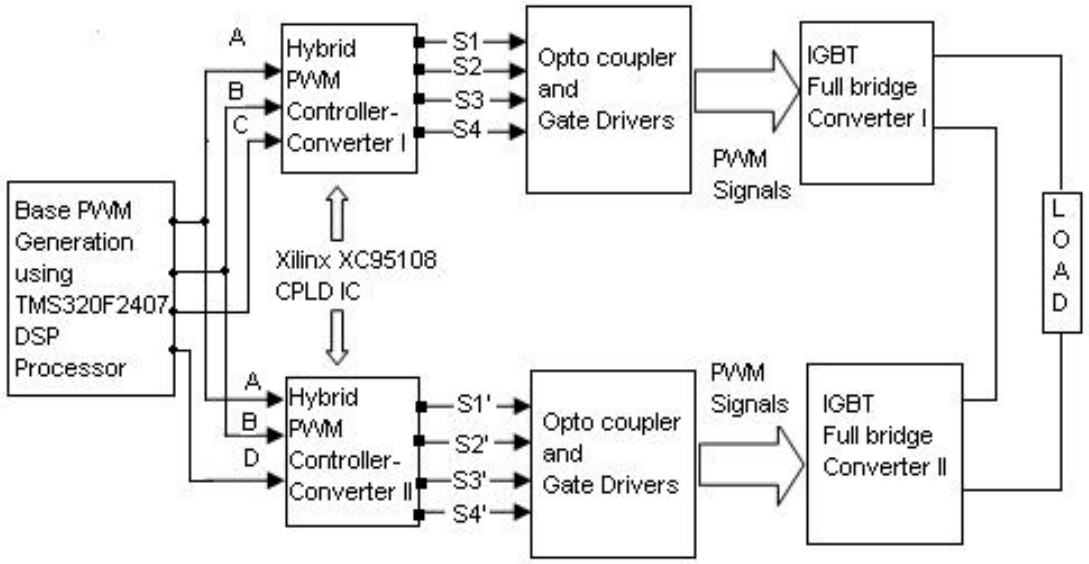


Fig. 9. Functional block diagram of hybrid CBSVM implementation (one phase).

$$P_{cond\_D} = \frac{1}{2\pi}\int_0^{2\pi} V_F(\theta) * I_l(\theta) * V_{cmd}(\theta) d\theta$$

where $V_{cmd}(\theta)$ is the PWM signal of the IGBTs. The sum of the conduction losses for all of the IGBTs ($P_{cond\_IGBT\_T}$) and for all of the diodes ($P_{cond\_D\_T}$) is computed to obtain the total conduction losses.

$$P_{cond\_T} = P_{cond\_IGBT\_T} + P_{cond\_D\_T}$$
$$P_{Total} = P_{cond\_T} + P_{sw\_T}.$$

Fig. 6(a) shows, for the full range of modulation indexes and relative angles of the output currents, the ratio of the switching losses for a five level inverter with the modulation strategy proposed in this paper versus the conventional PWM technique. The fundamental component of the current is kept constant while varying its phase angle. It is noted that the surface is always below one, which means that the switching losses are significantly smaller for the proposed method. Fig. 6(b) shows that the conduction losses are higher. This is because of an increase in the conduction period due to the mixing of the fundamental frequency PWM. Fig.6(c) shows the ratio of the total power losses between the two PWM methods.

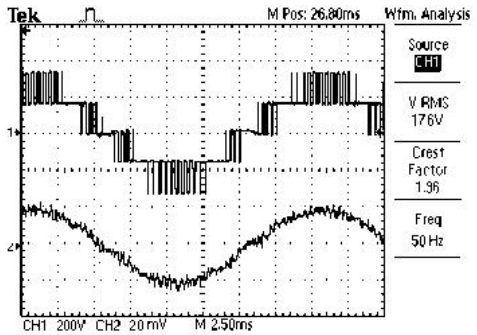
Since the switching losses are predominant, the power losses of the proposed PWM method are less than those of conventional PWM operations. The mean value of the surface is found to be approximately 0.7152, which means that the power loss reduction is about 28.5%. The best case is produced for a unity power factor and a modulation index of one. Under these conditions the power loss saving is about 31%. In a practical high power system, the switching losses are higher than the conduction losses. Therefore, reducing the switching losses becomes important for improving the efficiency of the system.

IV. SIMULATION AND EXPERIMENTAL RESULTS

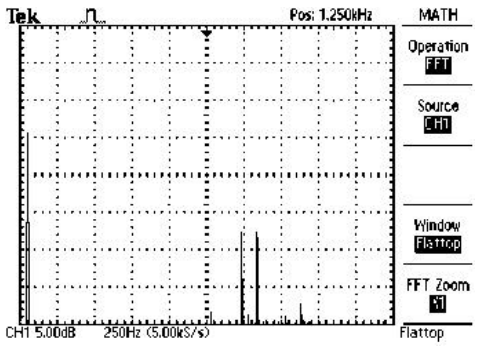
In order to verify that the proposed PWM can be practically implemented in a five phase multilevel inverter, simulations were performed using MATLAB/Simulink software. It also helps to confirm the PWM switching s trategy which can be implemented in a digital signal processor (DSP) and a complex programmable logic device (CPLD). The load resistance and inductance are 10Ω and 15mH, and the dc bus voltage is set at 100V. The inverter is operated in the linear modulation range and the corresponding phase voltage waveforms with FFT analysis are shown in fig.7 (a)-(b).

It can be seen that all the lower order harmonics are absent and that the fundamental is controlled at its pre-defined value. It is interesting to note that the next significant harmonic will be the 23^{rd} for a frequency ratio of 30. The significant harmonics are the 23^{rd}, 25^{th}, 29^{th}, and 31^{st}, which are high frequency, with RMS values under 11% of the fundamental term. In addition, the current waveform appears highly sinusoidal due to the inherent low voltage distortion provided by the multilevel PWM operation. This can be clearly appreciated with the current harmonic spectrum shown in fig.8 (b).

To verify the validity of the proposed hybrid modulation, a five phase five-level inverter is designed to implement this scheme. Fig.11 shows a functional block diagram of the laboratory based prototype of a five level inverter (one phase leg) that is implemented with eight insulated gate bipolar transistor (IGBT) switches with internal anti-parallel diodes (IRG4BC20SD). The base PWM pulses (fundamental frequency PWM and SC-SPWM) are generated using a low cost high speed Texas Instruments TMS320F2407 digital signal processor (DSP) board with an accuracy of $20\mu s$. A sequential signal is generated to operate each IGBT with fundamental frequency PWM and SC-SPWM sequentially to equalize power losses and heating among the devices. A hybrid PWM control algorithm based on combinational logic is developed and it



(a)



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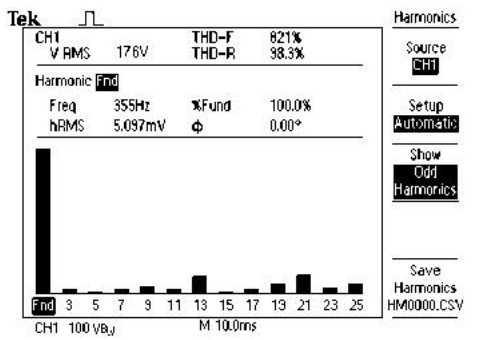

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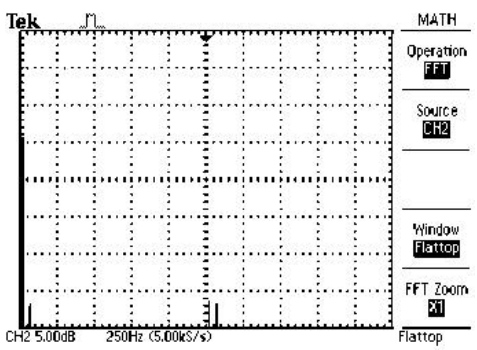

(d)

Fig. 10. Experimental results of the five phase five-level inverter with hybrid SC-SPWM for f_0 = 50Hz, f_c =1500Hz, and modulation index $M = 0.8$. (a) Phase voltage and current waveform. (b) Phase voltage spectrum. (c) Phase voltage harmonic spectrum (d) Phase current spectrum.

is implemented in a Xilinx CPLD XC95108 IC. The CPLD controller combines fundamental frequency PWM, sequential signal and SC-SPWM to generate hybrid modulation pulses for a five level inverter.

The XC95108 IC is used to develop the control algorithm, since it has a better response for high frequency input signals, narrow pulse width pulses and no jitter of the delay in the circuit. A switching dead time of $1\mu s$ is introduced into the CPLD hardware. The optically coupled isolators (MCT2E) are used to provide electrical isolation between the Xilinx CPLD controller board and the power circuit. Four high voltage high speed IGBT drivers (IR2112) are used to provide proper and conditioned gate signals to the power switches. A digital real time oscilloscope (Tektronix TPS2024) is used to display and capture the output waveforms. With its Fast Fourier Transform (FFT) feature the spectrum of the output voltage is obtained for different operating points as discussed hereafter. The DC bus voltage is set at 100V and the frequency of the modulated wave and the carrier wave are 50 Hz and 1500 Hz, respectively.

Selected experimental results for a five phase five-level inverter are obtained and they validate the simulation results. Specifically, Fig.10 (a) shows the phase voltage and current waveform of the proposed five-level hybrid SC-SPWM for a standard modulation range and the associated spectrum is presented in fig.10 (b) and (d), respectively. It is confirmed that the harmonic cancellation up to the sidebands around the carrier frequency is achieved in the voltage waveform and that the first significant harmonic is the 23^{rd} as predicted.

V. CONCLUSIONS

A hybrid single carrier sinusoidal modulation technique for multiphase multilevel inverters was presented in this paper. This hybrid modulation was based on a combination of fundamental frequency PWM and single carrier sinusoidal modulation for multiphase inverter operation. Compared to conventional SC-SPWM, a reduced numbers of switchings was obtained while achieving the same fundamental voltage tracking. It also offered a reduction of 28.5% in power loss. The best case was produced at a unity power factor and a unity modulation index. Under these conditions the power loss saving was about 31%. It was shown that the harmonic performance of the proposed PWM strategy was better when compared to standard sinusoidal modulation throughout the entire range of modulation indexes. It was also shown to be valid for any number of phases or levels and that it can be used with standard cascaded inverter topologies. In addition, the proposed algorithm was found suitable for real time implementation due to its low computational complexity. Analyses, simulations and experimental results demonstrated the superiority of the proposed system.

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