This document is downloaded from DR‑NTU (https://dr.ntu.edu.sg)
Nanyang Technological University, Singapore.

Analysis and modeling of internal state variables for dynamic effects of nonvolatile memory devices

Shang, Yang; Fei, Wei; Yu, Hao

2012

Shang, Y., Fei, W., & Yu, H. (2012). Analysis and modeling of internal state variables for dynamic effects of nonvolatile memory devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 59(9), 1906‑1918.

https://hdl.handle.net/10356/95525

https://doi.org/10.1109/TCSI.2011.2180441

© 2012 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. The published version is available at: [DOI: http://dx.doi.org/10.1109/TCSI.2011.2180441].

Downloaded on 24 Aug 2022 23:22:28 SGT

Analysis and Modeling of Internal State Variables for Dynamic Effects of Nonvolatile Memory Devices

Yang Shang, *Student Member, IEEE*, Wei Fei, *Student Member, IEEE*, and Hao Yu, *Member, IEEE*

***Abstract*—Hybrid integration of CMOS and nonvolatile memory (NVM) devices has become the foundation for emerging nonvolatile memory-based computing. The primary challenge to validate hybrid memory system with both CMOS and NVM devices is to develop a SPICE-like simulator that can simulate the dynamic behavior accurately and efficiently. Since memristor, spin-transfer-toque magnetic-tunneling-junction (STT-MTJ) and phase-change-memory (PCM) devices are the most promising candidates of next generation of NVM devices, it is under great interest in including these new devices in the standard CMOS design flow. The previous approaches either ignore dynamic effect without consideration of internal states for dynamic behavior, or need complex equivalent circuits to represent those devices. This paper proposes a new modified nodal analysis for NVM devices with identified internal state variables for dynamic behavior. As such, compact SPICE-like implementation can be derived for all three new NVM devices in the design of large-scale memory circuits. As demonstrated by a number of examples on hybrid memory circuits with both CMOS and NVM devices, our newly developed SPICE-like simulator can capture dynamic behaviors of memristor, STT-MTJ and PCM devices, and can also reduce CPU runtime by 20–69 times when compared to the previous equivalent circuit based approaches.**

***Index Terms*—Internal state variable, memristor, nonvolatile memory (NVM) device, spin-transfer-toque magnetic-tunneling-junction (STT-MTJ), phase-change-memory (PCM), SPICE-like simulation.**

I. Introduction

THE recent advance in nonvolatile memory (NVM) has introduced promising future for the development of memory-based-computing with a natural merge of processor and memory, which might break the bandwidth-bottleneck of the conventional von Neumann architecture. A range of NVM devices [1]–[3] such as memristor, phase-change RAM (PCRAM), magnetic RAM (MRAM) and resistive RAM (RRAM), have appeared to potentially replace both SRAM and DRAM for the memory hierarchy in the conventional computing system. More importantly, the nonvolatile property of new devices leads to fast access time, low energy and high integration density. For example, compared to the traditional memory devices, spin-toque-transfer (STT) magnetic-tunneling-junction (MTJ) based MRAM has a 3–4 times reduced cell size which is about 6–8 F^2 (F is the minimum technology dimension, $\sim 0.4\,\mu$m) [4]. With the advance in nanotechnology, even higher integration density can be achieved by memristor based crossbar-array, which can be fabricated with pitch of 17 nm [5]. Such advantage can be further enhanced by 3-D stacking [6].

In the emerging NVM technologies, very often new devices cannot be fully described by the conventional circuit state variables which are nodal voltage and branch current. For instance, additional internal state variables have to be considered when describing the dynamic behavior of following NVM devices: magnetization for STT-MTJ, doping ratio for memristor, temperature and crystalline fraction for PCM. The previous approaches describe these NVM devices by equivalent circuit [7]–[11] with additional circuit components and hence increased complexity. The equivalent circuit approaches are limited to deal with internal state variables for dynamic because many additional circuit components are required to maintain high accuracy. One equivalent circuit may require dozens of extra circuit components to describe one NVM device, and hence results in huge overhead to model and simulate large-scale memory designs. As such, novel modeling and simulation techniques are needed to improve the computation efficiency for the memory circuit design with hybrid CMOS and NVM devices.

In order to consider the new nonvolatile memory devices similarly to how we dealt with CMOS devices by physics based model, one critical perspective is to identify and include the new state variable relevant for the new dynamic behavior of the nonvolatile devices [12]. Note that different from device parameters, a device state variable varies with time under given input signals. Here, we deploy the term "internal state variables" to represent those physics-based state variables which cannot be observed from external electric behavior, while the conventional state variables such as nodal voltage and branch current are called "external state variables." Take STT-MTJ for instance, many variables can be extracted from the physics point of view, such as temperature, polarization, magnetization, etc. Variables like temperature and electron polarization are assumed to be constant and therefore called parameters, but the variable of magnetization is the state associated with STT-MTJ and can change with time similar to the states of nodal voltages and branch currents. As such, the angles to describe magnetization are identified as internal state variables for STT-MTJ devices.

In this paper, we have the following primary contributions: 1) internal state variables have been identified for the consideration of nonlinear dynamic models for memristor, STT-MTJ and PCM; and 2) a new modified nodal analysis (MNA) formulation has been developed to consider internal state variables of

Manuscript received July 30, 2011; revised September 27, 2011; accepted November 20, 2011. Date of publication January 24, 2012; date of current version August 24, 2012. This work was supported by MOE TIER-2 ARC5/11 and MOE TIER-1 RG26/10. This paper was recommended by Associate Editor M. Anis.

The authors are with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (e-mail: haoyu@ntu.edu.sg).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

TABLE I
DEFINITIONS OF VARIABLES USED FOR SPICE-LIKE SIMULATOR

Variables	Definitions
s_m	internal state variable for new MNA
v_n, j_b	traditional state variables for MNA: nodal voltage and branch current
v_b, j_i, j_l	branch voltage, source current, and inductor current
$\mathcal{G}, \mathcal{C}, L_l$	traditional conductance, capacitance and inductance
$\mathcal{S}$	new Jacobian as memductance
$\mathcal{K}_v^F, \mathcal{K}_s^F, \mathcal{K}_v^G, \mathcal{K}_s^G$	new Jacobians introduced by s_m
E_c, E_g, E_l, E_i	incident matrix for capacitor, resistor, inductor and current source
E_m	new incident matrix introduced for NVM devices
f, g	functions introduced by s_m for new state equations

nonvolatile memory devices within one SPICE-like simulator. Experiments show that our new MNA formulation with internal state variable can handle the simulation of timing, power, variation and detailed transient behavior for the hybrid design of CMOS and NVM devices at large scale, with results consistent with the measurement. More importantly, compared to equivalent circuit approaches that only consider the static behavior or with large overhead of additional nodes, the newly developed SPICE-like simulator can be used to study the dynamic behavior of NVM device and the CPU time can be reduced by 20–69 times.

The rest of this paper is organized in the following manner. We first introduce the general derivation of a new MNA formulation to consider internal state variables of nonvolatile memory devices in Section II. Then in Section III, the dynamic models of typical NVM devices: memristor, STT-MTJ and PCM device are briefly discussed. The SPICE implementation with the use of internal state variables in our simulator is also illustrated. Experimental results and discussion are presented in Section IV, and the paper is concluded in Section V.

II. MODIFIED NODAL ANALYSIS OF NVM DEVICES

The appearance of state variable of an electronic device could be the result of the interaction of numbers of physical phenomenon at different domains. In the traditional circuit analysis for electronic device, nodal voltage and branch current are employed to describe the device terminal change with time. However, for memory relevant devices such as memristor [13], the nonlinear dynamic with memory effect cannot be explicitly described by these two states and additional internal state variables have to be introduced [12]. These internal state variables can be represented by the external state variables from equivalent circuit point of view [7]–[11] but with increased circuit complexity for simulation. In order to directly include internal state variables, we have introduced a new modified nodal analysis (MNA) for internal state variables of NVM devices, which can provide compact physics-based description for internal states with high efficiency and accuracy. All the relevant variables used in this section are summarized in Table I.

A. Background of Traditional MNA

MNA is constructed based on Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) [14]. These two laws can be compactly formulated by an incidence matrix

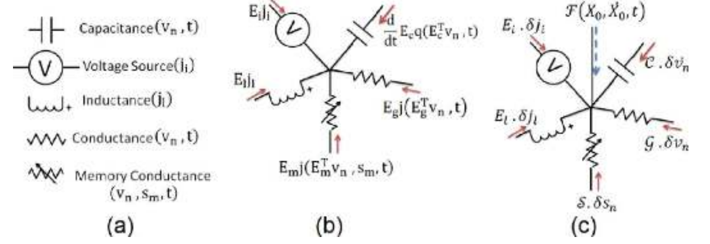

Fig. 1. New MNA with: (a) components and state variables; (b) large signal KCL; and (c) small signal KCL.

determined by the topology of circuits. Assuming n nodes and b branches, the incident matrix E ($\in \mathrm{R}^{n\times b}$) is defined by

$$e_{i,j} = \begin{cases} 1, & \text{if branch } j \text{ flows into node } i \\ -1, & \text{if branch } j \text{ flows out of node } i \\ 0 & \text{if branch } j \text{ is not included at node } i. \end{cases}$$

With j_b, v_b and v_n defined as in Table I, KCL and KVL can be described by

$$\text{KCL} : E\, j_b = 0 \quad \text{KVL} : E^T v_n = v_b.$$

Considering the presence of capacitor, inductor, resistor, and voltage controlled voltage source, the KCL and KVL become

$$\frac{d}{dt}E_c q\left(E_c^T v_n, t\right) + E_g j\left(E_g^T v_n, t\right) + E_l j_l + E_i j_i = 0,$$
$$L_l \frac{d}{dt} j_l - E_l v_n = 0, \quad E_i^T v_n = 0.$$

Here the four incident matrices $[\,E_c \quad E_g \quad E_l \quad E_i\,]$ describe the topological connections of capacitive, conductive, inductive, and voltage-source elements. Matrix L_l provides values for inductors in the circuit. Introducing the state variable $x = [\,v_n \quad j_l \quad j_i\,]^T$, the above MNA formulation can be denoted shortly by a differential-algebra-equation (DAE) as follows:

$$\mathcal{F}(x, \dot{x}, t) = \frac{d}{dt}q(x,t) + j(x,t) = 0. \tag{1}$$

B. New MNA With Internal State Variables

In order to handle the dynamic models of NVM device with internal state variables, one needs to develop a new MNA by adding internal state variables into the traditional MNA (for CMOS devices). As shown in Fig. 1(a), these internal state variables, termed as s_m, determine the conductance of all nonvolatile memory devices, termed as memductance (memory conductance) here, and therefore can be categorized as one new device branch. Note that the simulation time is directly related to the total number of state variables generated for the circuit. Compared to the traditional approaches with complex equivalent circuits, the introduction of memductance adds much fewer state variables by including internal state variables to represent dynamic effect of NVM device. Take memristor for example, its equivalent circuit requires dozens of additional nodal voltages to characterize the circuit behavior, while only two nodal voltages and one internal state variable are required in our memductance approach. Therefore, the introduction of memductance greatly simplifies the model complexity and in turn largely reduces the verification and design cost.

One NVM device may require one or multiple internal state variables to accurately describe its dynamic behaviors. The corresponding incident matrix is termed as E_m, with which the nonvolatile device branch current is obtained as $E_m j(E_m^T v_n, s_m, t)$. As Fig. 1(b) shows, combined with branch currents from the traditional CMOS devices, a new KCL equation is formed by

$$\begin{aligned}
&\frac{d}{dt}E_c q\left(E_c^T v_n, t\right) + E_m j\left(E_m^T v_n, s_m, t\right) + E_g j\left(E_g^T v_n, t\right) \\
&\quad + E_l j_l + E_i j_i = 0 \\
&L_l \frac{d}{dt} j_l - E_l v_n = 0; \quad E_i^T v_n = 0 \\
&f\left(E_m^T v_n, s_m, t\right) + \frac{d}{dt} g\left(E_m^T v_n, s_m, t\right) = 0.
\end{aligned} \tag{2}$$

Here functions f and g are the additional state equations for nonvolatile devices with s_m. Moreover, with the new state variable vector $X = [v_n, j_i, j_l, s_m]^T$, the above new MNA can still be described by the differential-algebra-equation (DAE) as (1).

We can further derive the Jacobian as generalized conductance $\mathcal{G}$, capacitance $\mathcal{C}$, and memductance $\mathcal{S}$. The additional term of memductance $\mathcal{S}$ is introduced to describe the conductance of nonvolatile devices for the induced current change under the change of internal state s_m. At one biasing point X_0, the first-order derivative or Jacobian of the new DAE with respective to X are

$$\begin{aligned}
\mathcal{G} &= \left(E_g \frac{d}{dv_b^g} j\left(v_b^g, t\right) E_g^T \right. \\
&\quad \left. + E_m \frac{d}{dv_b^m} j\left(v_b^m, s_m, t\right) E_m^T \right)\Bigg\|_{X=X_0} \\
\mathcal{C} &= \left(E_c \frac{d}{dv_b^c} q\left(v_b^c, t\right) E_c^T \right)\Bigg\|_{X=X_0} \\
\mathcal{S} &= \left(E_m \frac{d}{ds_m} j\left(v_n^m, s_m, t\right) E_m^T \right)\Bigg\|_{X=X_0}
\end{aligned} \tag{3}$$

where $v_b^g = E_g^T v_n, v_b^m = E_m^T v_n, v_b^c = E_c^T v_n$.

In addition, there are four additional Jacobian terms introduced from functions f and g due to the new state variable s_m for NVM device

$$\begin{aligned}
\mathcal{K}_v^F &= \left(E_m \frac{d}{dv_b^m} f\left(v_b^m, s_m, t\right) E_m^T \right)\Bigg\|_{X=X_0} \\
\mathcal{K}_s^F &= \left(E_m \frac{d}{\mathrm{ds_m}} f\left(v_b^m, s_m, t\right) E_m^T \right)\Bigg\|_{X=X_0} \\
\mathcal{K}_v^G &= \left(E_m \frac{d}{dv_b^m} g\left(v_b^m, s_m, t\right) E_m^T \right)\Bigg\|_{X=X_0} \\
\mathcal{K}_s^G &= \left(E_m \frac{d}{ds_m} g\left(v_b^m, s_m, t\right) E_m^T \right)\Bigg\|_{X=X_0}.
\end{aligned} \tag{4}$$

The subscripts v and s denote the derivatives to nonvolatile device branch voltage v_b^m and its internal state variable s_m, respectively. The superscript F and G correspond to functions f and g, which describe the additional state equation for the internal state variable s_m.

TABLE II
DEFINITIONS OF VARIABLES USED FOR MEMRISTOR DEVICE

Variables	Definitions
$w(t)$	doping ratio (W/D), $w(t) \in [0,1)$ (state variable)
$dw(t)/dt$	normalized drift velocity
W	Length of the doped region
D	thickness of memristor film
R_{on}	ON-state resistance
R_{off}	OFF-state resistance
$F(x)$	window function defining the boundary condition of $w(t)$
μ	mobility at small electric field
E_0	characteristic field for a particular mobile atom in the crystal

In addition, with the new small-signal current introduced by s_m as shown in Fig. 1(c), the new linearized small-signal DAE becomes

$$\begin{aligned}
&\mathcal{G} \cdot \delta v_n + \mathcal{C} \cdot \delta \dot{v_n} + E_i \cdot \delta j_i + E_l \cdot \delta j_l + \mathcal{S} \cdot \delta s_m \\
&\quad = -\mathcal{F}(X_0, \dot{X}_0, t) \\
&E_i^T \cdot \delta v_n = 0; \quad E_l^t \cdot \delta v_n = L_l \cdot \delta \dot{j_l} \\
&\mathcal{K}_v^F \cdot \delta v_n + \mathcal{K}_s^F \cdot \delta s_m + \mathcal{K}_v^G \cdot \delta \dot{v_n} + \mathcal{K}_s^G \cdot \delta \dot{s_m} = 0.
\end{aligned} \tag{5}$$

Therefore, we have the following matrix form for linearized system equation with all Jacobian matrices $(\mathcal{G}, \mathcal{C}, L_l, \mathcal{S}, \mathcal{K}_v^F, \mathcal{K}_s^F, \mathcal{K}_v^G, \mathcal{K}_s^G)$ and incident matrices (E_c, E_g, E_l, E_i):

$$\begin{aligned}
&\begin{bmatrix} \mathcal{G} & E_i & E_l & \mathcal{S} \\ -E_i & 0 & 0 & 0 \\ -E_l & 0 & 0 & 0 \\ \mathcal{K}_v^F & 0 & 0 & \mathcal{K}_s^F \end{bmatrix} \begin{pmatrix} \delta v_n \\ \delta j_i \\ \delta j_l \\ \delta s_m \end{pmatrix} \\
&\quad + \begin{bmatrix} \mathcal{C} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & L_l & 0 \\ \mathcal{K}_v^G & 0 & 0 & \mathcal{K}_s^G \end{bmatrix} \begin{pmatrix} \delta \dot{v_n} \\ \delta \dot{j_i} \\ \delta \dot{j_l} \\ \delta \dot{s_m} \end{pmatrix} \\
&\quad = -\mathcal{F}(X_0, \dot{X}_0, t).
\end{aligned} \tag{6}$$

Note that both large-signal and small-signal system equations can be obtained when introducing internal state variables. Its implementation for NVM devices is shown in the following section.

III. Internal State Variable of NVM Devices

In this section, the internal state variables are identified from the dynamic operation of memristor, STT-MTJ and PCM devices separately. Then the application of new NMA is derived for each device in the SPICE-like simulator based on the modified nodal analysis in Section II. All the variables used in this section are summarized in Table II for memristor, Table III for STT-MTJ and Table IV for PCM, respectively.

A. Memristor Device

The existence of memristor was first predicted by Chua in 1976 [13], but not until nearly 30 years later was it first discovered in nano-scale devices in HP lab [15]. A typical structure of memristor is illustrated in Fig. 2(a) with doping and undoping regions. The term doping ratio (w) is introduced to numerically

TABLE III
DEFINITIONS OF VARIABLES USED FOR STT-MTJ DEVICE

Variables	Definitions
θ and ϕ	azimuthal angles of magnetization orientation in x-y and y-z plane. (state variables)
R_H, R_L	resistance values of anti-parallel state and parallel state
ΔR_{GMR}	difference between R_H and R_L
α	damping constant
e	charge of electron
A	area of STT-MTJ cross-section
l_m	thickness of oxide barrier
H, H_k	applied field and effective anisotropy field
M_s	saturation magnetization of material
η	spin transfer efficiency
$\hbar$	reduced planck constant
m, h	normalized magnetization and effective magnetic field
M	magnetization
τ	normalized time, $\tau = \gamma_0 Ms \cdot t$
Δ	thermal stability factor
τ_0	inverse of attempt frequency (~1ns)
I_c	critical current of spin torque transfer

TABLE IV
DEFINITIONS OF VARIABLES USED FOR PCM DEVICE

Variables	Definitions
T_M	active region temperature of chalcogenide material
K_0	frequency factor
K_B	Boltzmann' constant
E_a	activation energy
T_m	melt temperature
T_X	crystallization temperature
n	Avrami exponent

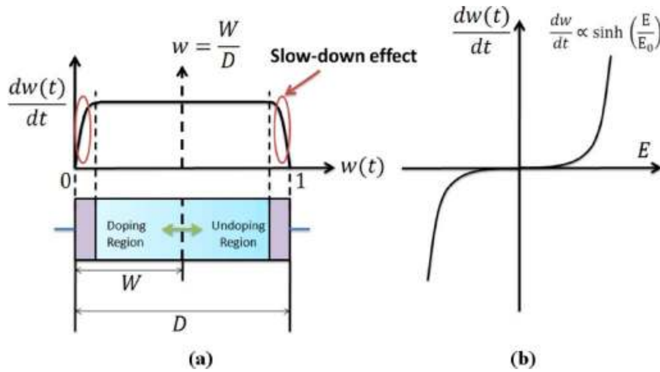

Fig. 2. Structure of memristor and nonlinear effects for dynamic model: (a) slow-down effect at boundary; (b) exponential relation between drift velocity and electric field.

represent the ratio of doping region (W) over the whole thickness of memristor film (D). As there is a large difference of resistivity in doping and undoping regions, the total resistance is changing with doping ratio. For instance, when $w = 1$ the memristor is at ON-state, where the resistance is a thousand times smaller than the resistance at OFF-state with $w = 0$.

The operating principle of memristor device can be summarized as: charge induced state (doping-ratio w) shifting. For instance, when the positive charge flows towards the right-hand side of memristor junction shown in Fig. 2(a), the doping ratio (w) increases and the resistance reduces accordingly, and vice-verse for the charge flowing in the reverse direction. Traditionally, this mechanism can be described as generalized current-controlled memristive system [13] with the following equations:

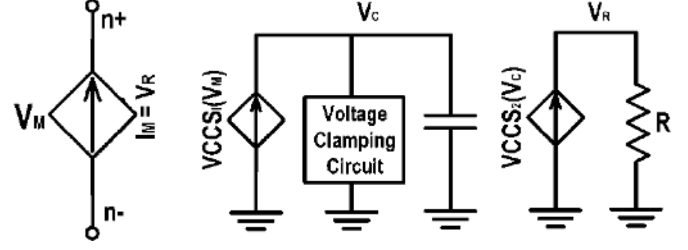

Fig. 3. Equivalent circuit of memristor model in [10].

$$v(t) = \mathcal{R}(w, v)i(t)$$
$$\frac{dw(t)}{dt} = f(w, v) \tag{7}$$

where $\mathcal{R}$ is the resistance of memristor and f is the explicit function of w and applied voltage v; dw/dt is the normalized drift velocity determined by w and external voltage v. Note that the complementary current-controlled memristive system can be defined similarly. We can easily see from (7) that, other than the voltage v and the current i, the complete status of memristor is also dependent on the doping-ratio w. Therefore, w is identified as the internal state variable for memristor.

The dynamic effect relevant to doping-factor w can be found in details from Appendix A. Considering charge-induced-drifting effect, slow-down effect and strong-electric-field effect as shown in Fig. 2(b), we can obtain a complete nonlinear dynamic memristor model from (10), (11) and (13):

$$\frac{v(t)}{i(t)} = R_{\text{off}} - (R_{\text{off}} - R_{\text{on}})w(t)$$
$$\frac{dw(t)}{dt} = \frac{\mu E_0}{D} \sin h\left(\frac{v(t)}{DE_0}\right) F(w(t)). \tag{8}$$

Equation (8) can be used to link internal state variable $w(t)$ with the external state variables (nodal voltage and branch current). Accordingly, we can effectively determine the memductance of memristor when all state variables are determined.

Previous approaches by equivalent circuit [10], [16] require the use of many additional circuit components to capture dynamics and hence lead to large complexity for large-scale circuit simulation. For instance as depicted in Fig. 3 to implement an equivalent circuit of memristor shown in [10], many circuit components have to be added, including resistor, capacitor, diode and current-controlled-current-source, etc.

In the following, we first define the new state variable vector: $X = [v_n, j_i, j_l, w_m]^T$, and then show how to obtain the Jacobian terms $\mathcal{G}, \mathcal{S}, \mathcal{K}_v^F, \mathcal{K}_s^F, \mathcal{K}_v^G$ and $\mathcal{K}_s^G$ in (6).

Applying (3) and (4) derived in last section to the memristor dynamic function described in (8), one can obtain the Jacobian terms

$$\mathcal{G} = \begin{bmatrix} G & -G \\ -G & G \end{bmatrix} \quad \mathcal{S} = \begin{bmatrix} v_n \times \frac{dG}{dw_m} \\ -v_n \times \frac{dG}{dw_m} \end{bmatrix} \quad C = 0$$
$$\mathcal{K}_v^F = [-c_1 c_2 F(w_m) \cos h(c_2 v_n) \quad c_1 c_2 F(w_m) \cos h(c_2 v_n)]$$
$$\mathcal{K}_s^F = -c_1 \sin h(c_2 v_n) \times \frac{dF(w_m)}{dw_m}; \quad \mathcal{K}_v^G = 0; \quad \mathcal{K}_s^G = 1$$

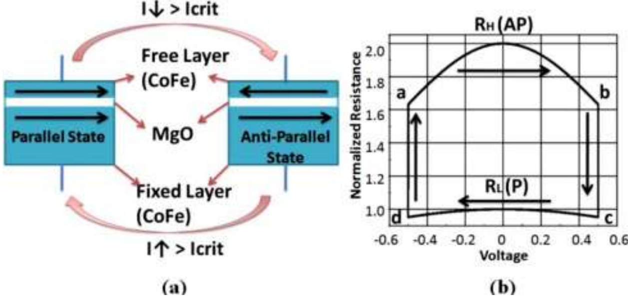

Fig. 4. (a) Typical STT-MTJ structure and state change diagram; and (b) V-R curve of STT-MTJ device.

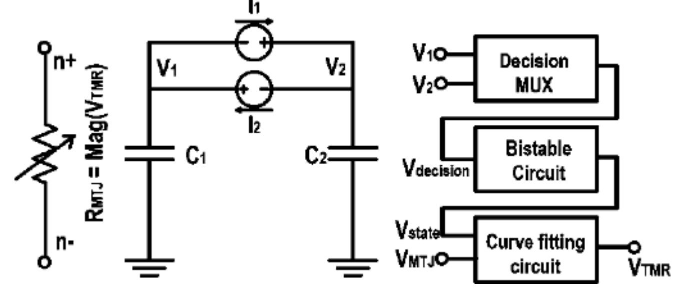

Fig. 5. Simplified equivalent circuit of STT-MTJ model in [9].

where G is the conductance and $(dG)/(dw_m)$ is the internal state variable derivative of conductance, $c_1 = (\mu E_0)/(D), c_2 = (1)/(DE_0)$ are constants, and $F(w)$ is the window function. Recall that the other parameters are defined in Table II.

B. STT-MTJ Device

A typical STT-MTJ device structure appears as a sandwich with two ferromagnetic layers and one oxide barrier in between [11]–[13]. One STT-MTJ device has two stable states: parallel state (P) or anti-parallel state (AP), where the free layer magnetization is in the same or the opposite direction with respect to the hard axis (magnetization direction of fixed layer), respectively. One giant-magneto-resistance (GMR) at AP state (R_H) is higher than the GMR at P state (R_L) [17]. The GMR [18] can be expressed as

$$\begin{aligned} R(\theta) &= R_L + \frac{R_H - R_L}{2}(1 - \cos\theta) \\ &= R_L + \frac{\Delta R_{\mathrm{GMR}}}{2}(1 - \cos\theta). \end{aligned} \tag{9}$$

Note that angle θ is one magnetization angle between free-layer and hard-axis. It can be easily derived that: $R_{\theta=0} = R_L$ at P state and $R_{\theta=\pi} = R_{\mathrm{H}}$ at AP state.

As depicted in Fig. 4, the operating principle of STT-MTJ device can be summarized as: the external current induced state (θ for P or AP) change. STT-MTJ is switched from P to AP with sufficient forward biased current; and from AP to P with sufficient reverse biased current. The detailed dynamic effects required to describe the behavior of STT-MTJ is discussed in Appendix B. As discussed, we choose the azimuthal angles of normalized magnetization (M) of free layer in $x-y$ plane (θ) and $y-z$ plane (ϕ) as internal state variables to describe the dynamic behavior of STT-MTJ device.

Considering the tunneling, spin-transfer-torque effect and arbitrary driving condition, the dynamics of one STT-MTJ device model can be constructed from (9), (14), (17), and (18), linking internal state variables θ and ϕ with the external state variables (nodal voltage and branch current).

Previous approaches by equivalent circuit [7]–[9] require the use of many additional circuit components to capture this dynamics and hence have large overhead for large-scale circuit simulation. For instance as depicted in Fig. 5, to implement an equivalent circuit of STT-MTJ shown in [9], at least ten more circuit elements have to be added, including current-control-current-source, capacitor, decision circuit and curve fitting circuit, etc. As a result, the circuit overhead of equivalent circuit approach can grow as the circuit size increases, which leads to huge amount of computation time.

Similar to memristor device, we can define the new state variable vector $X = [v_n, j_i, j_l, \theta_m, \phi_{\mathrm{m}}]^T$, and then the Jacobian terms $\mathcal{G}, \mathcal{S}, \mathcal{K}_v^F, \mathcal{K}_s^F, \mathcal{K}_v^G$ and $\mathcal{K}_s^G$ in (6) for STT-MTJ.

Applying (3) and (4) derived in Section II to the STT-MTJ dynamic functions described in (9), (14), (17), and (18), we can easily obtain the Jacobian terms required as follows:

$$\mathcal{G} = \begin{bmatrix} \frac{dj_b}{dv_n} & -\frac{dj_b}{dv_n} \\ -\frac{dj_b}{dv_n} & \frac{dj_b}{dv_n} \end{bmatrix} \quad \mathcal{S} = \begin{bmatrix} v_n \times \frac{dG}{d\theta_m} & 0 \\ -v_n \times \frac{dG}{d\theta_m} & 0 \end{bmatrix}$$

$$C = 0$$

$$\mathcal{K}_v^F = \begin{bmatrix} -\frac{df(\phi_m, j_b, t)}{dj_b} \cdot \frac{dj_b}{v_n} & \frac{df(\phi_m, j_b, t)}{dj_b} \cdot \frac{dj_b}{v_n} \\ -\frac{d\omega_m}{dj_b} \cdot \frac{dj_b}{v_n} & \frac{d\omega_m}{dj_b} \cdot \frac{dj_b}{v_n} \end{bmatrix}$$

$$\mathcal{K}_s^F = \begin{bmatrix} 1 & -\frac{df(\phi_m, j_b, t)}{d\phi_m} \\ 0 & 0 \end{bmatrix} \quad \mathcal{K}_v^G = 0$$

$$\mathcal{K}_s^G = \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix}$$

where $(dj_{\mathrm{b}})/(dv_n)$ and $(dG)/(d\theta_m)$ can be derived from (9) and (14), and $(df(\phi_m, j_b, t))/(dj_b), (df(\phi_m, j_b, t))/(d\phi_m)$ and $(d\omega_m)/(dj_b)$ can be derived from (17) and (18), respectively. Note that G is the conductance of STT-MTJ, $\mathcal{S}$ is the memductance of STT-MTJ, $f(\phi_m, j_b, t)$ is the function at the right hand side of (17), and ω_m is the angular movement speed of ϕ_m. Recall that the other parameters are defined in Table III.

C. PCM Device

PCM device is based on the phase-changing technology of chalcogenide materials such as Ge_2SbTe_5 [19], of which the crystal structure can be thermally switched between two different stable states: crystalline and amorphous, and for the same PCM device, the resistance in amorphous state is one thousand times larger than that in crystalline state. Typically, PCM device has a mushroom structure as demonstrated in Fig. 6(a). This structure makes the heat dissipation rate at top surface much higher than that of bottom surface. As such, the thermal activation of phase changing always begins from the bottom side. Note that the resistance of PCM device is mainly determined by the active region shown in Fig. 6(a).

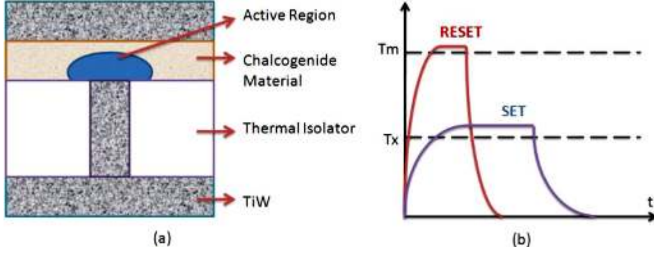

Fig. 6. (a) Typical structure of PCM device and (b) temperature profile of chalcogenide material in SET and REST operations.

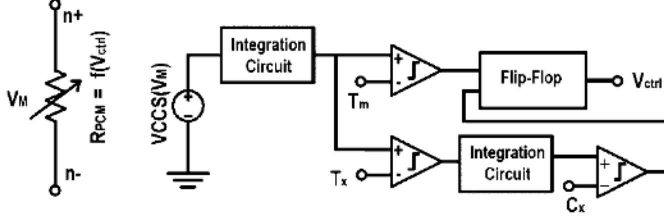

Fig. 7. Simplified equivalent circuit of PCM device in [11].

The operation of PCM device can be summarized as: thermal activated state (crystallizing and amorphousizing) change. As illustrated in Fig. 6(b), a narrow pulse of temperature surge above the melting temperature (T_m) will "RESET" the active region to the amorphous state; and a long pulse of temperature surge between melting temperature (T_m) and crystallization temperature (T_X) will "SET" the active region to the crystalline state. The dynamic effects required to describe the behavior of PCM device is discussed in Appendix C with details. As discussed, we choose crystallization ratio C_X and active region temperature T_M as internal state variables to describe the dynamic behavior of PCM device.

Considering the thermal effect and crystallization kinetics, we can describe dynamics of PCM device with (21), (22) and (23), linking internal state variables T_M and C_X with the external state variables (nodal voltage and branch current).

An equivalent circuit of PCM device [11] is shown in Fig. 7 with dozens of circuit elements required to realize the same dynamics mentioned above. This introduces large overhead for large-scale circuit simulation.

Similar to memristor and STT-MTJ, the new state variable vector is introduced as $X = [v_n, j_i, j_l, C_{X_m}, T_{M_m}]^T$, and the Jacobian terms $\mathcal{G}, \mathcal{S}, \mathcal{K}_v^F, \mathcal{K}_s^F, \mathcal{K}_v^G$ and $\mathcal{K}_s^G$ in (6) for PCM device are then obtained by

$$\mathcal{G} = \begin{bmatrix} G & -G \\ -G & G \end{bmatrix}$$
$$\mathcal{S} = \begin{bmatrix} v_n \times \frac{dG}{dT_{Mm}} & v_n \times \frac{dG}{dC_{Xm}} \\ -v_n \times \frac{dG}{dT_{Mm}} & -v_n \times \frac{dG}{dC_{Xm}} \end{bmatrix} \quad C = 0$$
$$\mathcal{K}_v^F = \begin{bmatrix} -\frac{dh(T_{M_m}, v_n, t)}{dv_b} & \frac{dh(T_{M_m}, v_n, t)}{dv_b} \\ 0 & 0 \end{bmatrix}$$
$$\mathcal{K}_s^F = \begin{bmatrix} 1 & 0 \\ -\frac{dg(T_{M_m}, v_n, t)}{dT_{Mm}} & 1 \end{bmatrix} \quad \mathcal{K}_v^G = 0 \quad \mathcal{K}_s^G = 0,$$

where G is the conductance, and $(dG)/(dT_{Mm}), (dG)/(dC_{Xm})$ are the temperature and crystalline fraction derivatives; $(dh(T_{Mm}, v_n, t))/(dv_b)$ and $(dg(T_{Mm}, v_n, t))/(dT_{Mm})$ are derived from (21) and (22), respectively. Note that $h(T_{Mm}, v_n, t)$ is the function at the right-hand side of (21), and $g(T_{Mm}, v_n, t)$ is the function at the right-hand side of (22). Recall that the other parameters are defined in Table IV.

IV. Numerical Experiment

The SPICE-like transient simulator is implemented in MATLAB to consider both NVM and CMOS devices. With the use of the newly developed SPICE-like simulator considering the internal state variables of NVM devices, a number of numeric experiments are conducted for designs of hybrid CMOS and NVM circuits, mainly large-scale memories. Other than the accurate dynamic models of memristor, STT-MTJ, PCM, and CMOS devices, the SPICE-like simulator also contains the basic circuit elements such as BJT, capacitor, resistor, and voltage/current source. All numerical experiments are conducted on the same work station with Intel Core i5 CPU and 8G RAM. The efficiency of the proposed SPICE-like simulator is demonstrated by experiment results from three perspectives: modeling of NVM devices, capability of hybrid simulation with CMOS and NVM devices, and the scalability of for large-scale memory circuits.

A. Verification of Dynamic NVM Device Model With Internal State Variables

1) Memristor Model Verification: In order to consider the slow-down effect for the drift-velocity near the boundary, Joglekar window function [20] can be introduced for this purpose. The window function implemented in our developed simulator and the corresponding *I-V* curves under one sine-input are plotted in Fig. 8. The device parameters are: $D = 10$ nm, $R_{\text{on}} = 200\,\Omega, R_{\text{off}} = 3800\,\Omega$, the initial memristance $M = 3790\,\Omega, p = 2, \mu = 1 \times 10^{-17}$ m^2/(V·s) and $E_0 = 1$ MV/cm. The dynamic behavior is investigated under the driving voltage of $V(t) = -0.2 + \sin(200\pi t)V$. As shown in Fig. 8, our dynamic model with Joglekar window function can capture the experiment results reported in [15].

Moreover, a Biolek window function [21] is also implemented in our simulator to show the impacts of different dynamic behaviors under different window functions: Biolek window function is asymmetric and Joglekar window function is symmetric. Two memristors with symmetric and asymmetric functions are investigated under sine voltage: $V(t) = 0.5\sin(200\pi t)$. As shown in Fig. 9, the asymmetric Biolek window function forces memristance to shift away from the boundary under the sine input. This has resulted in an oscillation around the center value regardless the initial value of memristor. On the other hand, Joglekar window function cannot show this behavior. Nevertheless, the difference between the symmetric dynamic and the asymmetric dynamic models obviously cannot be observed from a static device model.

2) STT-MTJ Model Verification: In order to validate our STT-MTJ model, the device-level simulation results are compared to the experiment verified modeling results from [22] under the same device parameters. The area of STT-MTJ cross-section is 130×90 nm^2, and the thickness of free layer

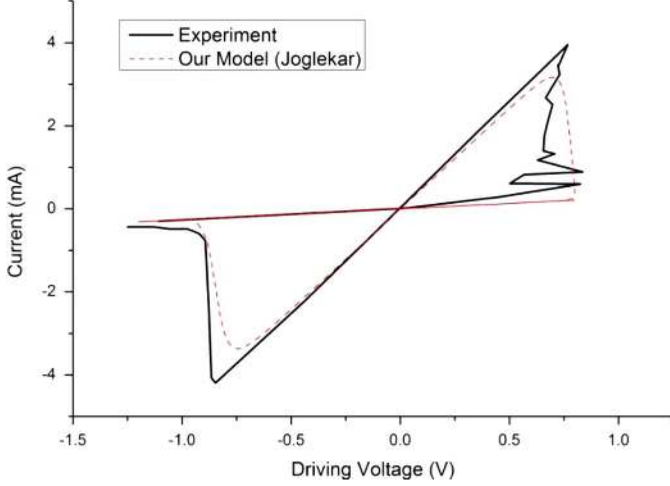

Fig. 8. Memristor device simulation with Joglekar window function: I-V curve, which is consistent to the measured results reported in [15].

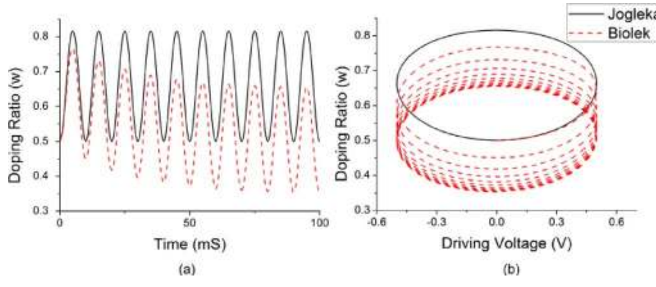

Fig. 9. Dynamic responses of memristor under different window functions Joglekar and Biolek. (a) w-t (doping ratio versus time) curve, and (b) w-v (doping ratio versus input voltage) curve.

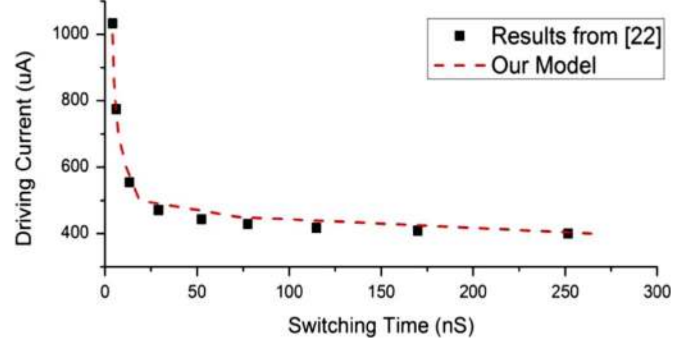

Fig. 10. STT-MTJ device simulation: switching time versus driving current, which is consistent to the measured results reported in [22].

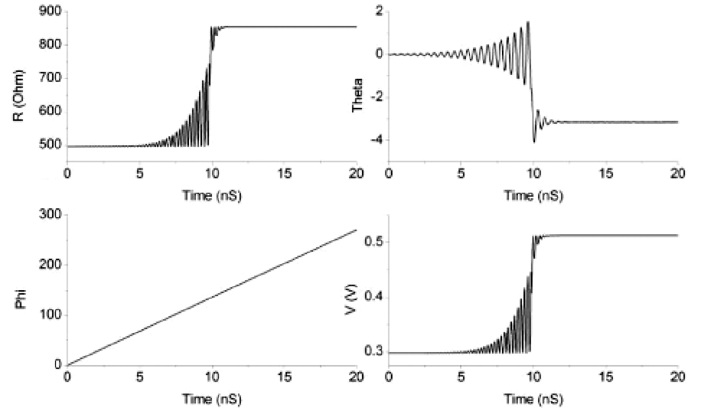

Fig. 11. Dynamic responses of STT-MTJ resistance and state variables under the step constant current induction.

is 2 nm. The saturation magnetization is 1000 emu/cm^3, and the crystal anisotropy is 20Oe. The polarization efficiency is 0.57 with tunnel-magneto-resistance (TMR) around 100%. The damping parameter is 0.005. 500 Ω is assigned as the GMR at P state (R_L). The voltage-dependent tunneling conductance coefficient for P and AP states are set to 0.1 and 0.65 to fit the TMR voltage relationship. The same STT-MTJ model is used in the later experiments as well for consistency.

Fig. 10 shows the free-layer switching time versus STT-MTJ driving current. Our STT-MTJ model fits well with the results reported from [22]. Moreover, we can observe that the switching time increases very fast when the driving current approaches the critical current. As such, a huge current has to be applied when a very short switching time is required.

Under the constant current driving condition, the dynamic behavior of STT-MTJ device can be observed from Fig. 11, which shows the changes of resistance, voltage, and two internal state variables (θ and ϕ) with respect to time. The STT-MTJ is initially at P state which has a smaller GMR (R_L). Upon applying a 600-μA driving current, it is switched to AP state in about 10 ns. ϕ increases continuously with a very high speed according to the large gyromagnetic ratio. At the same time, θ starts to deviate from the original value once the current is applied. Its maximum deviation increases exponentially with time before the reversal happens. Under the constant current condition, the voltage changes with the STT-MTJ resistance simultaneously, of which the fluctuation is observable after 5 ns and jumps to 850 Ω at 10 ns. This fluctuation decays very fast after reversal, and then STT-MTJ enters into the other stable state. Note that these dynamic behaviors of resistance fluctuation cannot be observed under the equivalent circuit-based STT-MTJ model in [9].

3) PCM Model Verification: To further validate the PCM model, the device level simulation results are compared to the experiment results shown in [11] under the same device parameters. The crystallization and melt temperature (T_X and T_m) are 155 °C and 620 °C, respectively. The crystalline state resistance (R_{SET}) is 10 KΩ and the amorphous state resistance (R_{RESET}) is 1 MΩ. We select the activation energy (E_a) to be 2.24 eV for a typical chalcogenide material $\mathrm{Ge_2Sb_2Te_5}$ [19], Avrami exponent (n) is 1.5 and the frequency factor is set to 1.2 e7.

Fig. 12 shows the resulting resistance of PCM device after a 300-ns current pulse, of which the amplitude is changed from 0.1 to 1 mA. We can see that our model fits well with the experiment results reported in [11]. Moreover, we can see the allowable current range for a 300-ns current pulse to change the PCM into crystalline state is between 0.3 and 0.6 mA. Out of this range the PCM remains in the amorphous state.

The dynamic responses of internal state variables: temperature and crystalline fraction of active region under SET and RESET operations are illustrated in Fig. 13. We can see that a 0.3-mA current pulse of 400 ns raises the temperature of active region well above the crystallization temperature

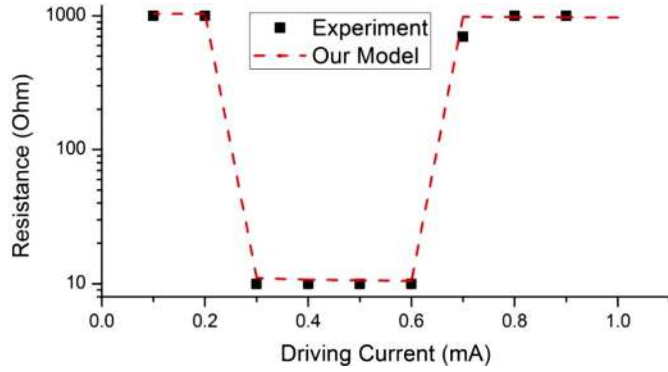

Fig. 12. PCM device simulation: *R-I* curve, which is consistent to the measured results reported in [11].

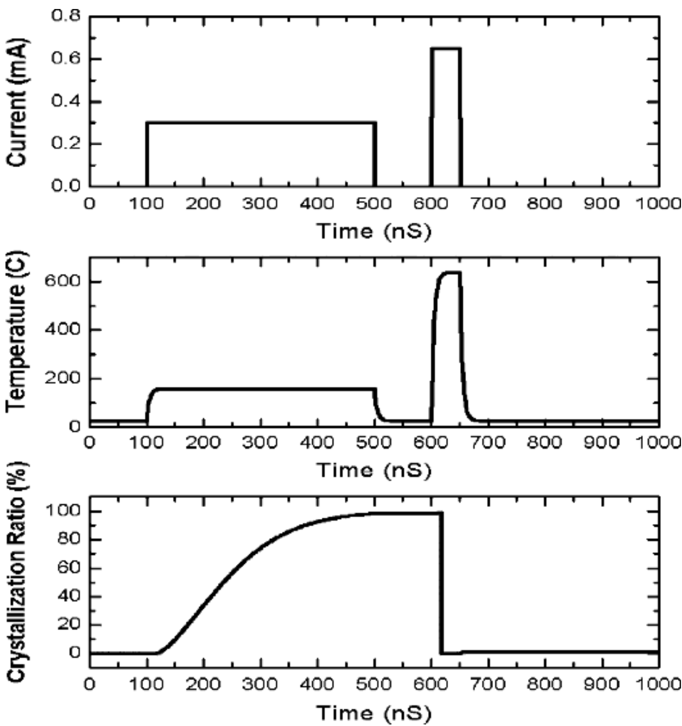

Fig. 13. Dynamic responses of internal state variables of PCM device under current driving SET and RESET operations.

and gradually changes PCM from amorphous to crystalline state. Then a 0.65-mA current pulse of 50-ns increases the temperature of active region higher than the melt temperature of 620 °C, and then changes PCM back to amorphous state. Actually, the storage temperature of PCM device is limited by the crystallization temperature. If the PCM memory is placed in the environment higher than the crystallization temperature, all the data stored will be corrupted.

B. Simulation of Memory Circuits of Hybrid CMOS and NVM Devices

1) Memristor Based Crossbar Memory: We first demonstrate the use of dynamic model of memristor for crossbar-based memory circuit as shown in Fig. 14. Both memory and demux circuits are realized by memristors with different threshold

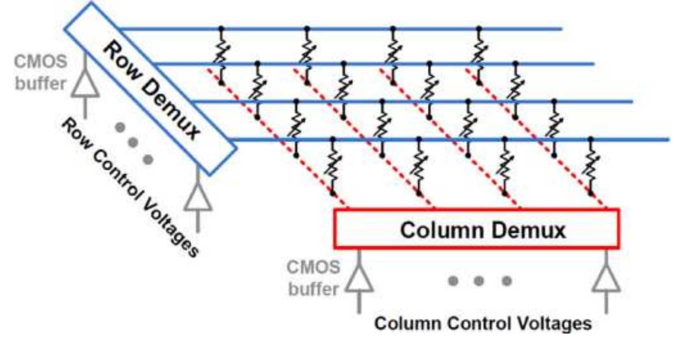

Fig. 14. A 4×4 memristor-based crossbar memory design [3]. Both column and row demuxes are implemented with memristors.

TABLE V
EFFECT OF DRIFT VELOCITY SLOW-DOWN NEAR BOUNDARY ON RISE AND FALL TIME. MODEL-1: STATIC MODEL WITHOUT WINDOW FUNCTION; MODEL-2: BIOLEK DYNAMIC MODEL WITH ASYMMETRIC WINDOW FUNCTION; AND MODEL-3: JOGLEKAR DYNAMIC MODEL WITH SYMMETRIC WINDOW FUNCTION

Window function type	Window function	p	Rise time (ns)	Fall time (ns)
Model-1	NA	NA	6.02	4.36
Model-2	f(x)=1-[x-u(-I)]^{2p}	2	6.75 (12%)	8.22 (89%)
		7	6.08 (1%)	4.85 (11%)
Model-3	f(x)=1-(2x-1)^{2p}	2	7.39 (23%)	7.5 (72%)
		7	6.14 (2%)	6.25 (43%)

voltages, and CMOS buffers are used to generate control signals.

Due to the slow-down effect of drift velocity near the boundary considered by the window function, the simulated access-time for a "Write"-operation is longer than the static model without the consideration of the window function. Recall the internal state variable here is doping-ratio (w). The two window functions by Joglekar model and Biolek model are compared with the static model in Table V. Up to 23% increase in rise-time (t_r) and 88.5% increase in fall-time (t_f) are observed (here rise/fall time is defined as time for w to change between the range of 5% and 95%).

Moreover, recall the strong-electric-field effect discussed in Appendix A. In HP's crossbar memory design [3], this relation is approximated by introducing the threshold voltage in the static model. However, in practice, there is an unclear cutoff for the formulation of the threshold region. The $sinh$ based relation is usually deployed for this purpose. In this realistic model, voltages below the threshold value can still cause small shift for the memristance, which can accumulate and eventually leads to an error such as "false-write" state, and hence can significantly affect the reliability for the memory design. To demonstrate this undesired dynamic result, a 4×4 crossbar memory is deployed here under a "Write-1"-operation. The driving voltage to the targeted memristor is 3 V while the applied voltages for the remaining memristors are only 1 V. The proposed dynamic model with Biolek's window function $(p = 7)$ is used. Here, we define the "error-free write time" $(t_{\rm ef})$ as the total time required for the first "false-write" to happen, when one non-targeted memristor is unintentionally shifted across its middle resistance. And "error-free write cycle" $(t_{\rm ef}/t_r)$ is defined as the

TABLE VI
EFFECT OF DYNAMIC MODEL PARAMETERS ON RISE TIME AND ERROR-FREE WRITE TIME AND ERROR-FREE WRITE CYCLE FOR MEMORY WRITE OPERATION

$\frac{1}{D}(nm^{-1})$	Rise time (t_r, ns)	Error-free write time (t_{ef}, ns)	Error-free write cycle (t_{ef}/t_r)
0.1	474	2134	4
0.15	70.6	786	11
0.2	11.8	346	29
0.25	2.1	166	78
0.3	0.4	83.7	211

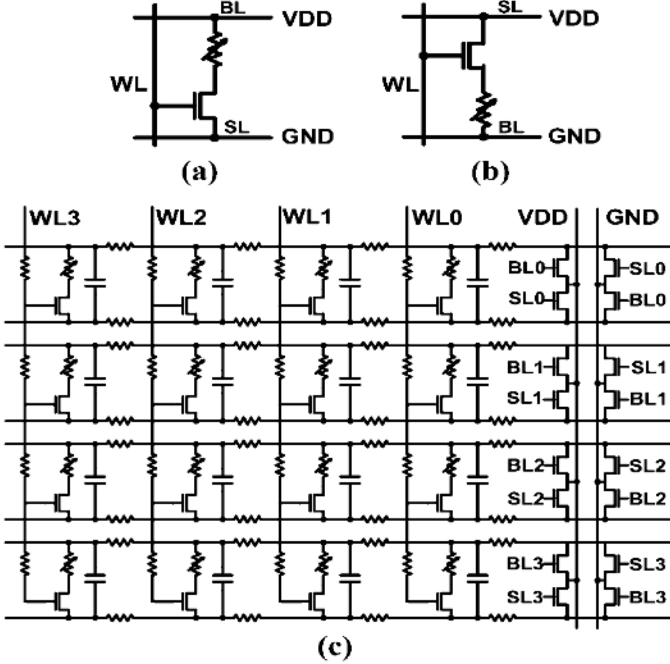

Fig. 15. Circuit diagrams of STT-MTJ memory cell: (a) simplified memory cell for write-1; (b) simplified memory cell for write-0; and (c) 16-bit STT-MTJ MRAM with 4 bit-lines and 4 word-lines.

number of write operation allowed in this period. Dynamic modeling parameter $(1)/(D)$ (inverse of film thickness) in (10) is swept from 0.1 to 0.3 nm^{-1}, while μ and E_0 are kept the same. As shown in Table VI, although the rise time and the error-free write time both reduces with the film thickness, the number of error-free write cycle increases from 4 to 211. A detailed analysis shows a logarithm relationship between error-free write cycle and the inverse of film thickness: $(1)/(D)$. Therefore, in order to increase the reliability, memristors need to have smaller D.

2) STT-MTJ Based Memory: We further investigate the STT-MTJ dynamic behavior in the design of STT-MTJ based nonvolatile memory. A typical hybrid CMOS and STT-MTJ MRAM cell is shown in Fig. 15(a). In the "Write-1"-operation, WL is connected to VDD, and BL and SL are connected to VDD and GND, respectively. In the "Write-0"-operation shown in Fig. 15(b), the polarities of SL and BL line are interchanged. One NMOS is included to simulate the actual operation of STT-MTJ based memory cell. Here we choose VDD to be 1.2 V as a common biasing for 65-nm process for CMOS devices.

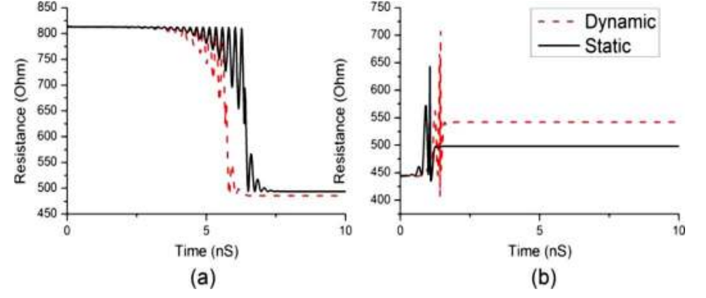

Fig. 16. Comparison between the dynamic model and static model for designs of STT-MTJ based memory: (a) under write-0 and (b) under write-1.

The dynamic model of STT-MTJ with NMOS is compared with the static model driving by constant current in the switching time of "write-1" operation. Note that the switching time with static model can also be obtained from (15). From the simulation results shown in Fig. 16, we can see that the switching time obtained by the static model with constant current [8] is over estimated for the change: AP to P, and is also under estimated for the change: P to AP. This is because the actual driving condition of STT-MTJ in NVM application is constant voltage instead of constant current. We can also observe that the actual switching time of "Write-1"-operation is $3\times$ smaller than that of the "Write-0"-operation. As such, the writing-pulse-width for 0 and 1 is not necessarily to be the same. Moreover, because the voltage is more than 1 V across the STT-MTJ device, the resistance stays at 550 Ω after reversal from P to AP, and it will go back to 1000 Ω once the applied voltage is removed.

3) PCM Based Memory: We also investigate the design of multilevel memory design based on PCM device similar to [11]. Note that the crystallization ratio increases with the time during SET-operation. As such, the resulting crystallization ratio is different with different pulse width. Therefore, it leads to different resistance levels in the same PCM to represent more than one bit of information. A 3-bit (8-resistance levels) memory design is used in this paper.

A simplified 4×4 PCM memory circuit shown in Fig. 17 is implemented in our simulator to demonstrate the multilevel storage with the use of our dynamic PCM device model. The current sources shown are only used for SET-operation. They are applied to drive the PCM devices once the controlling gates are triggered by the incoming pulses. The driving current is 0.3 mA and the different pulse widths selected are 22, 30, 40, 58, 88, 140, and 250 ns for different resistance levels (R_{1-7}) other than R_{RESET}.

The dynamic responses of crystallization ratio and temperature are shown in Fig. 18. We can see that a longer temperature pulse width pushes crystallization ratio to a higher level, which will result in a lower resistance level of PCM device. Table VII presents the resulting resistance levels for different SET-pulses. Note that R_7 obtained from a SET-pulse of 250 ns is already very close to the $\mathrm{R}_{\mathrm{SET}}$ value, which means 85% crystallization ratio is sufficient to SET a PCM device and not necessarily to be 100%.

We also implement the Kt^n function [11] in our simulator to further compare the dynamic crystallization processes modeled

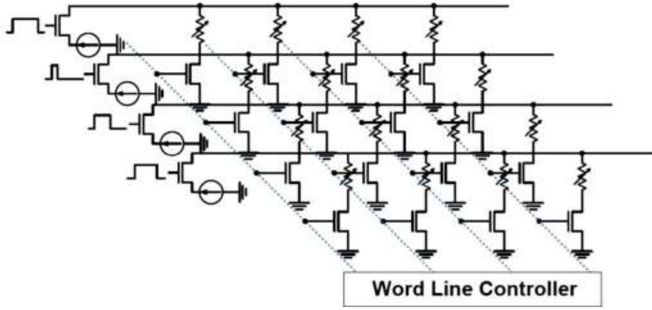

Fig. 17. Circuit diagrams of PCM memory cell in the application of multilevel storage.

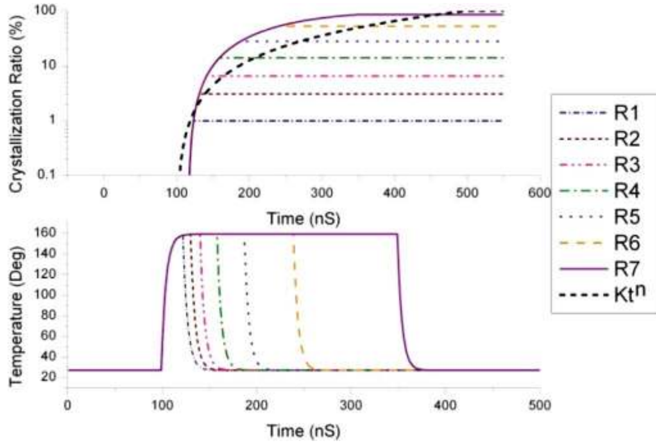

Fig. 18. Comparison between the dynamic model (JMAK) and Kt^n model in [11] for designs of PCM based memory: crystallization ratio and temperature for multilevel memory storage under SET-operation.

TABLE VII
STORAGE LEVELS CORRESPONDING TO DIFFERENT SET-PULSE-WIDTHS AND DIFFERENT RESULTING CRYSTALLIZATION RATIOS

Storage Level	Crystallization Ratio (%)	Resistance (KOhm)	Pulse Width (ns)	
			JMAK (Our dynamic model)	Kt^n[11]
R_{RESET}	0	1K	-	-
R_1	0.98	528	22	20
R_2	3.0	259	30	40
R_3	6.4	141	40	65
R_4	13.9	70.2	58	108
R_5	27.8	36.5	88	170
R_6	52.1	19.8	140	260
R_7	85.2	12.2	250	360

by the JMAK function [23] in our model. The crystallization curve is also shown in Fig. 18. Note that $K = 1.25 \times 10^{-4}$ is a fitting parameter and the Avrami exponent $n = 1.5$ is the same as our JMAK model. We can see that the crystallization process of Kt^n function is faster than the JMAK function in the beginning of SET-pulse-width (25 ns) and becomes slower afterwards. As such, the Kt^n function that ignores the dynamic effect overestimates the dynamic effect, and has different resistance levels (R_{2-7}) as shown in Table VII. This further affects the PCM memory design specifications.

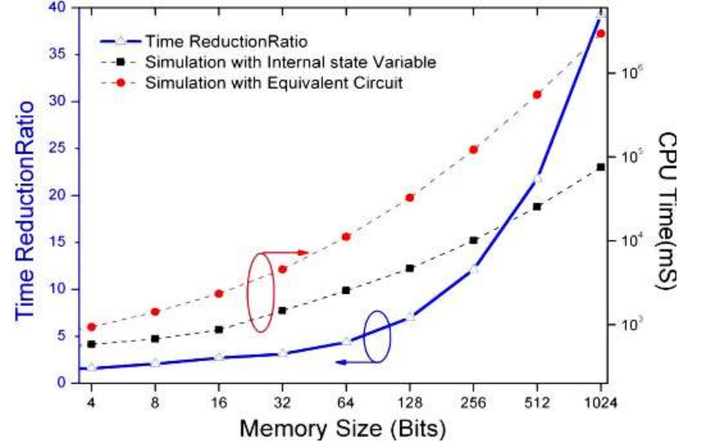

Fig. 19. CPU runtime comparison between our method and equivalent circuit-based model [10] for memristor.

C. Runtime Scalability Comparison

Finally, we evaluate the simulation efficiency of our developed simulator for NVM devices with dynamic models and internal state variable. The runtime scalability study is performed on size (bit) scaled memory designs with transient simulation of 10 time steps. Note that the equivalent circuits of memristor [10], STT-MTJ [9] and PCM [11] are also built in our SPICE-like simulator.

The CPU runtime comparisons are shown in Figs. 19, 20 and 21 for memristor, STT-MTJ, and PCM device, respectively. For a 4-bit memory simulation, the CPU time of our internal state variable based simulation is only half of equivalent circuit-based approach for all three devices. Note that the time reduction ratio obtained from experiment largely depends on the complexity of equivalent circuit and the memory circuit under study. With the increasing size of memory, the overall netlist complexity of equivalent circuit approach grows much faster than our approach. As such, this time reduction keeps increasing with the enlarged size of memory. For a 512-bit memory, compared to the equivalent circuit based simulation, the CPU time of our internal state variable-based simulation is 22 times smaller for memristor, 20 times smaller for STT-MTJ device, and 69 times smaller for PCM device.

V. CONCLUSION

In order to consider the nonlinear dynamic behavior of non-volatile memory (NVM) devices at nano-scale, internal state variables such as doping-ratio, magnetization orientation and crystallization ratio, active region temperature have been identified for memristor, STT-MTJ, and PCM devices, respectively. The corresponding modified nodal analysis considering internal state variables is developed inside one SPICE-like simulator to stamp all three NVM devices compactly together with CMOS devices. As such, one can perform efficient transient simulation for the design of large-scale memory circuits of hybrid CMOS and NVM devices. The experiment results show that our proposed method can accurately and efficiently simulate hybrid NVM circuits with up to 69 times CPU runtime speedup, when compared to the approaches using equivalent circuit models.

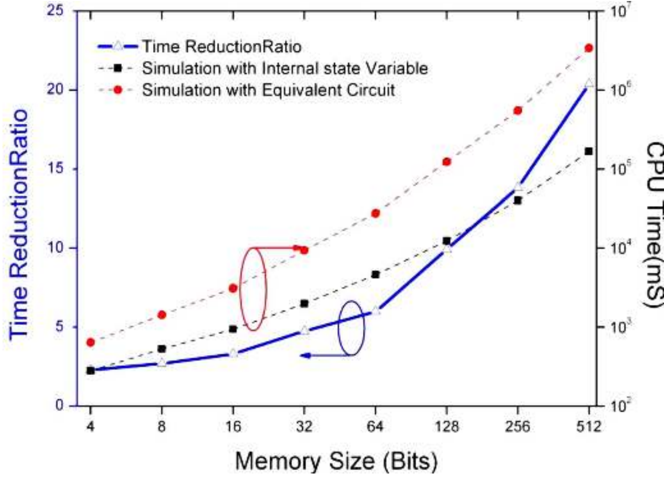

Fig. 20. CPU runtime comparison between our method and equivalent circuit-based model [9] for STT-MTJ device.

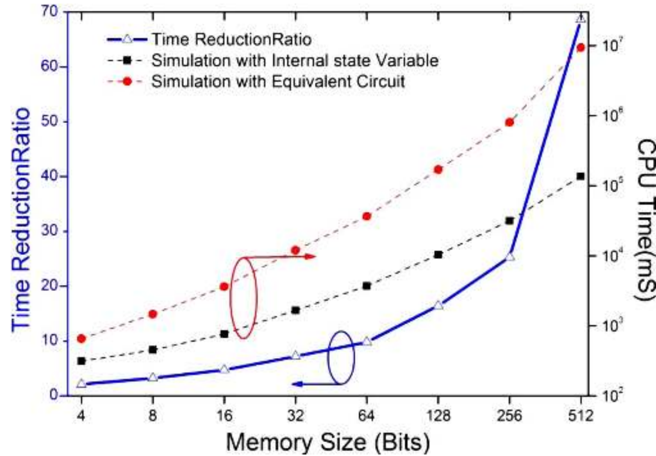

Fig. 21. CPU runtime comparison between our method and equivalent circuit-based model [11] for PCM device.

In addition, the nonlinear dynamic behaviors of NVM devices have shown significant impact on the performance.

Appendix A
Dynamic Effect of Memristor

To fully describe the dynamic behavior of memristor, we need to consider several nonlinear effects of memristive system including: charge-induced-drifting effect, slow-down effect and strong-electric-field effect [15], [20], [21], [24].

As we have mentioned earlier, the basic operation principle of memristor is the charge-induced-shifting of doping level, which means the drifting velocity of memristor is a function of applied current. Together with the relationship between doping-ratio and memductance $\mathcal{R}$ [15], (7) has the following piecewise linear form:

$$v(t) = \left(R_{\mathrm{on}} w(t) + R_{\mathrm{off}}(1 - w(t))\right) i(t),$$
$$\frac{dw(t)}{dt} = \begin{cases} \mu_v \frac{R_{\mathrm{on}}}{D^2} i(t), & \text{mode } 1: \text{ normal operation} \\ 0, & \text{mode } 2: w = 0 \text{ or } 1 \\ 0, & \text{mode } 3: |v| < V_{\mathrm{th}} \end{cases} \tag{10}$$

where V_{th} is the threshold voltage for memory operations.

Moreover, slow-down effect of memristor is illustrated in Fig. 2(a), when w is approaching the boundaries where $w = 0$ or 1, the drift velocity drops quickly and is no longer a linear with the current applied [25]. This nonlinear dynamic effect can be characterized by either of the following window functions [20], [21]:

$$F(w) = 1 - (2w - 1)^{2p} \tag{11}$$
$$F(w) = 1 - \left[(w - u(-i(t)))^{2p}\right] \tag{12}$$

where $p \in [0, 10]$ is a fitting parameter and $u(-i(t))$ equals to 1 when $i(t)$ is positive, and equals to 0 when $i(t)$ is negative. Note that the (11) is a symmetric window function, called Joglekar model [20]; while (12) is an asymmetric window function, called Biolek model [21].

In addition, strong-electric-field effect stands for the exponentially increase in the drift velocity under a strong electrical filed condition (>1 MV/cm). It usually happens in the nanoscale devices such as newly fabricated memristor [26] at scale of 20 nm. As illustrated in Fig. 2(b), the phenomenon can be approximated by a $\sin h$ function [24]:

$$\frac{dw(t)}{dt} = \frac{\mu E_0}{D} \sin h\left(\frac{E}{E_0}\right) \tag{13}$$

where $E = (v(t))/(D)$ is the applied field strength, and definitions of remaining variables are shown in Table II.

Appendix B
Dynamic Effect of STT-MTJ

Memory cell-based dynamic modeling with 1T1J structure (one transistor and one STT-MTJ) is proposed in [27]. However, to further make the STT-MTJ model usable at arbitrary circuit environment, we need to find the dynamic model of STT-MTJ separately. In order to model the operation mechanism of STT-MTJ device accurately, we need to look into two dominant dynamic effects: tunneling effect [28], and spin-transfer-torque effect [29].

Tunneling effect of STT-MTJ can be understood as a parabolic relationship between the junction conductance and the applied voltage [28]. This relationship is illustrated by line segments "ab" and "cd" in Fig. 4(b), which represents the change of normalized resistances with voltage at P and AP states, respectively. Tunneling effect normally becomes dominant when the applied voltage is relatively small such that it will not trigger the STT-MTJ to change state. This relation can be approximated by

$$R_L(V) = \frac{R_L(V=0)}{1 + k_a V^2}; \quad R_H(V) = \frac{R_H(V=0)}{1 + k_b V^2} \tag{14}$$

where $\mathrm{k_a}$ and $\mathrm{k_b}$ are voltage-dependent coefficients for parallel (P) state and anti-parallel (AP) state, respectively.

Moreover, spin-transfer-torque effect becomes dominant when the current flowing through the STT-MTJ is larger than the critical value (I_c). This relationship is illustrated by line segments "bc" and "da" in Fig. 4(b). When the current at the junction is higher than the critical value (I_c), the resistance

will switch between R_H and R_L regions. This process is called *magnetization reversal*. However, magnetization reversal is not an instantaneous process. The switching time required (T_s) for magnetization reversal decreases exponentially with the current applied (I_0) [8]

$$T_s = \tau_0 \exp\left(\Delta\left(1 - \frac{I_0}{I_c}\right)\right) \tag{15}$$

where $I_c = (2eAal_m M_s(H + H_k + 2\pi M_s))/(\eta\hbar)$, τ_0 is the switching time at $I_0 = I_c$, and the definitions of remaining variables are in Table III.

Note that T_s from (15) is the minimum pulse width requirement for certain I_0. For a particular write-operation in STT-MTJ device based memory, one must make sure that a constant current larger than I_c is applied within a period of T_s.

A better understanding of T_s is important for modeling STT-MTJ devices. This requires the analysis for the dynamic behavior of STT-MTJ device under arbitrary driving condition. The Landau–Lifshiltz–Gilbert equation (LLG) [29] is deployed for this purpose:

$$\frac{dm}{d\tau} = -m \times [h + \chi(m \times p)] + a\left(m \times \frac{dm}{d\tau}\right) \tag{16}$$

where χ is the pre-factor of the spin transfer term, p is the hard axis unit vector, and the definitions of remaining variables are shown in Table III.

The solution of (16) can be interpreted as the change of the normalized magnetization (M) of free layer over time. M can be expressed in spherical coordinates with variables ϕ and β as shown in Fig. 22. θ and ϕ are the azimuthal angles of M in $x-y$ plane and $y-z$ plane, respectively, and β is the elevation angle of M from $x-y$ plane. Note that for a very thin free layer, the value of β is rather small and will not affect the modeling of STT-MTJ device. So only θ and ϕ are associated with the state of STT-MTJ devices to describe the normalized magnetization direction. Note that θ and ϕ are calculated by [29]

$$\theta = \theta_0 \text{Exp}\left(-\frac{t}{t_0}\right) \cdot \cos(\phi), \tag{17}$$

$$\omega = \frac{d\phi}{dt} = k_c\sqrt{k_d - (\chi_{\text{crit}} - k_e I)^2} \tag{18}$$

where θ_0 is the initial value of θ, which is slightly tilted from P or AP directions; t_0 is procession time constant; and ω is the angular speed of ϕ; $k_c = \gamma_0 \cdot Ms$ is product of gyromagnetic ratio and saturation magnetization; $k_d \approx (H_k)/(M_s)$ is a function of anisotropy and applied field; χ_{crit} is the critical pre-factor of spin transfer term, which is around half of the damping constant a; k_e is the ratio between pre-factor of the spin transfer term and driving current. Definitions of remaining variables are shown in Table III.

Appendix C
Dynamic Effect of PCM

Two dominant effects have to be considered to describe the dynamic behavior of PCM effects: thermal effect and crystallization kinetics [23].

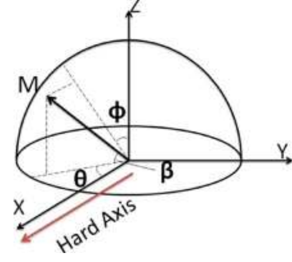

Fig. 22. STT-MTJ magnetization of free layer in spherical coordinates with three magnetization angles: $\boldsymbol{\theta}, \boldsymbol{\phi}$ and $\boldsymbol{\beta}$.

Thermal effect can be subdivided into two different processes: heat generation and heat dissipation. The heat generation power is mainly contributed by Joule heat, which can be represented as

$$W_j = I_M \times V_M \tag{19}$$

where I_M and V_M are current and voltage of one PCM device. The Joule heat generated will be dissipated through the surrounding media of active region. The heat dissipation power can be simplified as

$$W_d = k_e \cdot \nabla T \tag{20}$$

where k_e is the effective thermal conductivity of surrounding material and ∇T is the temperature gradient between active region and ambient environment. As such, the temperature of active region (T_M) will increase when $W_j > W_d$; and will decrease when $W_j > W_d$. This state of thermal effect can be represented by an integration function of the generated net-heat:

$$T_M = \int \frac{W_j - W_d}{C \cdot V}\, dt \tag{21}$$

where C is the specific thermal capacity and V is the volume of active region.

Moreover, crystallization kinetics is actuated when the temperature of active region is above crystallization temperature (T_X). Such a state change can be described by the Johnson–Mehl–Avrami–Kolmogorov (JMAK) equations [23]

$$C_X = 1 - \exp(-Kt^n)$$
$$K = K_0 \exp\left(\frac{-E_a}{K_B T_M}\right) \tag{22}$$

where C_X is the crystallization ratio, $n \in [1, 4]$ is the Avrami exponent, and K is the effective crystallization rate determined by the temperature of active region (T_M). The definitions of remaining parameters are given in Table IV.

When the temperature of active region is higher than T_m, the chalcogenide material melts in the active region, and C_X is reset to zero. As such, the total active region resistance of PCM device (R_M) can be approximated as a function of C_X:

$$\begin{cases} \frac{1}{R_M} = \frac{C_X}{R_{\text{SET}}} + \frac{1-C_X}{R_{\text{RESET}}}, & \text{when } V_M < V_{\text{th}} \\ R_M = R_B, & \text{when } V_M \geq V_{\text{th}} \end{cases} \tag{23}$$

where R_{SET} and R_{RESET} are the PCM device resistance at crystalline and amorphous state, respectively. V_{th} is the

breakdown threshold voltage and R_B is the break-down-state resistance.

ACKNOWLEDGMENT

The authors would like to thank the reviewers, who spent effort in reviewing and made great suggestions for the improvement of this work.

REFERENCES

[1] W. Xu *et al.*, "Improving STT MRAM storage density through smaller-than-worst-case transistor sizing," in *Proc. 46th ACM/IEEE Design Automat. Conf.*, 2009, pp. 87–90.

[2] F. Bedeschi *et al.*, "A bipolar-selected phase change memory featuring multi-level cell storage," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 217–227, Jan. 2009.

[3] P. Vontobel, "Writing to and reading from a nano-scale crossbar memory based on memristors," *Nanotechnology*, vol. 20, p. 425204, 2009.

[4] S. C. Oh *et al.*, "On-axis scheme and novel MTJ structure for sub-30 nm Gb density STT-MRAM," in *Proc. IEEE Int. Electron. Devices Meeting*, 2010, pp. 12.6.1–12.6.4.

[5] G.-Y. Jung *et al.*, "Circuit fabrication at 17 nm half-pitch by nanoimprint lithography," *Nano Lett.*, vol. 6, pp. 351–354, 2006.

[6] J. U. Knickerbocker *et al.*, "3-D silicon integration and silicon packaging technology using silicon through-vias," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1718–1725, Aug. 2006.

[7] A. Kostrov, "SPICE macro-model of magnetic tunnel nanostructure for digital applications and memory cells," in *Proc. 6th Int. Conf. MEMSTECH*, 2010, pp. 31–34.

[8] L. B. Faber *et al.*, "Dynamic compact model of spin-transfer torque based magnetic tunnel junction (MTJ)," in *Proc. 4th Int. Conf. DTIS Nanoscale Era*, 2009, pp. 130–135.

[9] J. D. Harms *et al.*, "SPICE macromodel of spin-torque-transfer-operated magnetic tunnel junctions," *IEEE Trans. Electron. Devices*, vol. 57, no. 6, pp. 1425–1430, Jun. 2010.

[10] S. H. Shin *et al.*, "Compact models for memristors based on charge-flux constitutive relationships," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 29, no. 4, pp. 590–598, Apr. 2010.

[11] X. Q. Wei *et al.*, "HSPICE macromodel of PCRAM for binary and multilevel storage," *IEEE Trans. Electron. Devices*, vol. 53, no. 1, pp. 56–62, Jan. 2006.

[12] W. Lu *et al.*, "Two-terminal resistive switches (memristors) for memory and logic applications," in *Proc. 16th Asia South Pacific Design Autom. Conf.*, 2011, pp. 217–223.

[13] L. Chua and S. M. Kang, "Memristive devices and systems," *Proc. IEEE*, vol. 64, no. 2, pp. 209–223, Feb. 1976.

[14] L. Chua *et al., Linear and Nonlinear Circuits*. New York: McGraw-Hill, 1987.

[15] D. B. Strukov *et al.*, "The missing memristor found," *Nature*, vol. 453, pp. 80–83, 2008.

[16] Y. P. Ho *et al.*, "Dynamical properties and design analysis for non-volatile memristor memories," *IEEE Trans. Circuits Syst. I*, vol. 58, no. 4, pp. 724–736, Apr. 2011.

[17] P. Grunberg *et al.*, "Layered magnetic structures: Evidence for anti-ferromagnetic coupling of Fe layers across Cr interlayers," *Phys. Rev. Lett.*, vol. 57, p. 2442, 1986.

[18] M. N. Baibich *et al.*, "Giant magnetoresistance of (001)Fe/(001)Cr magnetic superlattices," *Phys. Rev. Lett.*, vol. 61, p. 2472, 1988.

[19] I. Friedrich *et al.*, "Structural transformations of $Ge_2Sb_2Te_5$ films studied by electrical resistance measurements," *J. Appl. Phys.*, vol. 87, p. 4130, 2000.

[20] Y. N. Joglekar and S. J. Wolf, "The elusive memristor: Properties of basic electrical circuits," *Eur. J. Phys.*, vol. 30, p. 661, 2009.

[21] Z. Biolek *et al.*, "SPICE model of memristor with nonlinear dopant drift," *Radioengineering*, vol. 18, pp. 210–214, 2009.

[22] X. Wang *et al.*, "Spin torque induced magnetization switching variations," *IEEE Trans. Magn.*, vol. 45, no. 4, pp. 2038–2041, Apr. 2009.

[23] M. E. McHenry *et al.*, "The kinetics of nanocrystallization and microstructural observations in FINEMET, NANOPERM and HITPERM nanocomposite magnetic materials," *Scripta Mater.*, vol. 48, pp. 881–887, 2003.

[24] D. B. Strukov and R. Williams, "Exponential ionic drift: Fast switching and low volatility of thin-film memristors," *Appl. Phys. A: Mater. Sci. Process.*, vol. 94, pp. 515–519, 2009.

[25] O. Kavehei *et al.*, "The fourth element: Characteristics, modelling and electromagnetic theory of the memristor," in *R. Soc. London Proc. Ser. A*, 2010, vol. 466, pp. 2175–2202.

[26] J. P. Strachan *et al.*, "The switching location of a bipolar memristor: Chemical, thermal and structural mapping," *Nanotechnology*, vol. 22, p. 254015, 2011.

[27] Y. Chen *et al.*, "Design margin exploration of spin-transfer torque RAM (STT-RAM) in scaled technologies," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 18, no. 12, pp. 1724–1734, Dec. 2010.

[28] W. Brinkman, "Tunneling conductance of asymmetrical barriers," *J. Appl. Phys.*, vol. 41, p. 1915, 1970.

[29] M. Stiles and J. Miltat, "Spin-transfer torque and dynamics," in *Spin Dynamics in Confined Magnetic Structures III*. Berlin/Heidelberg, Germany: Springer, 2006, vol. 101, pp. 225–308.

Yang Shang (S'11) received the B.S. and M.S. degrees from the School of Electrical and Electronics Engineering, Nanyang Technological University, Singapore, in 2005 and 2009, respectively. He is currently working towards the Ph.D. degree at the same university.

His research interest includes characterization and design of devices in emerging technologies such as non-volatile-memory, meta-material device, and through-silicon-via.

Wei Fei (S'10) received the B.S. degree from the School of Electrical and Electronics Engineering, Nanyang Technological University, Singapore, in 2007. He is currently working towards the Ph.D. degree in the same university.

His research interests include design and modeling of both nano-scale circuit and millimeter-wave frequency circuit.

Hao Yu (M'06) received the B.S. degree from Fudan University, Shanghai, China, in 1999, and M.S. and Ph.D. degrees from the Electrical Engineering Department, University of California, Los Angeles, in 2007, with major of the integrated circuit and embedded computing.

He was a Senior Research Staff at Berkeley Design Automation (BDA). Since October 2009, he has been an Assistant Professor at the School of Electrical and Electronics Engineering, Nanyang Technological University, Singapore. His primary research interests are 3-D computing system and designs at nano-tera scale. He has 52 major peer-reviewed publications.

Dr. Yu received the Best Paper Award from the ACM Transactions on Design Automation of Electronic Systems (TODAES), Best Paper Award nominations in DAC/ICCAD/ASP-DAC, and the Inventor Award from Semiconductor Research Cooperation (SRC). He is an associate editor and technical program committee member of several journals and conferences.