Analysis and Optimization of Accumulation-Mode Varactor for RF ICs

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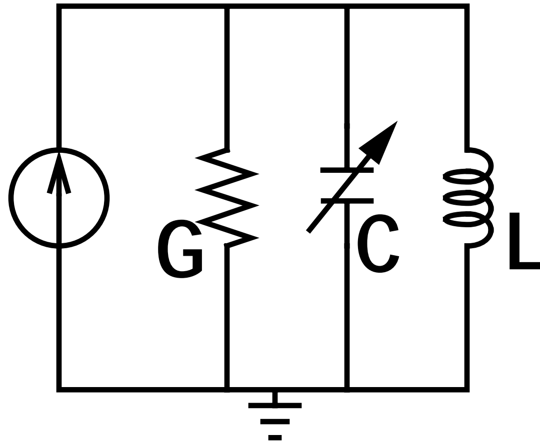
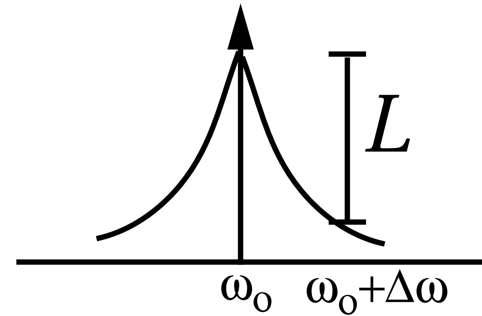
Outline

- Introduction
- Operation
- Characterization
- Optimization
- Conclusion

Phase Noise in VCOs





$$\frac{1}{Q_{tot}} = \frac{1}{Q_L} + \frac{1}{Q_C} + \frac{1}{Q_{ext}}$$

$$L(\Delta\omega) \propto \frac{\omega_o^2}{P_{diss} Q_{tot}^2 (\Delta\omega)^n}$$

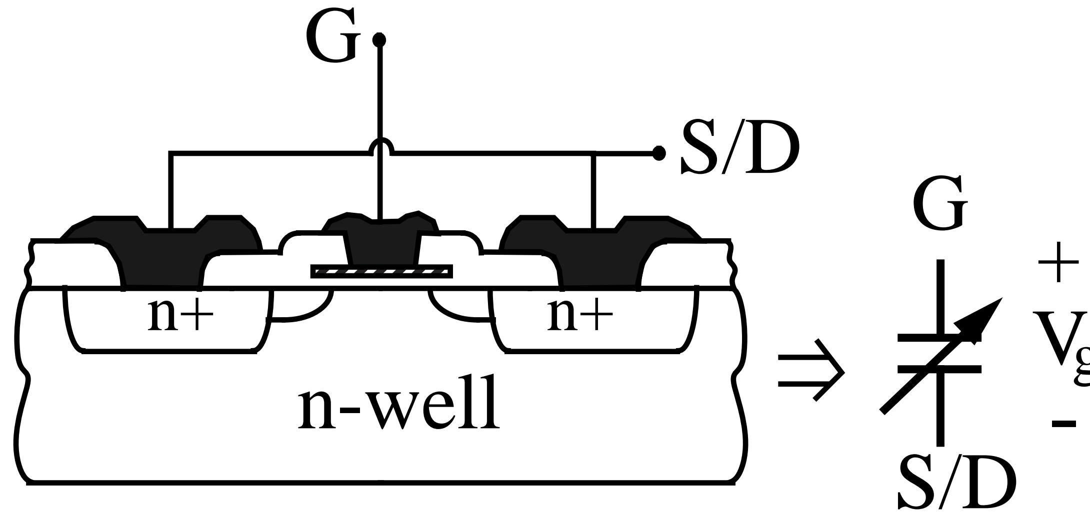
- Q_L ~ 4-8 for 1-10 nH spiral inductor.
- Need Q_C > 40-80 to minimize Q_{tot} degradation.

Conventional IC Varactors

	PN junction	MOS capacitor
Bias	reverse	depletion-inversion
C	moderate (0.4 fF/um^2)*	high (2-7 fF/um^2)
Q	low (5-7 for 1-10 pF)*	moderate (14/GHz/pF)*
Tuning range	small (33%)*	moderate (parasitic S/D junction cap limited)
f_{SR}	4-13 GHz*	8 GHz for 2 pF*
TC	high (200-1000 ppm/C)	moderate (30 ppm/C)

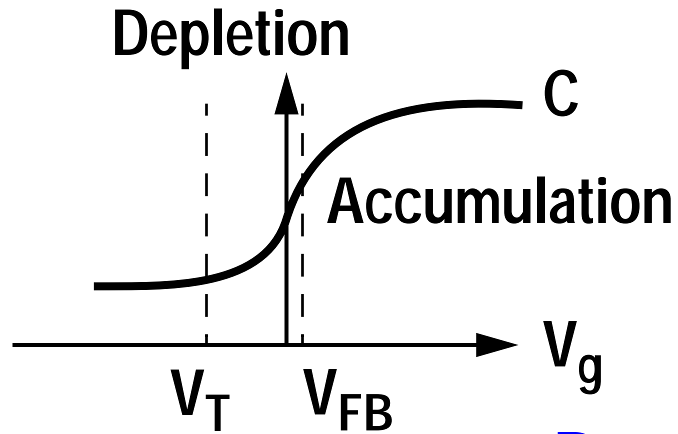
* [Burghartz, et.al., TED '96]

Accumulation-Mode Varactor

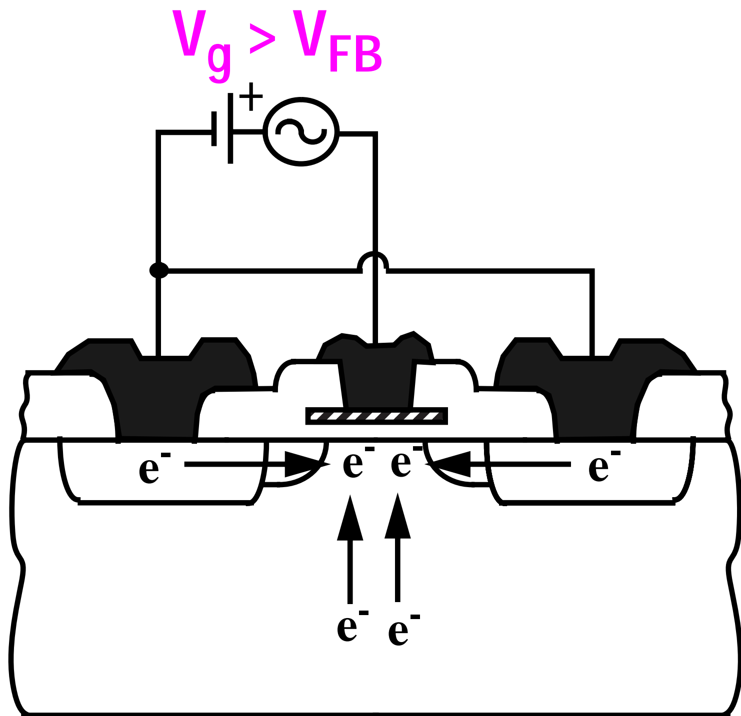


- Standard CMOS process
- Reduce parasitic S/D junction capacitance
- High C per area (increases with technology scaling)
- High Q (increases with technology scaling)
- High tuning range (improves with technology scaling, 200% maximum limit)
- Moderate TC

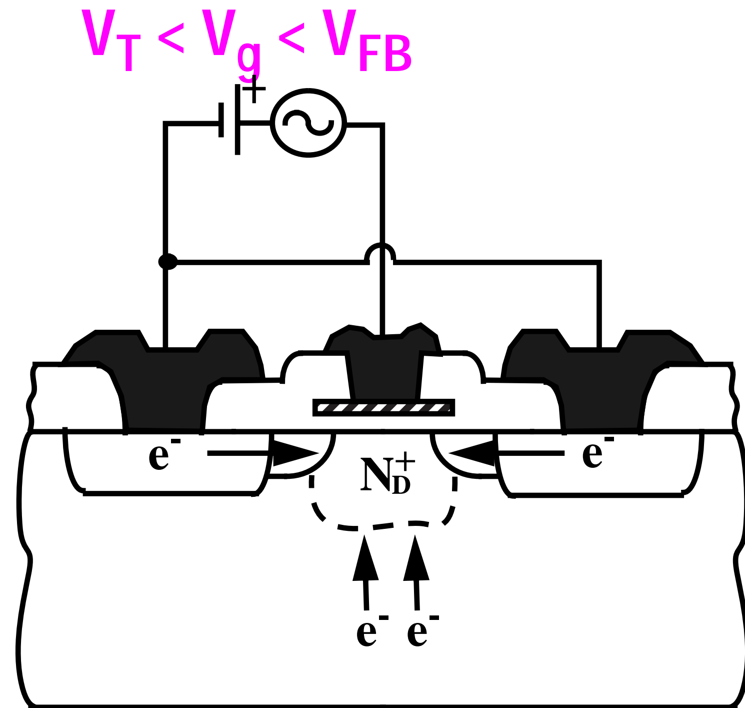
Operating Regimes



Accumulation



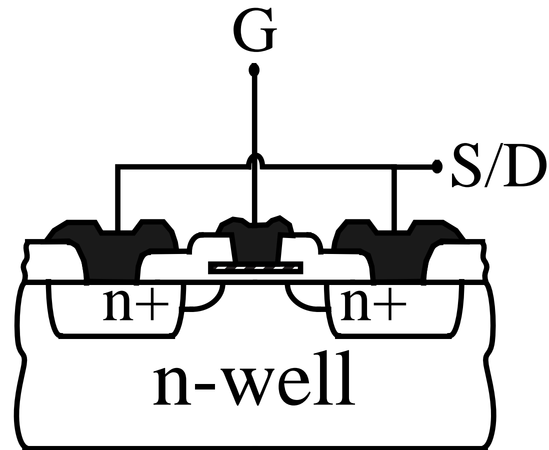
Depletion

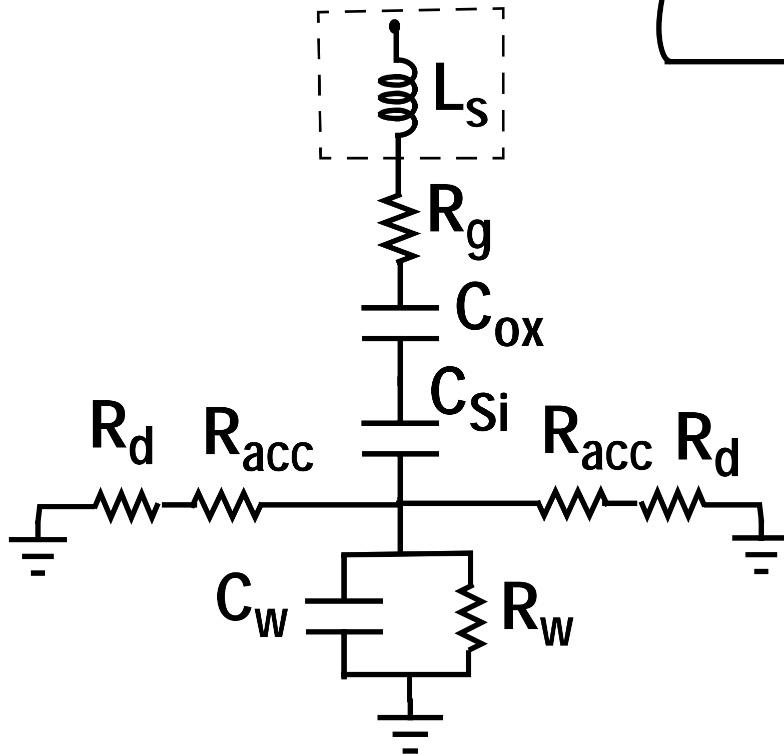


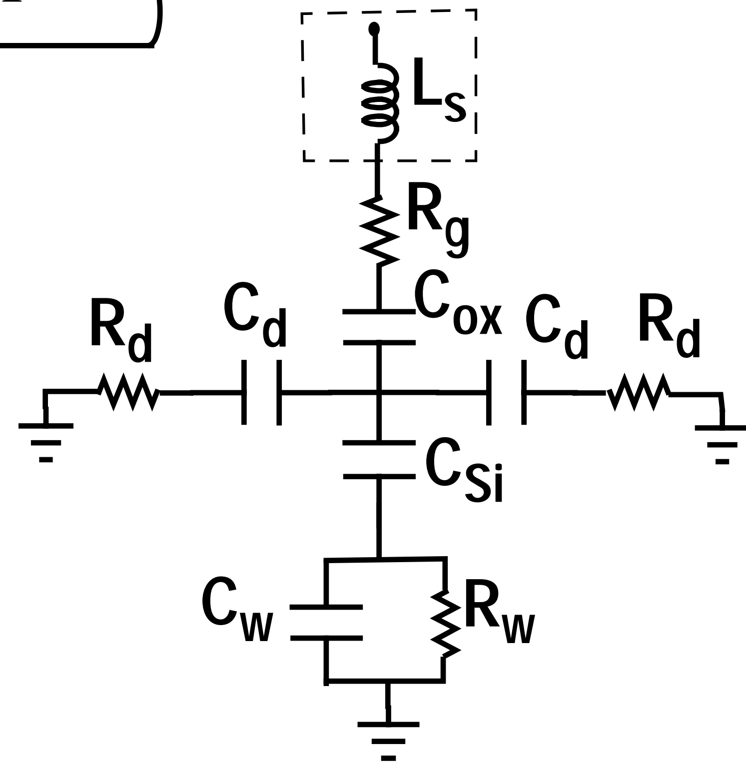
Physical Model

Accumulation

Depletion



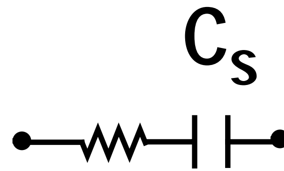




Physical Model Parameters

Parameters	Expression	Description
C_{ox}	$\frac{NWL\varepsilon_{ox}}{t_{ox}}$	oxide capacitance
$C_{Si}(u_s,u_b)$	$\frac{NWL\varepsilon_{Si}}{L_{di}}\left(\frac{\sinh(u_s)-\sinh(u_b)}{F(u_s,u_b)}\right)$ $F(u_s,u_b)=\sqrt{2}\,[\sinh u_b(u_b-u_s)-\cosh u_b-\cosh u_s]^{1/2}$	semiconductor capacitance
C_d	$NWx_{jldd}C_{Si}(u_s,u_{ldd})$	channel-to-S/D depletion cap
R_{acc}	$\frac{L}{2NW\mu_{acc}Q_{acc}}$ $Q_{acc}=\varepsilon_{Si}\left(\frac{kT}{qL_{di}}\right)F(u_s,u_b)$	accumulation-layer resistance
R_g, R_w	$\frac{R_{gsq}W}{3NL}$, $\frac{R_{wsq}L_w}{2NW}$	gate and well resistance
R_d	$\frac{R_{lddsq}L_{ldd}}{NW}+R_{contact}$	LDD and contact resistance

Series Capacitance



Accumulation

$$C_s = \frac{C_{ox} C_{Si}}{C_{ox} + C_{Si}}$$

- C_{Si} in accumulation is associated with accumulation-layer charge (e^-).

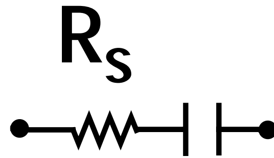
Depletion

$$C_s = \frac{C_{ox}(C_{Si} + 2C_d)}{C_{ox}(C_{Si} + 2C_d)}$$

- C_{Si} in depletion is depletion capacitance associated with fixed donor charge (N_D^+).

C_s varies with bias voltage as C_{Si}, C_d are bias-dependent.

Series Resistance (Varactor Loss)



Accumulation

$$R_S \cong \left(R_g + \left[\frac{1}{2}(R_{acc} + R_d) \,\|\, R_W\right]\right)$$

$$\cong \frac{R_{acc}}{2} \,\Big\|\, R_W$$

Depletion

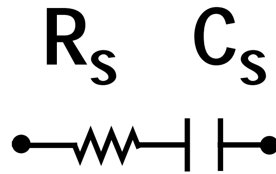
$$R_S \cong R_g + R_W \left(\frac{C_{Si}}{C_{Si} + 2C_d}\right)^2$$

$$\cong R_W \left(\frac{C_{Si}}{C_{Si} + 2C_d}\right)^2$$

- R_S can be reduced by controlling device geometry.

R_S varies with bias voltage as R_{acc}, C_{Si}, and C_d are bias-dependent.

Quality Factor (Q)



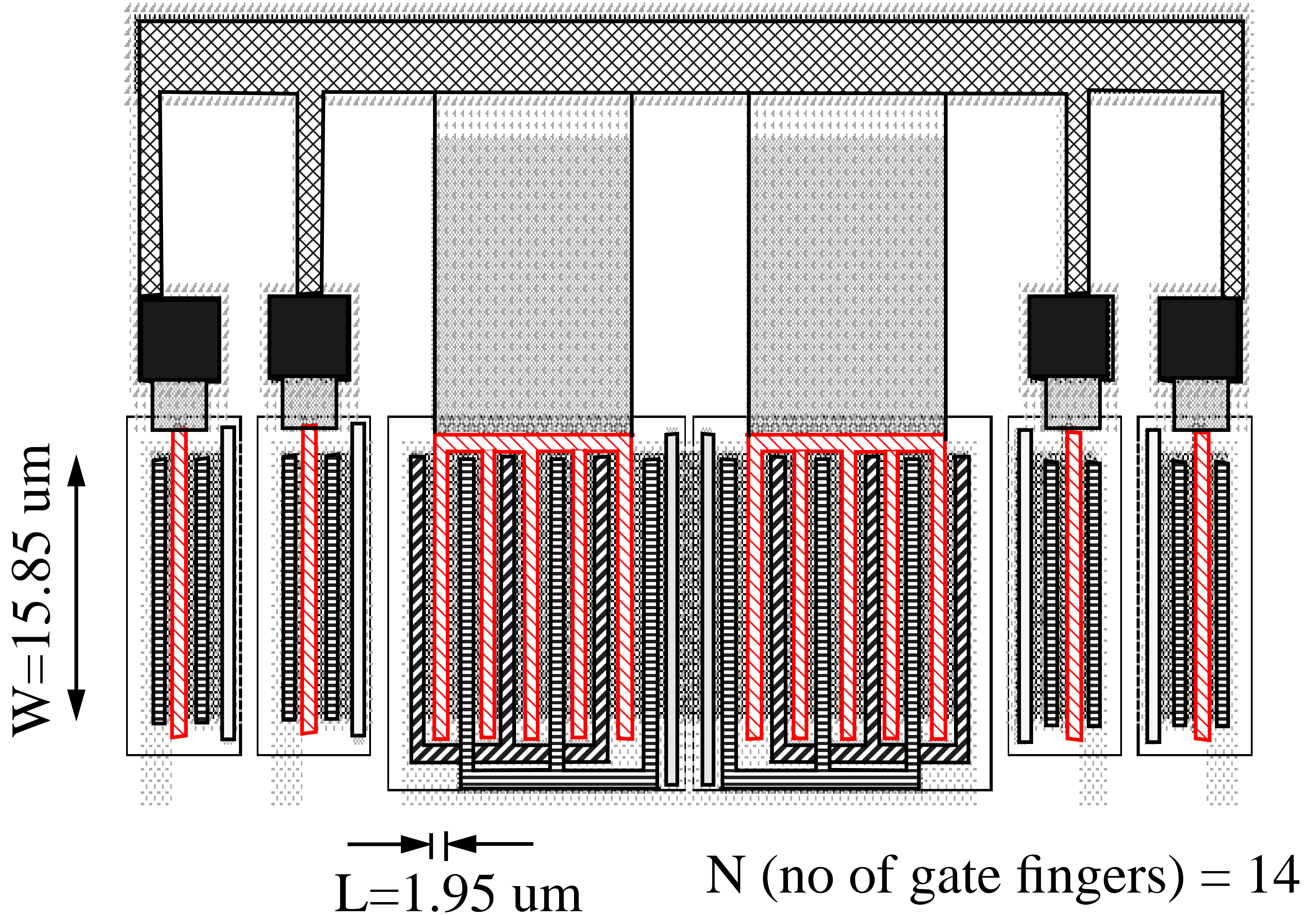
$$Q = \frac{1}{\omega R_s C_s}$$

- Frequency-dependent.
- Bias-dependent as R_s, C_s varies with bias.

Tuning Range

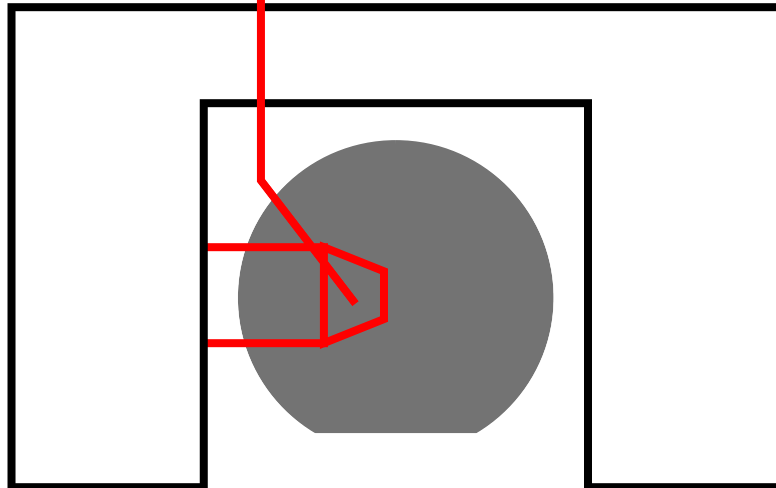
- Tuning range = $\frac{2C_{ox}}{C_{ox} + 2C_{Si,\,min}}$ $\Rightarrow$ 200% @ maximum limit.
- As technology scales, tuning range increases towards the limit.
- When used with low-TC capacitor (eg. MIM capacitor) temperature stability can be improved by trading-off with tuning range.

Test Structure

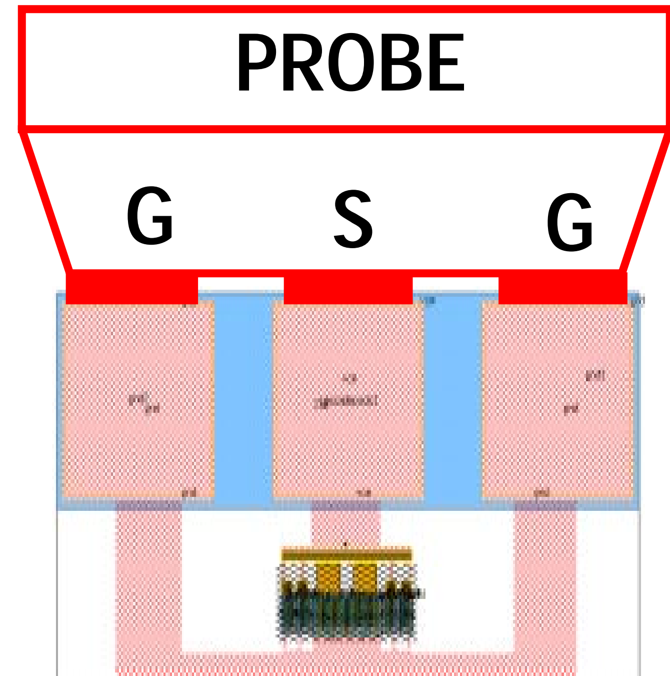


Measurement Setup

Bias Generator

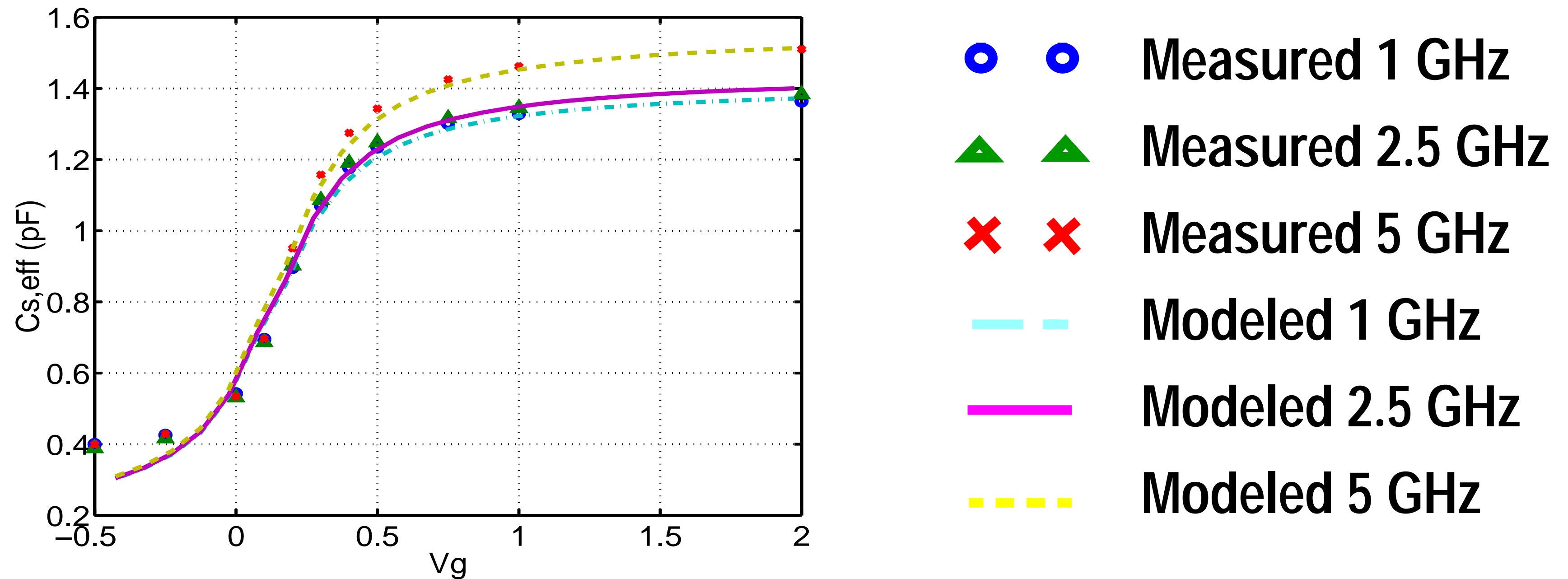


Probe Station



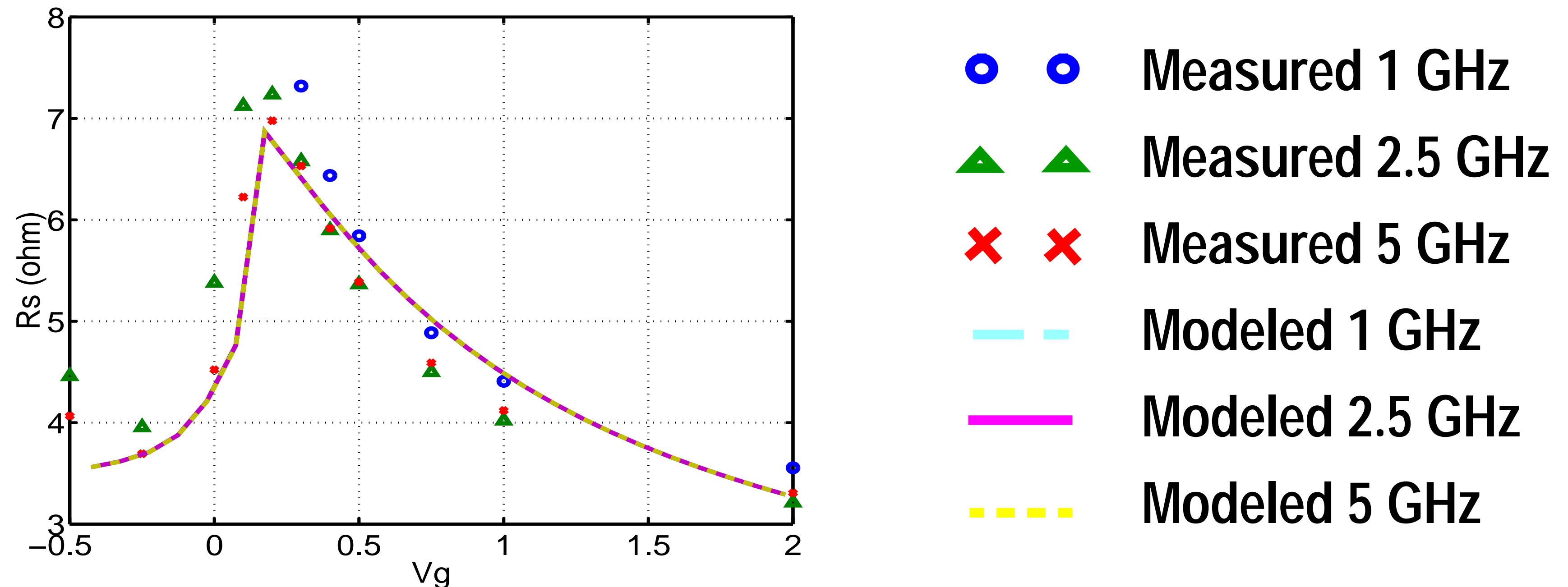
Device Under Test

Measured Series Capacitance



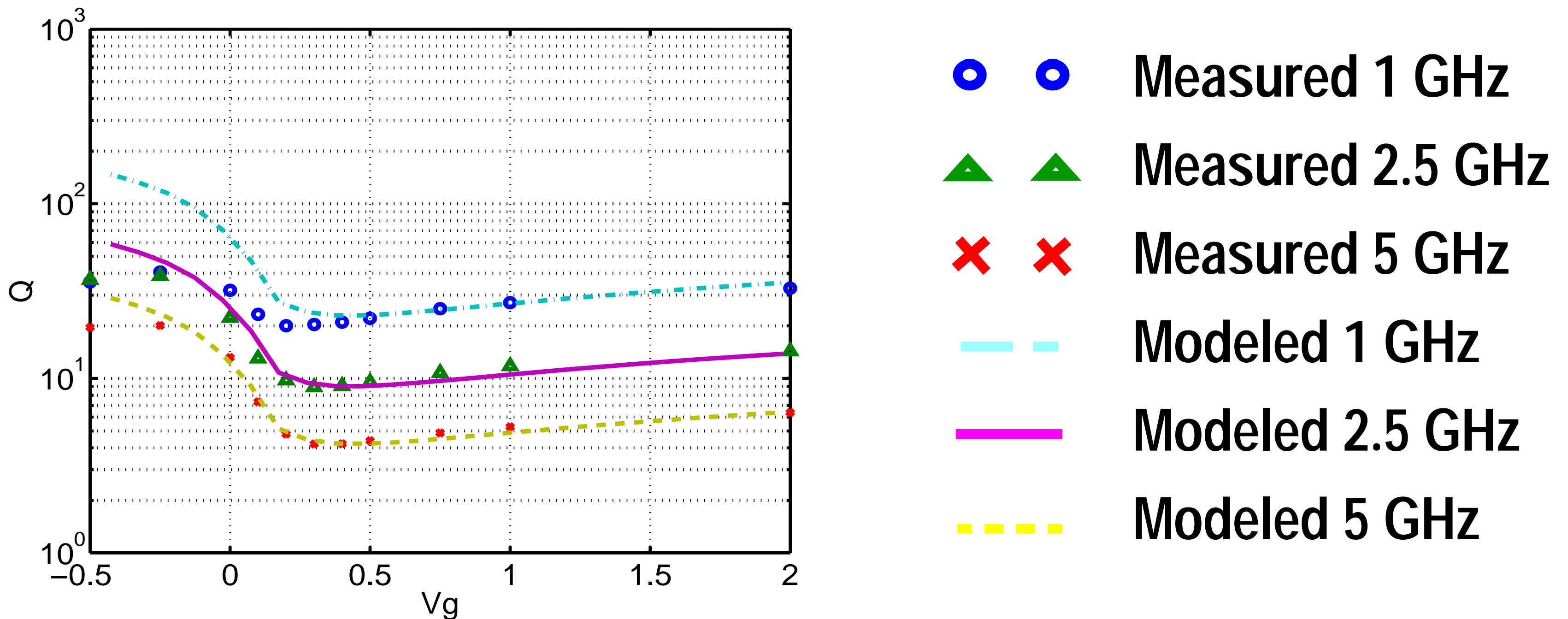
- At $V_g >> V_{FB}$, $C \approx C_{ox}$
- At $V_g < V_{FB}$, $C \approx \dfrac{C_{ox}C_{Si}}{C_{ox} + C_{Si}}$
- Exhibit frequency dependence associated with parasitic inductance => $C_{s,\,eff} = \dfrac{C_s}{1 - \omega^2 L_s C_s}$ $\qquad f_{SR} \geq 15\text{GHz}$

Measured Series Resistance



- In accumulation, R_s increases as V_g is swept from deep accumulation towards flatband due to extraction of accumulation-layer charges.
- In depletion, R_s decreases beyond flatband due to the decrease of C_{Si} which reduces the effect of R_w.

Measured Quality Factor



- Q reaches minimum at flatband voltage where changes in capacitance is large.

==> trade-off between Q and capacitance tuning.

Optimization Formulation

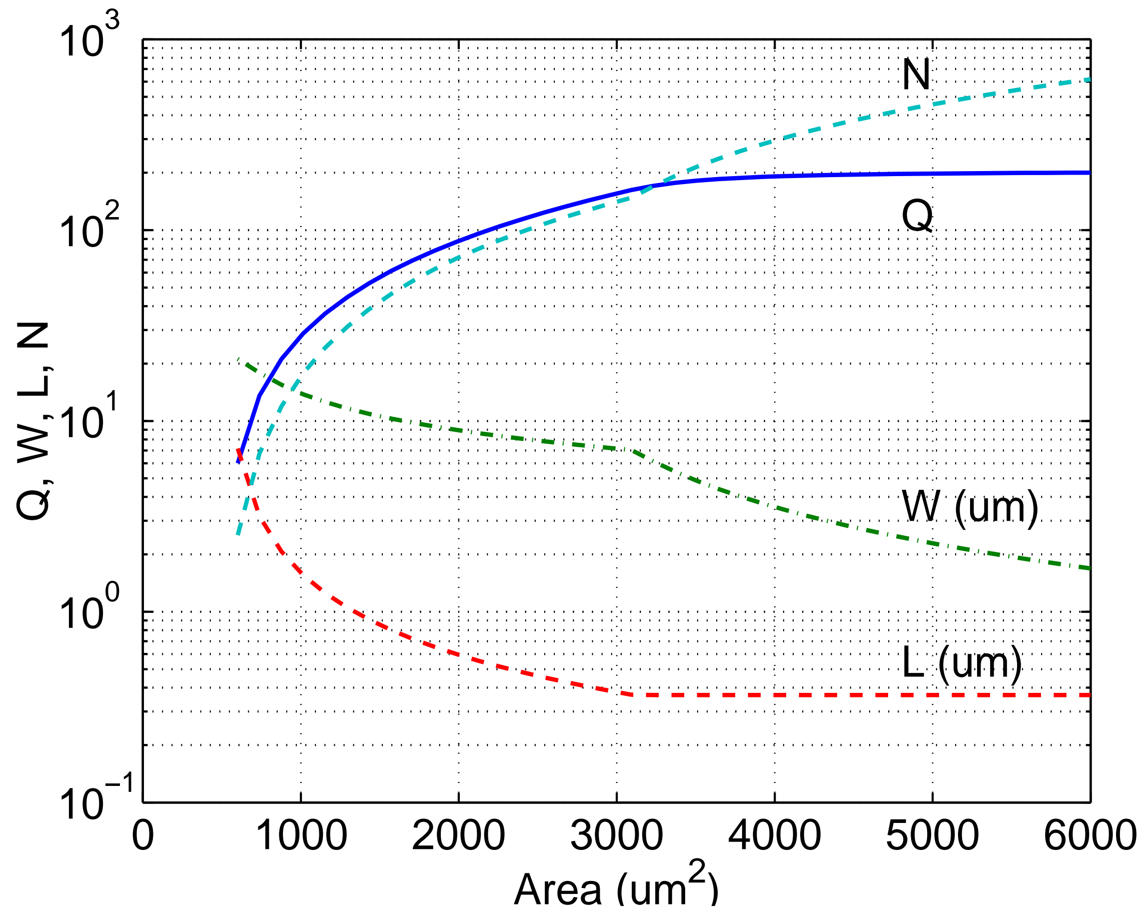
Objective : maximize Q subject to following constraints

- C = nominal desired capacitance (1 pF)
- Area < max allowed area
- Tuning range > min required tuning range (+/- 30%)
- W > min allowed channel width (0.6 um)
- L > min allowed channel length (0.4 um)
- N > min no of gate finger (1)
- Biased in accumulation mode (to minimize substrate effect) ($V_g > V_{FB}$)

Optimization variables : W, L, N, V_g

Optimization Results (0.5 μm CMOS)

C_{nom} = 1 pF, Q @ 1 GHz



$L\downarrow \Rightarrow R_{acc}\downarrow$

$\Rightarrow N\uparrow$

$\Rightarrow R_w, R_{acc}\downarrow$

$\Rightarrow R_{ser}\downarrow \quad Q\uparrow$

Q_{max}=200!!

Conclusions

- Standard CMOS implementation.
- Varactor model has been developed and used for device optimization.
- Substrate effect can be mitigated by operating in accumulation mode.
- Wide tuning range allows trade-off with temperature stability.
- Performance improves with technology scaling.