Analysis and Performance Evaluation of A Distribution STATCOM for Compensating Voltage Fluctuations

P. S. Sensarma, *Student Member,* K. R. Padiyar, *Senior Member,* V. Ramanarayanan

Abstract— Controller design of a STATCOM-based voltage compensator requires a valid analytical model of the system. If phasor algebra is used for modeling, it is difficult to accurately describe the STATCOM behaviour during compensation of subcycle transients in the PCC voltage. In this paper, a small-signal model of the system, with a distribution line, is derived. Predictions based on frequency-domain analysis are made, which are validated by experimental results. This model, therefore, can be used for controller design where subcycle voltage transients are to be compensated. It is shown that the voltage controller, so designed, can accomplish voltage sag mitigation. A discussion on the design of dc bus voltage controller ¯ and experimental results showing its performance ¯ is also included.

Keywords— Power Quality, voltage compensation, modeling, voltage sag, STATCOM

I. INTRODUCTION

In the deregulated power market, adherence to Power Quality (PQ) standards has emerged as a figure-of-merit for the competing power distribution utilities. Among the various PQ problems, voltage disturbances ¯ both steady-state and transient ¯ have been identified to have the maximum probability of occurrence. It has been reported [1] that, High Intensity Discharge (HID) lamps used for industrial illumination get extinguished at voltage dips of **20%.** Also, critical industrial equipment like Programmable Logic Controllers (PLCs) and Adjustable Speed Drives (ASDs) are adversely affected by voltage dips of about 10%. Solution approaches to the voltage disturbance problem, using active devices, can involve either (i) a series injection of voltage, or (ii) a shunt injection of reactive current. The Static Var Compensator (SVC) and the STATCOM are the available shunt compensation devices.

The problem of voltage compensation, using a STATCOM, has been addressed in literature. In [2], a *small-signal* analysis of the system was performed with a *transmission* line, which was modeled as a π network. Presence of *right-half plane zeros* in the transfer function was detected and an integral controller, *cascaded* with a second-order *notch-filter* was proposed. An exclusively experimental study of voltage sag mitigation, using reactive power injection, *can* be found in [3]. Here, a *distribution* line was considered and modeled as a series reactance. It should be noted that PQ issues are mostly relevant in the distribution system and distribution feeders, of length less than 80 km, can be correctly modeled as a *series impedance* [4].

In the present paper, the problem of voltage compensation by reactive current injection, at the end of a distribution line, is investigated. A *dynamic* model of the system is analytically derived and a linear controller designed, based on the derived model. Frequency domain analysis is performed on the compensated system and experimental results obtained to validate the analytical predictions. The capability of the STATCOM to mitigate voltage sag is also demonstrated.

ll. COMPENSATION STRATEGY

The steady-state analysis of voltage compensation using phasor algebra has been dealt with in detail [5], [6]. For a circuit as shown in fig. 1, when line voltage drops are small in comparison with the source voltage E, the PCC voltage magnitude can be expressed as

$$V \simeq E[1 - \frac{Q_l - Q_{inj}}{S_{sc}}] \qquad (1)$$

where,
Q_l : Load reactive power
Q_{inj} : Injected reactive power
S_{sc} : Short-circuit level at PCC.
Thus, under steady-state, a defined change in the PCC voltage magnitude is brought about by a unique magnitude of reactive power. Extending this concept, a control strategy to achieve compensation of voltage transients can be conceived.

lll. THE LINEAR MODEL

A. Derivation of Model

1)PCC Voltage Control : The three-phase voltages are transformed to another set of variables $(d-q)$, as
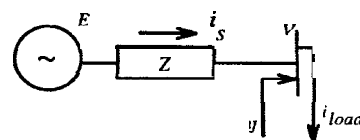

Fig. 1. Single line diagram of system.

The authors are with the Department of Electrical Engineering, Indian Institute of Science, Bangalore: **560 012,** INDIA. E-mail: vram@ee.iisc.ernet.in.

$$x = \omega_0 L/\text{km} = 0.61 \ \Omega/\text{km}$$
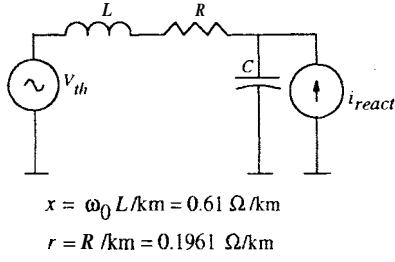$$r = R/\text{km} = 0.1961 \ \Omega/\text{km}$$

Fig. 2. Circuit model of transmission line.

viewed from a rotating reference-frame. Assuming no zero-sequence components, the governing equations are

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \sqrt{\frac{2}{3}} [A] \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \qquad (2)$$

where,

$$[A] = \begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \end{bmatrix}. \qquad (3)$$

To analyze the effect of reactive current on the voltage magnitude at the PCC, the following assumptions are made.

- The analysis is confined to positive − sequence components only.
- All harmonic currents and voltages are neglected.
- The transmission line is modeled, based on the circuit shown in fig. 2. V_{th} represents the Thevenin equivalent voltage source as seen from the PCC terminal into the network. It is considered to remain constant during the time interval of interest.

The PCC voltage magnitude, $|v(t)|$, is defined as

$$|v(t)| = \sqrt{v_d(t)^2 + v_q(t)^2}. \qquad (4)$$

Under the stated assumptions, for zero initial conditions and no real current injection, the transfer function between small changes in the voltage $\Delta|v(t)|$ in response to small changes in injected reactive current Δi_{react} has been shown [2] to be

$$\frac{\Delta|V|(s)}{\Delta I_{react}(s)} = j \frac{Z_{th}(s - j\omega_0) - Z_{th}(s + j\omega_0)}{2} \qquad (5)$$

where $Z_{th}(s)$ is the equivalent positive-sequence Thevenin impedance of the network and can be expressed as

$$Z_{th}(s) = \frac{R + sL}{s^2 LC + sRC + 1}. \qquad (6)$$

The model of a distribution line comprises only the series inductance and resistance, L, and R, respectively. So, the driving point impedance can be simplified to

$$Z_{th}(s) = R_s + sL_s. \qquad (7)$$

Substituting (7) in (5) yields

$$\frac{\Delta|V|(s)}{\Delta I_{react}(s)} = \omega_0 L_s = G(s) \qquad (8)$$

Therefore, if the mains frequency remains constant (ω_0), the transfer function is a *scalar* gain. It is observed that although the resistive part of the series impedance was considered in (7), it does not affect the voltage dynamics. This result cannot be derived from phasor algebra, which deals with steady-state sinusoidal quantities only.

2) STATCOM DC-bus Capacitor : The inverter dc bus voltage is held only by the dc bus capacitor, C_d. Since there are no energy sources or sinks attached to the dc bus, the net real power transacted by the STATCOM must be zero. In a practical situation, non-ideaiities in the capacitor and inverter switches result in a net energy loss. If these losses are not supplied from an external source, the capacitor will discharge. As the operating point of the STATCOM is decided by the dc bus voltage, it is necessary that some active power must be drawn from the ac side, to replenish the system losses. To stabilize the operating point, a dc bus voltage loop is therefore necessary.

The capacitor, along with its losses, is modeled as shown in fig. 3. Denoting its instantaneous voltage by $v_C(t)$ and the current through it by $i_C(t)$, its charging behaviour is described by

$$\frac{V_C(s)}{i_C(s)} = \frac{R_c}{1 + sR_cC_d} = \frac{1}{sC_d} \cdot \frac{s\tau_c}{1 + s\tau_c} \qquad (9)$$

where,

$$\tau_c = R_c C_d. \qquad (10)$$

Equation (9) can be interpreted in the following manner. If the capacitor time constant (τ_c) is much larger than the dc-bus controller time constant (τ_{dc}), then the capacitor can be approximately modeled as an ideal integrator, scaled by a factor $1/C_d$. In such cases,

$$\frac{V_C(s)}{i_C(s)} = \frac{1}{sC_d}. \qquad (11)$$

B. Controller Design

1)PCC Voltage Control : Assuming that the current controller has a much larger bandwidth, the voltage loop with the controller is shown in fig. 4. Arbitrary bandwidth ω_b can be assigned to the closed-loop system by using either an integral or a PI-controller. The idealized Bode diagrams for both these cases are shown in fig. 5. With a PI controller, to obtain a finite system bandwidth

$$K_p < 1. \qquad (12)$$

2) DC-bus Voltage Control : Equation (11) gives the plant transfer function for the dc bus charge-up. A
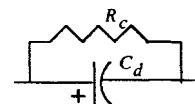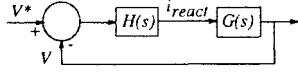

Fig. 3. Capacitor Model.
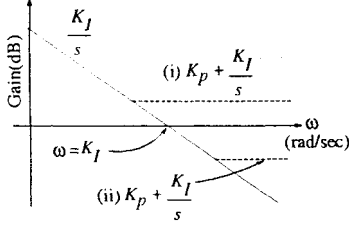
Fig. 4. PCC Voltage control loop.

Fig. 5. Controller Options. [i] PI controller : $K_p > 1$ [ii]$K_p < 1$.

proportional controller $H_d(s)$, with gain K_d, is used to obtain a first-order closed-loop response. The closed-loop time constant (τ_{dc}) is given by

$$\tau_{dc} = \frac{C_d}{K_d}. \qquad (13)$$

IV. EXPERIMENTAL IMPLEMENTATION

A. Hardware Set-up

An 8-KVA, IGBT-based STATCOM was chosen to experimentally verify the analytical model. The STATCOM used is a standard 3-phase inverter with PWM switching. Fig. 6 shows the schematic diagram of the experimental hardware.

The control platform was built around the TMS320C50, a fixed-point DSP processor. The controller board has provisions for acquisition and A/D conversion of 10 analog signals and digital 1/O ports for PWM generation.

An 8253 timer generates the interrupts for the start-of-sampling. The passive elements, namely, the series inductors L_f and the dc-bus capacitor C_d are designed to limit the ripple in the ac side current and dc bus voltage of the STATCOM, respectively. Ratings of the hardware parameters are provided in Table I.

Typical parameters for a distribution line (66 kV, 10 MVA) are shown in fig. 2. It is to be noted that a distribution line with a higher X_s/R_s ratio, of approximately 9, has been selected for the experimental set-up.

B. Control Implementation

Fig. 7 shows the controller structure used for voltage compensation and comprises an inner current loop and an outer voltage loop. For the present study, the current control was implemented using a hysteresis control scheme. The current response obtained is immune to PCC voltage variations *and* second-harmonic components in the dc bus voltage.

A P-I controller is chosen for PCC voltage control and K_p is selected such that (12) is satisfied. Thus,

$$H(s) = K_I \frac{1 + s\tau_c}{s}. \qquad (14)$$

Assuming an approximately balanced system, the PCC voltage magnitude, computed as in (4), is expected to remain constant. In a practical situation, however, $|v(t)|$ will not be constant on account of several reasons. Some possible sources of this deviation are listed below.

- Offset errors in the voltage sensors introduce an oscillatory component in $|v(t)|$, at the fundamental frequency w_s.
- The PCC voltages carry a small unbalance. Any negative sequence voltage introduces a second harmonic component in $|v(t)|$.
- Any PCC voltage harmonic at frequency ω_h introduces an oscillatory component in $|v(t)|$ at a frequency $\omega_h \pm w_s$.

The filter block $G_F(s)$, as shown in fig. 7, is introduced to attenuate the noise in the $|v(t)|$ signal and is of the form

$$G_F(s) = \frac{1}{1 + s\tau_F}. \qquad (15)$$

Since the filter appears *within* the closed-loop, it also affects the controller dynamics in addition to noise filtration. The reactive current command generated by the voltage controller is output-limited so as not to exceed the STATCOM rating.

V. EXPERIMENTAL RESULTS

A. Analytical Predictions

The loop gain $G_O(s)$ of the voltage loop is given by

$$G_O(s) = G(s)G_F(s)H(s). \qquad (16)$$

Plant gain $G(s)$ is as given in (8). Substituting (8), (14) and (15) in (16), the following expression can be obtained

$$G_O(s) = K_I \omega_0 L_s \frac{(1 + s\tau_c)}{s(1 + s\tau_F)}. \qquad (17)$$

TABLE I
CIRCUIT AND CONTROL PARAMETERS

Inverter Rating		8 kVA
Coupling transformer rating		415/208 V, Δ/Δ, 1 winding
Inverter series inductance	L_f	9.67 mH
Inverter series resistance	R_f	0.206 Ω
Inverter dc bus voltage	V_d	400 V
Inverter dc bus capacitance	C_d	1750 μF
Dc-bus capacitor time constant	τ_c	105 s
Inverter switching frequency (max)	f_s	5 kHz
Supply line inductance	L_s	9 mH
Supply line resistance	R_s	0.3 Ω
Induction Motor		
HP		5 hp
Voltage		415 V
Rated current		7.5 A
Starting kVA		32.35 kVA
Controller Parameters		
K_p		0.5
K_I		320
τ_c		24ms

Fig. 6. Circuit Diagram.

Fig. 7. Control Schematic.

Controller and filter parameters used are listed in Table I. The filter time-constant was selected to attenuate the 50Hz component in the $|v(t)|$ signal by a factor of 88%. The root-locus for the above system is plotted in fig. 8, with K_I varying within the range indicated. For the present value of $K_I = 1$, the closed loop poles are read out as

$$s = -21.16 \pm j19.64 \qquad (18)$$

Hence, by the predictions of the analytical model, to a step input, the bus voltage *and* the reactive current will show a nearly critically damped response. From standard results for second-order systems, the settling time for this closed-loop system is 123 ms.

Fig. 8. Root Locus plot for the compensated system, $0 < K_I < 2.5$.

B. Observations

The STATCOM was started to an existing overvoltage condition, which was obtained by setting the reference for the PCC voltage magnitude $|v(t)|^*$ at a value that is lower than the nominal. Fig. 9(a) and fig. 9(b) show the starting transients in the PCC voltage magnitude error and in the injected reactive current, respectively. The inverter was switched on at $t = 0$ and the current is zero till that instant.

After the STATCOM reached steady-state, a step-change was given to the voltage reference command of the controller. Fig. 10(a) and fig. 10(b) show the resultant transients.

The low frequency oscillations in the PCC voltage error (fig. 9(a) and 10(a)) are due to unbalance and harmonic components in the PCC voltage waveform. The high frequency components are due to measurement noise. The current controller was based on a frequency-limited, hysteresis rule. The switching ripples in the output current are expected to be higher, in comparison with a carrier-based PWM scheme. The high-frequency oscillations in the reactive current waveforms (fig. 9(b) and 10(b)) are due to the switching ripples in the STATCOM current. Some measurement noise is also introduced.

C. Discussions

The steady-state voltage compensation capability of the STATCOM is illustrated by the experimental results shown in fig. 9(a) and fig. 9(b). It is seen in fig. 9(a), that the voltage error settles to zero, 150 ms after the STATCOM is switched on at $t = 0$. This de-

Fig. 9. STATCOM starting transients (a) PCC voltage error (b) STATCOM reactive current.

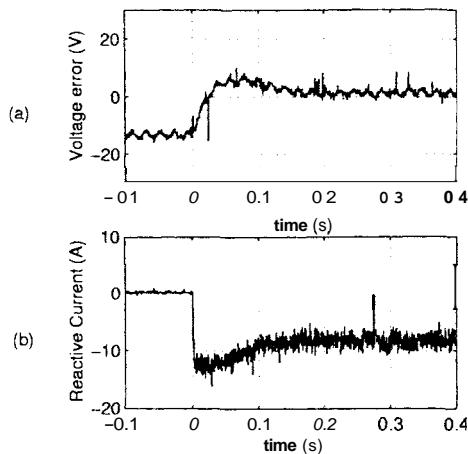Fig. 10. STATCOM transients for step change in voltage reference (a) PCC voltage error (b) STATCOM reactive current.

lay is due to the PI controller, which saturates before the STATCOM is started. Hence the overshoot in the voltage error, as seen in fig. 9(a).

Fig. 10(a) and fig. 10(b) show the above variables in response to a step increase in the PCC voltage command. The system is still in the linear zone. It is seen that the settling time is about 128 ms which matches closely with the analytically predicted value of 123 ms. The response is nearly critically damped, as there is practically no overshoot, and this matches the analytical prediction too. It can be concluded, therefore, that the derived model represents the system accurately.

VII. VOLTAGE SAG COMPENSATION

A. Sag initiation

Voltage sag has been defined [7] as a reduction in the voltage magnitude from its nominal value for a duration ranging from a few milliseconds to one minute. In this paper, a load-induced sag is addressed, with the load placed downstream from the PCC. The load comprises an induction motor, shown in fig. 6, which is started Direct on Line (DOL). The resulting heavy starting current initiates a sag. The STATCOM is expected to reduce the intensity of the sag.

B. Sag mitigation

Fig. 11(a) and fig. 11(b) depict the experimental results of the PCC voltage error during sag, with and without STATCOM support, respectively. Although various loads react differently to varying levels of *sag,* it has been emphasized [8] that both magnitude and duration of sag are of comparable concern. A suitable indicator of the intensity of sag can, therefore, be the area under the PCC voltage error vs. time curve. Using this definition, the area for the case without compensation is 20.22 V-s, whereas with compensation it reduces to 12.34 V-s. The starting current of the motor being *6* times its rated current, the effective load rating during *sag,* which is the starting kVA of the motor, is propor-
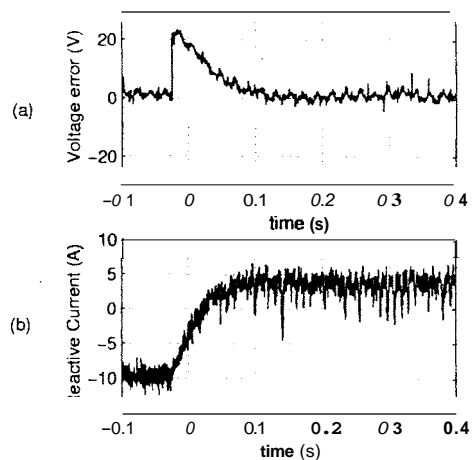
tionately higher (32.35 kVA). Thus, with a STATCOM rated at 25% of the effective load kVA, the intensity of sag was reduced by 39%.

VIII. DC BUS VOLTAGE CONTROL

Fig. 12(a) shows the dc bus voltage during initial charge-up. In this region, the voltage error is large and hence the output of the proportional controller, $H_d(s)$, the charging current reference is clamped to its upper saturation limit. This is a constant-current charging region and the capacitor voltage is seen ramping up to its reference value. The active component of the STATCOM's ac side current is 3.65 A, for which the theoretical dc voltage slope is 1.942 V/ms. The experimentally observed value is 1.913 V/ms. As there is close agreement, the capacitor can be modeled as *a* scaled integrator.

Fig. 12(b) shows the dc bus voltage during a voltage sag at the PCC. This involves very fast reversal of the STATCOM's ac side current from reactive leading to full reactive lagging. The sag occurs at $t = 0$. It is seen that the dc bus voltage remains at its reference value throughout the period of sag. The ability of the dc capacitor to hold its voltage is decided by its capacitance value. For the present case, the capacitor was designed for a 5% ripple at rated current and it is observed that the capacitor voltage does not overshoot its design limits. It may be concluded, therefore, that a proper selection of capacitance value at the design stage ensures its satisfactory performance under transient conditions.

IX. CONCLUSIONS

In this paper, the problem of voltage compensation at a PCC, at the end of a distribution line, was investigated. On the basis of linearized analysis of the system and experimental results on an 8 kVA STATCOM the following can be concluded.
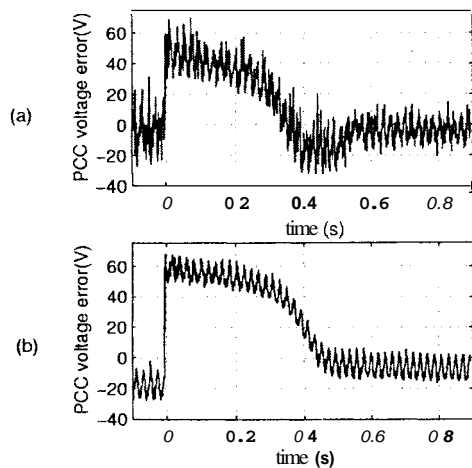
Fig. 11. PCC voltage error during sag (a) with STATCOM support (b) without STATCOM support.

Fig. 12. DC bus voltage (a) charging during startup (b) during voltage sag at PCC.

- When the shunt capacitances in the distribution line are negligible, the transfer function $(\Delta|V|(s)/\Delta I_{react}(s))$ is a scalar gain, for constant system frequency.
- A linear voltage controller was designed on the basis of the derived model. Experimental results closely match the analytical predictions (4% error in settling time).
- The STATCOM was used to compensate for a load-induced voltage sag. For a STATCOM rated at 25% of the effective load kVA, voltage sag could be reduced by 39%.
- The dc capacitor was designed for 5% dc bus voltage ripple, when the STATCOM delivers rated reactive current. With this capacitance value and a proportional controller, the operating point is stabilized even during severe transients.

X. ACKNOWLEDGMENTS

References

[1] M. F. McGranaghan, D. R. Mueller and M. J. Samotyj, "Voltage Sags in Industrial Systems", *IEEE Trans on Industry Applications*, Vol. 29, No. 2, Mar/Apr 1993
[2] K. R. Padiyar, A. M. Kulkarni, "Design of reactive current and voltage controller of static condenser", *Electrical Power & Energy Systems*, Vol.19, No.6, 1997.
[3] P. Wang, N. Jenkins, M. H. J. Bollen "Experimental Investigation of Voltage Sag Mitigation by an Advanced Static VAR Compensator", *IEEE Trans on Power Delivery*, Vol.13, No.4, Oct 1998.
[4] W. D. Stevenson Jr., "Elements of Power System Analysis", *McGraw Hill*, 4th Ed.
[5] R. S. Weissbach, G. G. Karady and R. G. Farmer "Dynamic Voltage Compensation on Distribution Feeders using Flywheel Energy Storage", *IEEE Trans on Power Delivery*, Vol.14, No.2, Apr 1999, pp 465-471.
[6] T. J. E. Miller, "Reactive Power Control In Electric Systems", *John Wiley*, 1982.
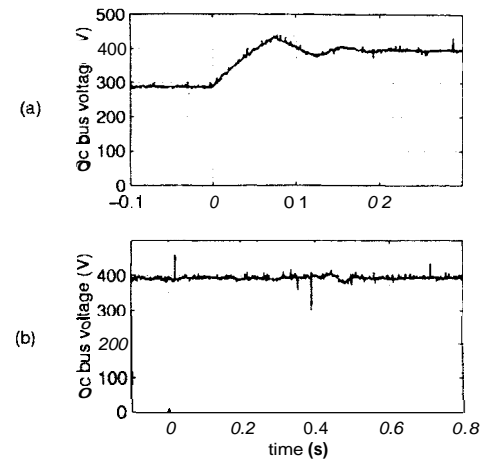[7] D. D. Sabin, A. Sundaram, "Quality Enhances Reliability", *IEEE Spectrum*, Feb '96
[8] W. E. Reid, "Power Quality Issues- Standards and Guidelines", *IEEE hns. on Power Delivery*, Vol. 32, No. 3, May/June 1996.

P. S. Sensarma receiwd his B.E.E and M.Tech from Jadavpur University, Calcutta (1990) and I.I.T Kharagpur (1992), respectively. From 1992 to 1994 he worked in the Motor Design department, Bharat Bijlee Ltd, Thane, India and in a power plant of CESC Ltd, Calcutta, India. In 1994, he joined as a PhD student in the Electrical Engineering Department, Indian Institute of Science, Bangalore, India, where he is working on power quality issues.

K. R. Padiyar is a Professor of Electrical Engineering at the Indian Institute of Science, Bangalore, India. He obtained his B.E degree in Electrical Engineering from Poona University in 1962, M.E degree from Indian Institute of Science in 1964, and PhD degree from University of Waterloo, Canada in 1972. He was with I.I.T Kanpur from 1976-1987 prior to joining I.I.Sc. His research interests are in the area of HVDC and FACTS, System Dynamics and Control. He has authored three books and over 150 papers. He is a Fellow of National Academy of Engineering (India).

V. Ramanarayanan is a Professor and Chairman of the Department of Electrical Engineering at the Indian Institute of Science, Bangalore, India. He took his B.E., M.E., and Ph.D., from University of Madras, Indian Institute of Science, and California Institute of Technology in the years 1970, 1975 and 1986 respectively. He had held positions in industry as Senior Design Engineer, and Chief of R&D with M/s Larsen & Toubro Ltd (1970-79) and NGEF Ltd (1979-82). His areas of interest include Power Electronics, Industrial Drives, Switched Mode Power Conversion, and Power Quality issues. He is a consultant to several industries in related areas.