Analysis, Design, and Performance Evaluation of Droop Current-Sharing Method

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Abstract -**The droop current sharing method is analyzed, and a general design procedure is proposed. It is shown that the current-sharing accuracy of N+1 power supplies is a function of the output-voltage set-point accuracy, the slope of the output-voltage droop, and gains of the control loop. It was found that to achieve a current sharing accuracy of 10% the output voltage of the paralleled power supplies needs to be set within 0.35%. The accuracy of the design procedure was compared against measured results of three power supplies operating in parallel.**

I. INTRODUCTION

Generally, the paralleling of lower-power converter modules offers a number of advantages over a single, high-power, centralized power supply. Performance-wise, the advantages include higher efficiency, better dynamic response due to a higher frequency of operation, and better load regulation. System-wise, paralleling allows for redundancy implementation, expandability of output power, and ease of maintenance. In fact, paralleling of standardized converter modules is the approach that is widely used in distributed power systems for both front-end and load converters.

When operating converter modules in parallel, the major concern is load-current sharing among the paralleled modules. A variety of approaches, with different complexities and current sharing (CS) performances, were proposed, developed, and analyzed in the past [1]-[5]. Among these approaches, the most attractive are those that provide the desired CS without implementing a master/slave configuration or requiring a separate current-share controller. These "democratic" (also referred to as autonomous or independent) CS approaches, which allow each module to operate either as a stand-alone unit or as a parallel module, make possible the implementation of true N+1 redundant systems.

The simplest "democratic" CS technique is the droop method. The droop method relies on the internal (output) and/or externally added resistance of the paralleled modules to maintain a relatively equal current distribution among the modules. The droop method can be implemented in a variety of schemes, as described in [2]. Generally, the droop CS technique is simple to implement, and it does not require any communication (control-wire connection) between the paralleled modules. However a trade-off must be made between load regulation and output-voltage set-point accuracy.

In this paper, the current-sharing accuracy of N+1 units that use the droop method is analyzed as a function of the output-voltage set-point accuracy, the slope of the output-voltage droop, and the gain of the control loop. A complete design procedure is presented and experimentally verified on three power supplies operating in parallel.

II. ANALYSIS OF A DROOP CURRENT SHARING TECHIQUE

Generally, the current-sharing techniques based on the droop method rely on the slope of the load regulation characteristic of the paralleled power supplies. To demonstrate the droop current-sharing approach, Fig. 1 shows the parallel connection of two power supplies which have slightly mismatched regulation characteristics due to a difference in their output-voltage set points. It should be noted that the slopes of the characteristics in Fig. 1(b) are the same.

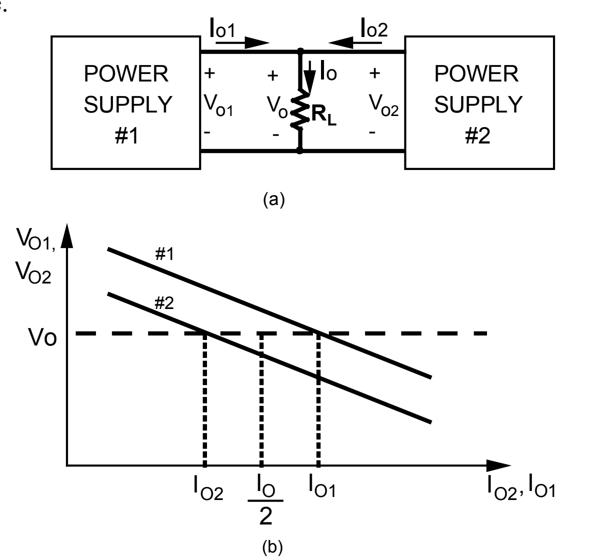

Fig. 1 Droop current-sharing method: (a) connection of two power supplies in parallel; (b) load regulation characteristics.

As can be seen from Fig. 1(b), because of the mismatching, power supply #1, which has a higher output-voltage set point, carries more load current than power supply #2. Generally, the current-sharing accuracy, i.e. the difference between the output current of the individual modules, is determined by the difference between the output-voltage set point of individual modules, and by the slope of their load-regulation characteristic. Figure 2 illustrates the dependence of the current-sharing accuracy on the mismatch of output-voltage set points, whereas Fig. 3 shows the current-sharing accuracy dependence on the slope.

As can be seen from Fig. 2, the current-sharing accuracy improves as the output-voltage set-point mismatching decreases. When the load-regulation characteristics are perfectly matched, as shown in Fig. 2(d), the modules share the load current equally. Similarly, from Fig. 3 it can be seen that a steeper load-regulation characteristic results in better current sharing. It should be noted that for power supplies with ideal load-regulation characteristics, as shown in Fig. 3(d), the power supply with the highest output-voltage set point carries the entire load current.

The output-voltage droop can be realized several ways. One implementation is to add series resistance (R_{droop}) to the output of the individual power supplies. The major drawback of this approach is increased power dissipation. As a result, the method is not suitable for high-current applications.

Another method of implementing the droop characteristic is to utilize the leakage inductance of the main transformer and various voltage drops through the output stage of the power supply, as discussed in [2]. However, this method does not seem practical because it relies on component parasitics to achieve current sharing.

The best approach to implement the droop characteristic is to use a signal that is proportional to the output current to modify the output-voltage feedback loop characteristic so that the output voltage decreases as the load current increases. The block diagram of a circuit which uses this approach is

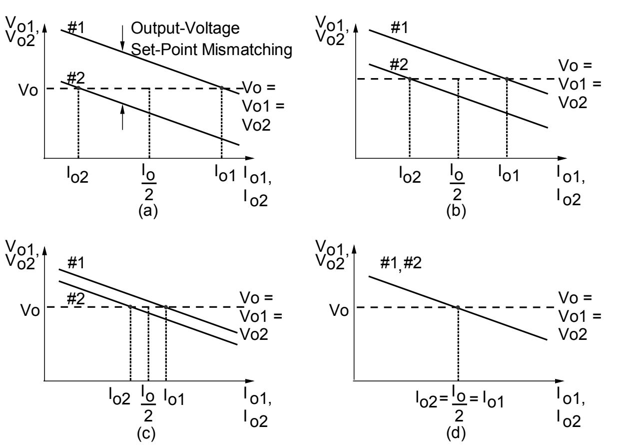

Fig. 2 Effect of output-voltage set-point mismatching on current-sharing accuracy: (a) very large mismatch; (b) large mismatch; (c) small mismatch; (d) no mismatch. Slope of characteristics in all plots are same.

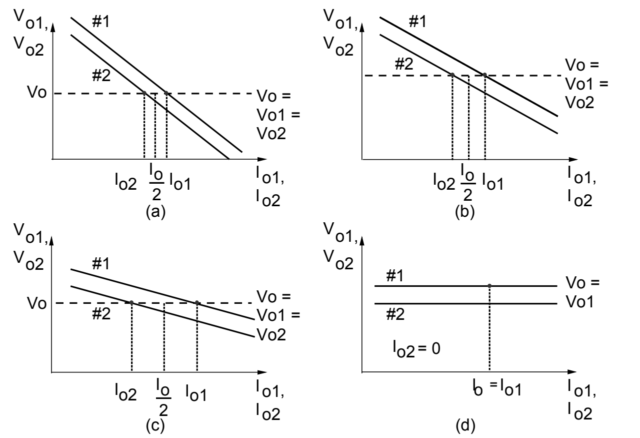

Fig. 3 Effect of load-regulation-characteristic slope on current-sharing accuracy: (a) very large slope; (b) large slope; (c) small slope; (d) zero slope (ideal power supply). The output-voltage set-point mismatching is same for all characteristics.

shown in Fig. 4.

In Fig. 4, signal $R_i \cdot i_{SW}$, which is proportional to switch current i_{SW}, is compared to control voltage Vc at the input of the PWM modulator (PWM MOD). Since control voltage Vc is the output of the error amplifier (E/A) that has a dc gain Ko, Vc represents the amplified difference between reference voltage V_{REF} and the sum of the signals which are proportional to output voltage Vo and output current Io by factors Kd, Kcs, respectively. The output of the PWM modulator is the duty cycle of the power stage.

As can be seen from Fig. 5(a), which shows the key steady-state waveforms of the circuit in Fig. 4, when the load current is increased from I_{01} to I_{02}, error-amplifier output-voltage Vc decreases from V_{C1} to V_{C2} because the amplitude of the signal at the inverting input of the PWM modulator $V^- = Kd * V_O + Kcs * I_O$ increases. As a result, the duty cycle of the signal at the output of the modulator decreases from D_1 to D_2 causing a drop of output-voltage V_O, as shown in Fig. 5(b).

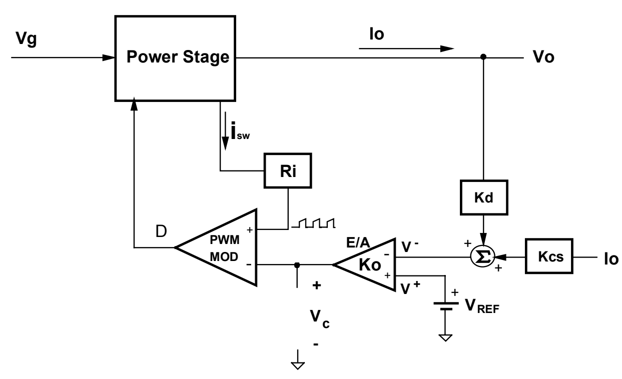

Fig. 4 Block diagram of PWM converter with current-mode control which has output-voltage droop characteristic implemented with approach that modifies output-voltage feedback loop with signal proportional to load current.

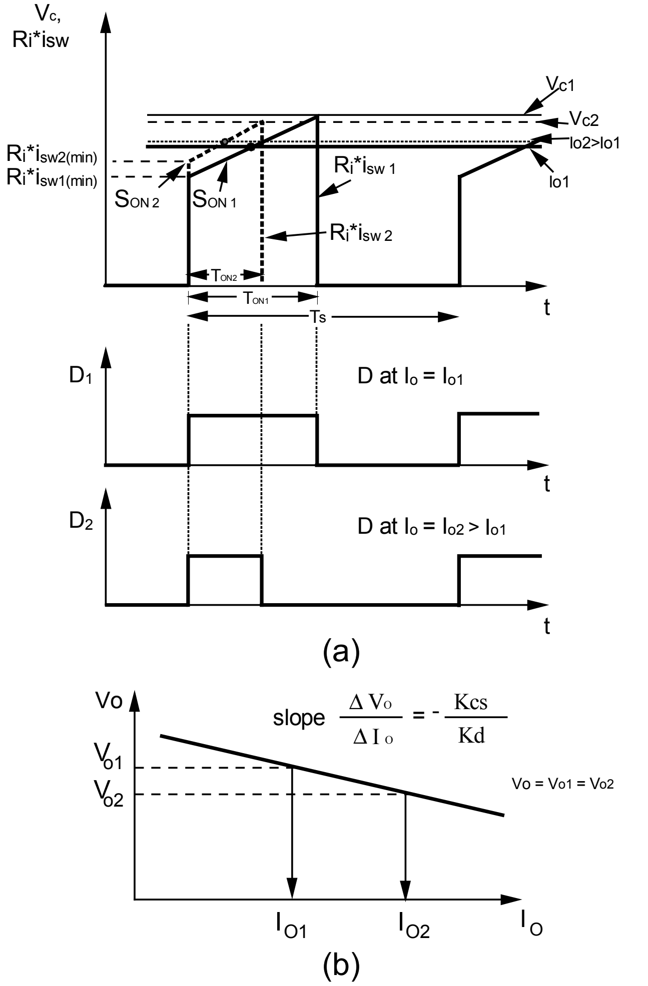

Fig. 5 Operation of droop method in Fig. 4: (a) steady-state waveforms at input and output of PWM modulator at two load currents $I_{O2} > I_{O1}$ (b) load-regulation characteristic.

Assuming that the gain of the error amplifier is high ($K_O \rightarrow \infty$), it can be shown that the governing equation for the output voltage is

$$V_O = \frac{V_{REF}}{Kd} - I_O \cdot \frac{Kcs}{Kd} = V_O(@ I_O = 0) - I_O \cdot \frac{Kcs}{Kd}, \qquad (1)$$

where V_{REF} is the reference voltage, and $V_O\ (@\ I_O = 0)$ is output voltage V_O at no load. According to Eq. (1), the slope of the regulation characteristic is given by $\Delta V_O / \Delta I_O = -Kcs/Kd$.

III. DESIGN GUIDELINES

The design of the droop-current-sharing approach shown in Fig. 4 requires that the droop of the load-regulation characteristic is properly determined so that the current sharing meets the specified accuracy, while output voltage V_O stays within the specified regulation band $V_O \pm \Delta V_O$. To achieve the best possible accuracy for a given output-voltage set-point mismatching, the droop of the load regulation characteristic should be maximized, as seen from Fig. 3.

A. Calculation of Maximum Droop Range

The maximum droop range, defined as the difference between output-voltage V_O at no load $(I_O = 0A)$ and full load $(I_O = I_{O(FL)})$, is limited by the specified output-voltage regulation range $V_O \pm \Delta V_O$, the output-voltage set-point accuracy $\Delta V_{O(SPA)}$, and the desired design margin $\Delta V_{O(margin)}$, as illustrated in Fig. 6. The maximum relative output-voltage droop $\Delta V_{O(droop)\max} / V_O$ is than determined from Fig. 6 as

$$\frac{\Delta V_{O(droop)\max}}{V_O} = 2 * \left(\frac{\Delta V_O}{V_O} - \frac{\Delta V_{O(margin)}}{V_O} - \frac{\Delta V_{O(SPA)}}{V_O}\right). \qquad (2)$$

Fig. 7 shows the plot of the maximum relative droop range as a function of output-voltage range and output-voltage set-point accuracy, assuming 1% design margin. For example, from Eq. (2), or Fig. 7, it can be calculated that the maximum output-voltage droop for output voltage $V_O = 5\ V \pm 5\%$ with a set-point accuracy of $\pm 1\%$, is $\Delta V_{O(droop)\max} = 300mV$.

Finally, since the load-regulation characteristic droop is set by gain Kcs, it is necessary to find the relationship between Kcs and maximum output-voltage droop. From Eq. (1), this relationship is given by

$$\frac{\Delta V_{O(droop)\max}}{V_O} = \frac{V_O(@ I_O = 0) - V_O(@ I_O = I_{O(FL)})}{V_O} = \frac{Kcs}{Kd} \cdot \frac{I_{O(FL)}}{V_O}, \qquad (3)$$

where $I_{O(FL)}$ is the full-load current of the individual power supply.

B. Current-Sharing Accuracy

Once the droop range of the load regulation characteristics of individual power supplies is maximized, the current-sharing accuracy of paralleled supplies is solely determined by their output-voltage set-point mismatching, as illustrated in Fig. 2. To facilitate the derivation of the relationship between the current-sharing accuracy and the output-voltage set-point mismatching, Fig. 8 shows the load regulation characteristics of N power supplies connected in parallel, which have different output-voltage set-points. It should be noted that all load-regulation characteristics in Fig. 8 are constrained between the load regulation characteristics of the power supply with the lowest output-voltage set point (LOWEST) and the power supply with the highest output-voltage set point (HIGHEST), i.e., within the defined output-voltage set-point accuracy range $\pm \Delta V_{O(SPA)}$.

From Fig. 8, it can be seen that the difference between the load currents of the power supply with the lowest output-voltage set point and the power supply with the highest

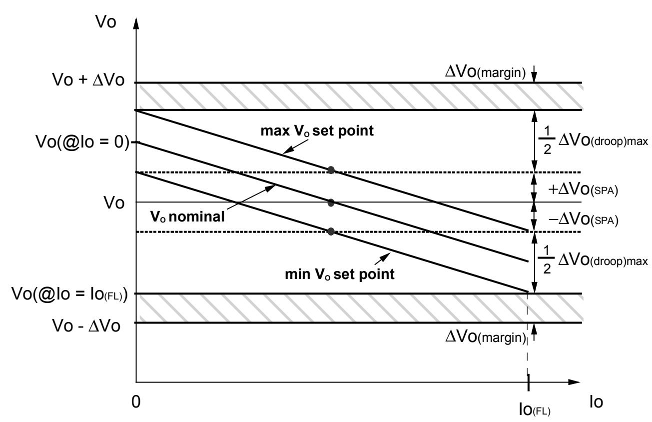

Fig. 6 Load regulation characteristic with maximum droop range taking into account output-voltage set-point accuracy and design margin.

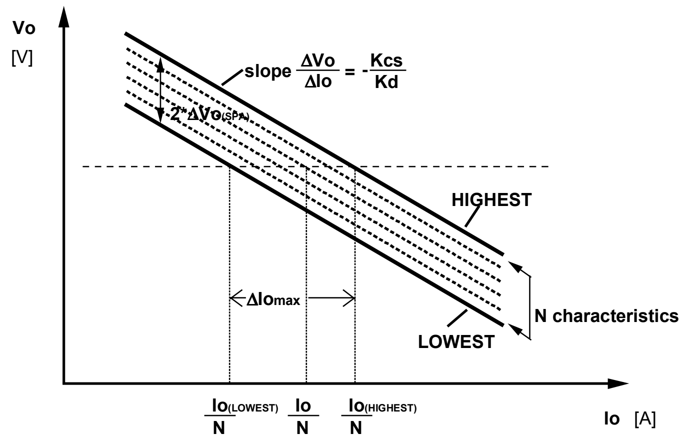

Fig. 8 Load regulation characteristics of N power supplies with mismatched output-voltage set points in $\Delta V_{O(SPA)}$ range.

output-voltage set point is

$$\left|\Delta I_{O\max}\right| = 2 * \Delta V_{O(SPA)} * Kd/Kcs \,. \tag{4}$$

The maximum relative current sharing error is then defined as

$$CS_{error} = \frac{\Delta I_{O\max}}{I_O/N} \,. \tag{5}$$

From Eq. (1), (4), and (6), the maximum relative current sharing error can be expressed as a function of the relative output-voltage set point, the relative output-voltage regulation, and the desired design margin.

$$CS_{error} = \frac{I_{O(FL)}}{I_O} \cdot \frac{\Delta V_{O(SPA)}/V_O}{(\Delta V_O/V_O - \Delta V_{O(SPA)}/V_O - \Delta V_{O(m\arg in)}/V_O)} * 100\% \,. \tag{6}$$

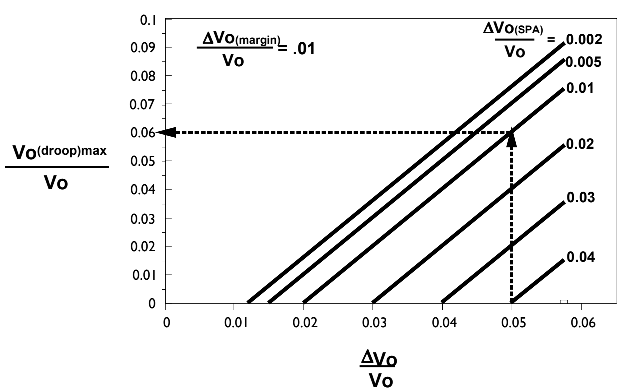

Fig. 7 Maximum relative output-voltage droop as a function of output-voltage range for different set-point accuracy's and 1% design margin. For $\Delta V_O/V_O = 0.05$ and $\Delta V_{O(SPA)}/V_O = 0.01$, $\Delta V_{O((droop)\max}/V_O = 0.06$, i.e., $\Delta V_{O((droop)\max} = 300\,mV$ for $V_O = 5V$.

As can be seen from Eq. 6, the relative current-sharing error depends on load current I_O. Its usefulness at the initial design stage is now readily apparent, since the current-sharing error can now be determined directly from the power supply specifications with a specific output-voltage set-point accuracy.

Fig. 9 shows full-load, current-sharing error as a function of relative output-voltage set-point accuracy for different relative output-voltage ranges, assuming a relative design margin of 1%. As can be seen from Fig. 9, for an output voltage V_O with a ±5% regulation range, the full-load relative current-sharing error is 33.3% if the set-point accuracy is ±1%. To keep the full load accuracy below 10%, it is necessary to have an output-voltage set-point accuracy better than ±0.35%. Generally, the described droop current-sharing method requires a very accurate adjustment of the output voltage to achieve good current sharing. It should be noted that the output-voltage adjustment must be stable over the entire temperature range and time.

C. Current-Sharing Circuit Implementation

A simple implementation of the current sharing circuit is shown in Fig. 10. In this circuit, Kd is implemented as the voltage divider consisting of fixed resistor R_{11} and R_{22}, and trim pot R_{TRIM} which is used to adjust the output voltage with the desired accuracy. Gain Kcs is implemented by a difference amplifier whose input is connected across sensing resistor Rs, which is used to sense the output current.

Using the superposition principle, gain Kd can be calculated by setting $I_O = 0$, whereas gain Kcs can be calculated by setting $V_O = 0$. Assuming that the output of the CA difference amplifier is zero when $I_O = 0$, gain Kd is

$$Kd = \frac{V_{REF}}{V_O(@I_O = 0)} = \frac{(R_2 \,//\, R_5)}{(R_2 \,//\, R_5 + R_1)} \,, \tag{7}$$

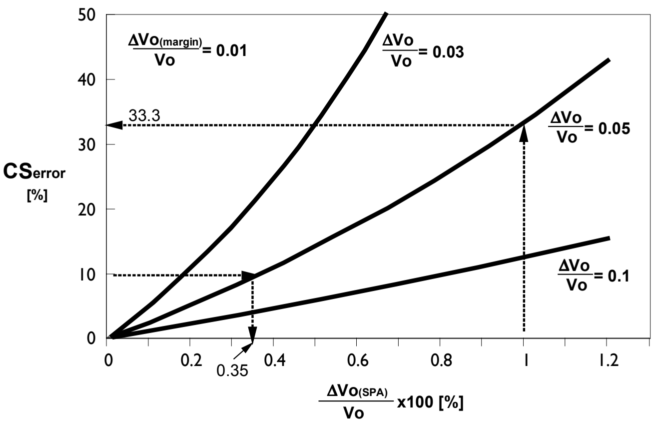

Fig. 9 Full-load, relative current-sharing error CS_{error} as a function of relative output-voltage set-point accuracy for relative output-voltage regulation range as parameter. Relative design margin of 1% is assumed. For $\Delta V_O / V_O = 0.05$ and $\Delta V_{O(SPA)} / V_O = 1\%$, $CS_{error} = 33.3\%$. To achieve $CS_{error} \leq 10\%$ for $\Delta V_O / V_O = 0.05$, $\Delta V_{O(SPA)} / V_O \leq 0.35\%$.

where R_1 is the total resistance of the branch between the output of the converter and the wiper of R_{TRIM}, and R_2 is the total resistance of the branch between the wiper and ground. When the output-voltage is set to zero to calculate Kcs, divider resistors R_1 and R_2 appear in parallel. Gain Kcs is given by

$$Kcs = \frac{V_{REF}}{I_O} = Rs \cdot \frac{R_3}{R_4} \cdot \frac{(R_1 // R_2)}{(R_1 // R_2 + R_5)} . \qquad (8)$$

It should be noted that in the current-sharing implementation in Fig. 10, coupling exists between gains Kd and Kcs. Generally, this coupling is undesirable because an adjustment made to R_{TRIM} to change the output-voltage set point (i.e., by changing gain Kd) results in a slight adjustment of gain Kcs. This coupling effect can be minimized if the components are chosen such that $\Delta R_{TRIM} << R_1, R_2 << R_5$.

D. Effect of Kd and Kcs Mismatching

So far, it has been assumed that all power supplies connected in parallel have identical gains Kd and Kcs. As a result, the slope of the load-regulation characteristic of all power supplies were the same, i.e., the characteristics were parallel as shown in Fig. 8. However, if gains Kd and Kcs of individual power supplies are not the same, the slope of the load-regulation characteristics of the power supply are either convergent or divergent. This tends to degrade the current sharing at either lighter loads or heavier loads, respectively.

To reduce this effect, the current-sharing circuit in Fig. 10 should be designed with enough margin while minimizing the coupling between the gains Kd and Kcs, and using resistors

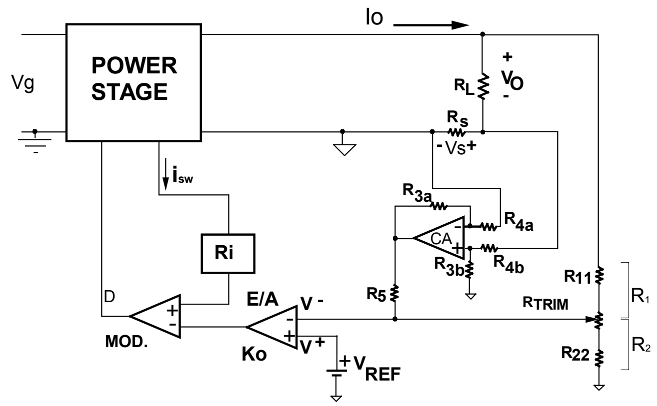

Fig. 10 Implementation of droop current sharing circuit.

and voltage reference with small tolerances, e.g., 1% or better.

E. Stability

Since in this approach, the droop characteristic is implemented in an open-loop fashion, the current sharing circuit does not affect the stability of the paralleled converters.

IV. Performance Evaluations

The droop current sharing implementation shown in Fig. 10 was applied to the 5-V output of three power supplies operating in parallel. The evaluation of the current sharing accuracy was performed at full load (i.e. the maximum individual output current $I_{OFL}^{ind} = 30\ A$), 75% of full load, half-load, and 25% of full load for relative output-voltage set-point accuracies $\Delta V_{O(SPA)} / V_O$ of ±0.25%, ±0.5%, and ±1%. In all evaluations it was assumed that the regulation range of the 5 V output is 5 V ± 0.25 V, i.e. 5 V ± 5%, and that the design margin is $\Delta V_{O(margin)} = \pm 50\ mV$, or $\Delta V_{O(margin)} / V_O = 0.01$.

A. Evaluation of ±0.25% Output-Voltage Set-Point Accuracy

The first step in designing the current-sharing circuit in Fig. 10 is to calculate the maximum relative output-voltage droop $\Delta V_{O(droop)max} / V_O$. Using Eq. 2 (or Fig. 7), the maximum relative output-voltage droop is 0.075, i.e., $\Delta V_{O(droop)max} = 0.375\ V$. Since from Eq. 7 and Fig. 6, Kd can be written as

$$Kd = \frac{V_{REF}}{V_O - \Delta V_O + \Delta V_{O(margin)} + \Delta V_{O(droop)\max} + \Delta V_{O(SPA)}} , \qquad (9).$$

Therefore, Kd = 0.4819 for $\Delta V_{O(SPA)}/V_O = 0.25\%$, i.e., $\Delta V_{O(SPA)} = 12.5\,mV$. Also from Eq. 3, Kcs can be calculated as Kcs = 0.006024. Once the values of Kd and Kcs are determined, the components R_S, R_1, R_2, R_3, R_4, and R_5 can be selected using Eqs. 7 and 8. To minimize the coupling effect between gains, R_5 was chosen to be much greater than R_1 and R_2. In addition, to decrease as much as possible the current sensing resistor value R_S to minimize unnecessary power dissipation, the gain of the current sharing amplifier should be high, typically on the order of 100. Table I summarizes parameter and component values of the current sharing circuit designed for ±0.25% output-voltage set-point accuracy. Once the component values of the current sharing circuit were determined, the output voltage of each of the three units was adjusted with trim pot R_{TRIM} to be ±0.25% apart at half load, i.e., at I_O = 15 A. The measured and calculated load regulation characteristics of units A, B, and C are shown in Fig. 11 to have very good agreement.

The relative current sharing error CS_{error} is determined directly from the measurements at approximately one-quarter, one-half, three-quarters and full load. A comparison of measured and predicted CS_{error} is presented in Table II and is shown to have very good agreement. It should be noted that

TABLE I

Parameter and component values for $\Delta V_{O(SPA)}/V_O = \pm 0.0025$

V_O	5 V	**Kd**	.4819
ΔV_O	.25 V	**Kcs**	.006024
$\Delta V_O/V_O$	.05	R_S	3.33 mΩ
$\Delta V_{O(margin)}$	.01	R_3	51kΩ
$\Delta V_{O(SPA)}/V_O$	.0025	R_4	510 Ω
$I_{O(FL)}^{ind}$	30 A	R_2	100 Ω
$\Delta V_{O(droop)max}/V_O$	.075	R_1	108 Ω
$\Delta V_{O(droop)max}$	.375 V	R_5	2.7 kΩ

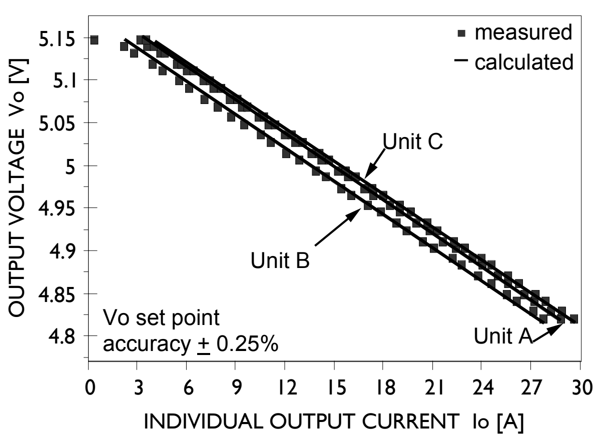

Fig. 11 Measured current sharing of Units A, B and C operating in parallel with relative output-voltage difference of 0.5%, i.e., $\Delta Vo_{(SPA)}/Vo$ = ±0.25%.

TABLE II

Measured CS_{error} and predicted CS_{error} for output-voltage set-point accuracy ±0.25%.

	CS_{error}	
Io [A]	**measured [%]**	**predicted [%]**
22	27	27.3
45	12.3	13.3
67	8.1	8.9
87	6.5	6.9

the predicted CS_{error} in Table II is a worst case prediction, since it is assumes the LOWEST and HIGHEST units to be at the limits of the output-voltage set-point accuracy.

Since $R_5 >> R_1$ and R_2, the coupling effect of Kd and Kcs is minimized. This minimized coupling effect allows the slopes of the load regulation characteristics of the three units to be nearly parallel, as shown in Fig. 11.

B. Evaluation of ±0.5% Output-Voltage Set-Point Accuracy

The design procedure is exactly the same as the previous example. For $\Delta V_{O(SPA)}/V_O = \pm 0.5\%$ the gain Kd was determined to be Kd = 0.4789, and gain Kcs was determined to be Kcs = 0.007024. The measured and calculated load regulation characteristics of units A, B, and C are shown in Fig. 12, whereas a comparison of measured and predicted CS_{error} is presented in Table III. The relative current sharing error CS_{error} is determined directly from the measurements at one-quarter, one-half, three-quarters and full load.

As in Fig. 11, the slope of the load regulation characteristic of each unit are nearly parallel. Trim-pot R_{TRIM} required more adjustment than the previous case (i.e., $\Delta V_{O(SPA)}/V_O = \pm 0.0025$) to be ±0.5% apart at half-load. Therefore the coupling effect between Kd and Kcs is more noticeable in Fig. 12 than in Fig. 11 because the slope of the individual load regulation characteristics are slightly more mismatched.

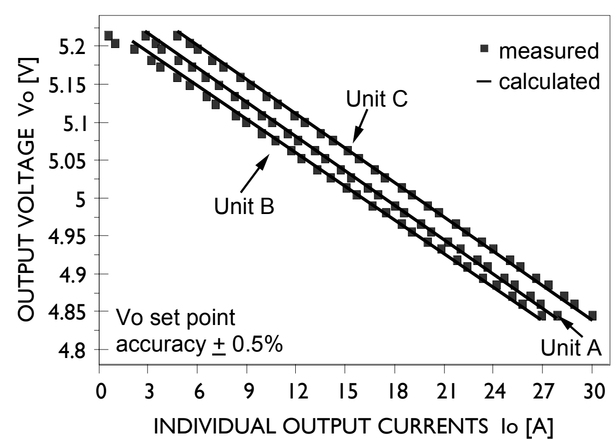

Fig. 12 Measured current sharing of Units A, B, and C operating in parallel with relative output-voltage difference of 1%, i.e., $\Delta Vo_{(SPA)}/Vo$ = ±0.5%.

TABLE III

Measured CS_{error} and predicted CS_{error} output-voltage set-point accuracy ±0.5%.

	CS_{error}	
Io [A]	**measured [%]**	**predicted [%]**
12	95.3	83.3
37	28.4	27
60	16.4	16.67
85	13	11.74

C. Evaluation of ±1% Output-Voltage Set-Point Accuracy

For $\Delta Vo_{(SPA)}/Vo = \pm 1\%$, the gain Kd was determined to be Kd = 0.4854, and gain Kcs was determined to be Kcs = 0.004854. The measured and calculated load regulation characteristics of units A, B, and C are shown in Fig. 13, whereas a comparison of measured and predicted CS_{error} is presented in Table IV.

The relative current sharing error is determined directly from the measurements at one-quarter, one-half, three-quarters and full load.

Figure 13 shows the most noticeable effect of the coupling between gains Kd and Kcs since R_{TRIM} required the most adjustment for $\Delta Vo_{(SPA)}/Vo = \pm 1\%$.

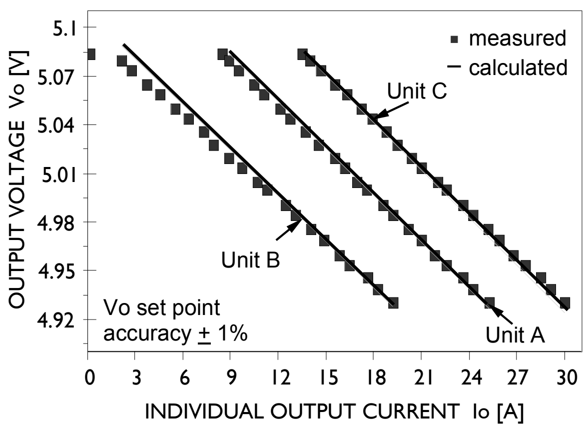

Fig. 13 Measured current sharing of Units A, B, and C operating in parallel with relative output-voltage difference of 2%, i.e., $\Delta Vo_{(SPA)}/Vo = \pm 1\%$.

TABLE IV

Measured CS_{error} and predicted CS_{error} for output-voltage set-point accuracy ±1%.

	CS_{error}	
Io [A]	**measured [%]**	**predicted [%]**
25	138	130
45	77	72.1
67	50	48.4
74.8	43.4	43.4

V. CONCLUSIONS

This paper presents the analysis and design of the droop current sharing technique. Generally, the droop current sharing technique is the simplest current sharing technique available. Its main feature is that it does not require any communication link (e.g., current-share bus) between the parallel modules. The droop current sharing technique uses the droop of the load-regulation line of paralleled power supplies to achieve an even distribution of the load current among them.

The key findings of this work can be summarized as follows:

- The current sharing accuracy is primarily determined by the output-voltage set-point accuracy. As a result, the droop current sharing technique requires precise adjustment of the initial output voltage. In addition, this adjustment needs to be stable over the entire operating temperature range.
- The droop current sharing technique can be a viable approach in applications where current-sharing accuracy of 10% or larger is acceptable.
- To achieve current sharing accuracy of 10%, the output voltage of the paralleled power supplies needs to be set within 0.35%.

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