Analysis of Bias Stress Instability in Amorphous InGaZnO Thin-Film Transistors

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***Abstract*—In this paper, we report an analysis of electrical bias stress instability in amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs). Understanding the variations of TFT characteristics under an electrical bias stress is important for commercial goals. In this experiment, the positive gate bias is initially applied to the tested a-IGZO TFTs, and subsequently, the negative gate bias is applied to the TFTs. For comparison with the subsequently negative-gate-bias-applied TFTs, another experiment is performed by directly applying the negative gate bias to the tested TFTs. For the positive gate bias stress, a positive shift in the threshold voltage ($V_{\rm th}$) with no apparent change in the subthreshold swing ($S_{\rm SUB}$) is observed. On the other hand, when the negative gate bias is subsequently applied, the TFTs exhibit higher mobility with no significant change in $S_{\rm SUB}$, whereas the shift of the $V_{\rm th}$ is much smaller than that in the positive gate bias stress case. These phenomena are most likely induced by positively charged donor-like subgap density of states and the detrapping of trapped interface charge during the positive gate bias stress. The proposed mechanism was verified by device simulation. Thus, the proposed model can explain the instability for both positive and negative bias stresses in a-IGZO TFTs.**

***Index Terms*—Density of states (DOS), electrical instability, InGaZnO (IGZO), modeling, thin-film transistors (TFTs).**

I. Introduction

TRANSPARENT oxide thin-film transistors (TFTs) are of great interest for the applications in flat-panel displays, optical sensors, and solar cells [1]–[4]. Recently, transparent ZnO-based TFTs have attracted much attention for flexible displays because they can be fabricated on plastic substrates at a low temperature and have the ability to be used to produce highly uniform and large area displays with a low production cost [1]. In particular, amorphous InGaZnO (a-IGZO) TFTs have arisen due to their high mobility and reasonable on/off ratio [1], [2]. However, like other TFTs, the characteristic variations of a-IGZO TFTs, such as the change of threshold voltage ($V_{\rm th}$), occur from bias stress, and those variations limit the application of a-IGZO TFTs in display applications, such as active matrix organic light-emitting diodes, resulting in the nonuniform pixel brightness [5].

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For commercialization, understanding the electrical stability of a-IGZO TFTs is important. Although several papers have explored the electrical stability of a-IGZO TFTs [6]–[8], there were limited papers explaining the origin of bias stress instability with numerical modeling [8]. In addition, only acceptor-like subgap density of states (DOS) was considered in a previous report since a-IGZO is an n-type semiconductor [8]. However, the acceptor-like subgap DOS does not offer a sufficient physical explanation of carrier transport in TFTs in this experiment.

In this paper, the positive gate bias is initially applied as an electrical stress, followed by the application of the negative gate bias stress to the tested a-IGZO TFTs. Additional donor-like subgap DOS is proposed as an additional conduction carrier transport mechanism for modeling to explain the change of TFT characteristics, and the effects of the electrical stress on a-IGZO TFTs are analyzed.

II. Experiments and Modeling Scheme

The tested a-IGZO TFTs in this paper were fabricated on a conventional staggered bottom gate structure [9], [10]. The test structures were fabricated on a glass substrate with a 250-nm Mo gate metal deposited by sputtering. The 200-nm SiN_X layer was then deposited as a gate dielectric by plasma-enhanced chemical vapor deposition. The a-IGZO channel was deposited by sputtering using a polycrystalline $In_2Ga_2ZnO_7$ target with a thickness of 40 nm. Finally, the source and drain electrodes were deposited via sputtering and patterned via photolithography and wet etching. The channel width (W) and length (L) of the TFTs were 50 and 25 μm, respectively. The current–voltage (I–V) and capacitance–voltage (C–V) characteristics at 1 MHz of the TFTs were measured using a Keithley 236 source measure unit and a Keithley 590 CV analyzer, respectively.

The gate electrode was stressed at 30 V for 10^4 s with grounded drain and source electrodes to test the electrical instability of the a-IGZO TFT. After the stress test, the gate electrode was subsequently stressed at -30 V for 10^4 s. Additionally, another a-IGZO TFT was stressed by directly applying the negative gate bias for comparison with the subsequently negative-gate-bias-applied TFT. The transfer ($I_{\rm DS}$–$V_{\rm GS}$) curve for the TFT was measured during the stress test. A commercial ATLAS device simulator produced by Silvaco, Inc., was used to analyze the stress mechanism [11]. Four parameterized components were used to express the subgap DOS, i.e., the acceptor-like exponential and Gaussian functions and the donor-like exponential and Gaussian functions.

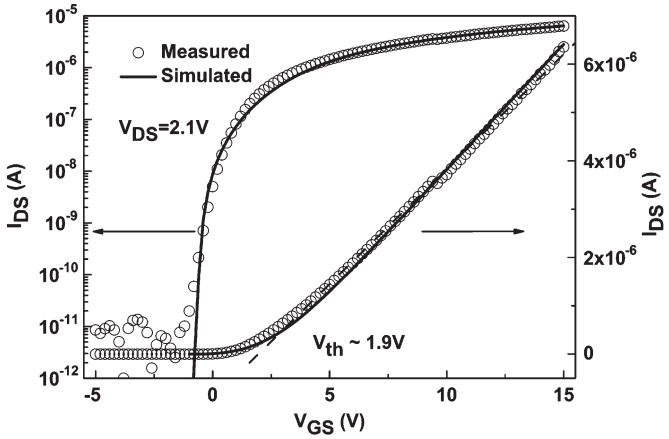

Fig. 1. Initial transfer characteristics for the tested TFT. (The sweep was performed at $V_{\rm DS} = 2.1$ V.)

The acceptor-like states can be modeled by a linear superposition of the exponential and the Gaussian functions described in [12]

$$g_A(E) = N_{\rm TA} \times \exp\left(\frac{E - E_C}{W_{\rm TA}}\right) + N_{\rm GA} \times \exp\left[-\left(\frac{E_{\rm GA} - E}{W_{\rm GA}}\right)^2\right] \quad (1)$$

where $N_{\rm TA}$ is the conduction band edge intercept density, E is the state energy, E_C is the conduction band edge, $W_{\rm TA}$ is the characteristic decay energy, $N_{\rm GA}$ is the total DOS, $E_{\rm GA}$ is the peak energy, and $W_{\rm GA}$ is the characteristic decay energy. The donor-like Gaussian function is described as

$$g_{\rm GD}(E) = N_{\rm GD} \times \exp\left[-\left(\frac{E - E_{\rm GD}}{W_{\rm GD}}\right)^2\right] \quad (2)$$

where $N_{\rm GD}$ is the total DOS, $E_{\rm GD}$ is the peak energy, and $W_{\rm GD}$ is the characteristic decay energy.

III. Results and Discussion

A. Initial Test

Prior to modeling of the gate bias stress test, the initial transfer characteristic is modeled with the ATLAS device simulator. Fig. 1 shows the transfer characteristics of the tested TFT.

The apparent field-effect mobility ($\mu_{\rm FE}$) is determined by

$$\mu_{\rm FE} = \frac{G_m}{\left(\frac{W}{L}\right) C_i V_{\rm DS}} \quad (3)$$

where G_m, C_i, and $V_{\rm DS}$ are the transconductance, gate capacitance per unit area, and drain bias, respectively. For simplicity of comparison between the experimentally measured mobility and the simulation mobility parameters, the maximum $\mu_{\rm FE}$ ($\mu_{\rm FE\,max}$) and the constant electron mobility (μ_n) [12] are used in this paper, respectively. $\mu_{\rm FE\,max}$ is defined as the maximum value of extracted $\mu_{\rm FE}$ in the area of the measured bias. The $\mu_{\rm FE\,max}$, $V_{\rm th}$, and subthreshold swing ($S_{\rm SUB}$) before the stress test are 3.7 cm^{2}V^{-1}s^{-1}, ~1.9 V, and ~428 mV/dec, respectively. After fitting the initial data, the acceptor-like subgap DOS parameters are extracted with $N_{\rm TA} = 2.46 \times 10^{18}$ cm^{-3}eV^{-1}, $W_{\rm TA} = 0.07$, $N_{\rm GA} = 10^{16}$ cm^{-3}eV^{-1}, $W_{\rm GA} = 0.86$, and $\mu_n = 3.7$ cm^{2}V^{-1}s^{-1}. For the a-IGZO TFT, $E_{\rm GA}$ is fixed at E_C to represent gradually descending deep-gap states. These parameters are consistent with other previously reported values [12], [13].

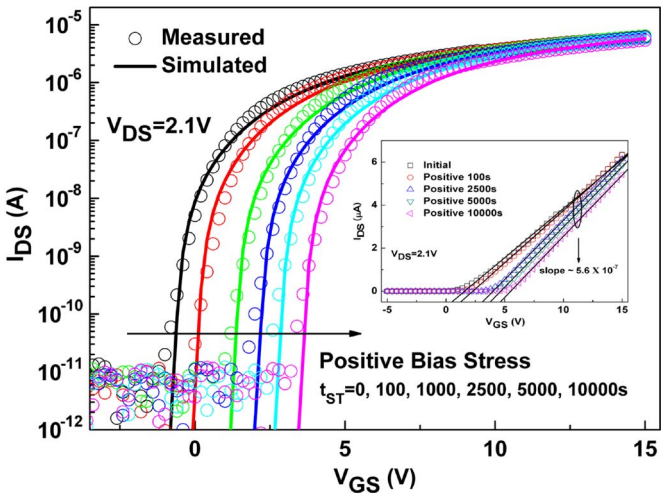

Fig. 2. Transfer characteristics of the tested TFT for positive gate bias stress test ($V_{\rm GS} = 30$ V).

B. Positive Gate Bias Stress

Fig. 2 shows the plots of $[\log(I_{\rm DS}) - V_{\rm GS}]$, and the inset shows the linear plots of the transfer characteristics before and after the positive gate bias stresses.

The transfer curves are shifted in the positive direction by incrementing the positive gate bias stress time with no definite change in $S_{\rm SUB}$. In addition, the slope of the inset curves does not change much despite the increase of the positive gate bias stress time indicating that the change of mobility can be ignored [14].

In previous reports, two main mechanisms for the shift in $V_{\rm th}$ were identified. One is carrier trapping at the channel/dielectric interface [15], [16], and the other is the creation of additional defect states in the deep-gap states at or near the channel/dielectric interface [17], [18]. A lack of $S_{\rm SUB}$ variation indicates that additional defect states are not generated [6], [8], and therefore, the modeling of positive gate bias stress is analyzed by just implying the channel/dielectric interface trap charge ($Q_{\rm it}$) without changing the acceptor-like subgap DOS parameters extracted from the initial data. The simulated data fit well with the addition of $Q_{\rm it}$, as shown in Fig. 2. Table I represents the extracted $Q_{\rm it}$. The positive $V_{\rm th}$ shift with increasing $Q_{\rm it}$ is explained by negative charge screening of the applied gate bias [7]. Thus, an additional gate bias is required to turn on the device due to the screening of the added trap charges.

C. Negative Gate Bias Stress

After the positive gate bias stress, the negative gate bias is subsequently applied to the tested a-IGZO TFT. Fig. 3 shows

TABLE I
SUMMARY OF THE EXTRACTED PARAMETERS FOR POSITIVE GATE BIAS STRESS TEST (FOR THE INITIAL DATA, $Q_{\rm it}$ IS SET TO BE ZERO)

Positive gate bias stress time (second)	Increment ratio of $Q_{\rm it}$ to the initial state (before stress) (cm^{-2})
1.0×10^{2}	-1.6×10^{11}
1.0×10^{3}	-4.2×10^{11}
2.5×10^{3}	-5.9×10^{11}
5.0×10^{3}	-7.3×10^{11}
1.0×10^{4}	-8.7×10^{11}

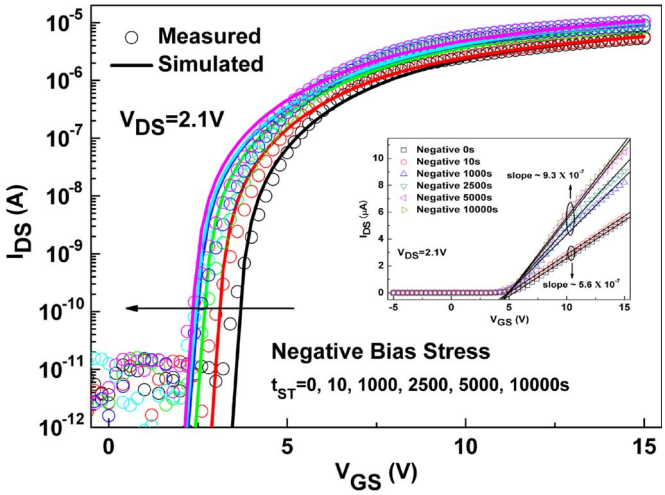

Fig. 3. Transfer characteristics after negative gate bias stress test ($V_{\rm GS} = -30$ V) where data at $t_{\rm ST} = 0$ indicate the data after positive gate bias stress of 10^4 s.

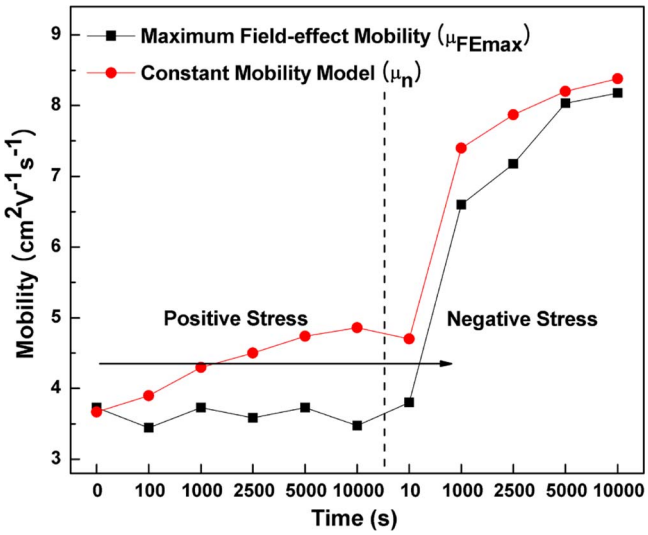

Fig. 4. Comparison of $\mu_{\rm FE\,max}$ and μ_n for positive and negative gate bias stresses.

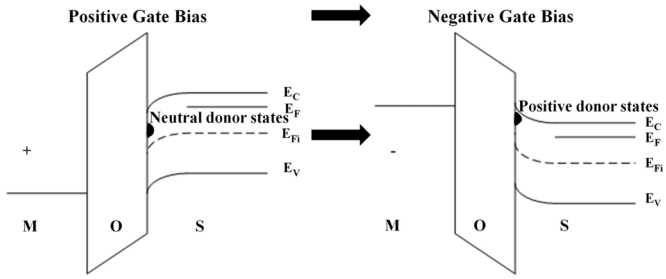

Fig. 5. Schematic diagram illustrating the proposed mechanism of band bending on the channel/dielectric interface when applying positive and negative gate bias stresses.

the transfer characteristics when the negative bias is stressed for the tested TFT, and the inset shows the linear plots of the transfer characteristics.

$V_{\rm th}$ is shifted negatively when it shows a relatively small shift in the positive gate bias stress. The increase of the slope at the linear transfer curves as the negative gate bias stress time is increased indicates that the current level increases not only from the shift of $V_{\rm th}$ but also from the increase of $\mu_{\rm FE}$[14]. The comparison of the $\mu_{\rm FE\,max}$ and the constant μ_n at the tested experiments is shown in Fig. 4. It is found that μ_n well follows the large increase of $\mu_{\rm FE\,max}$ when the stress changes from a positive to a negative gate bias. Although $\mu_{\rm FE\,max}$ and μ_n are a little different in some regions due to the modeling and measurement errors, the overall trends of μ_n are well matched with $\mu_{\rm FE\,max}$ for both the positive and negative gate bias stress regions to sufficiently support the proposed model. As shown in Fig. 4, the mobility rapidly increases after the negative gate stresses are applied. The increase of mobility can be explained by the previously reported characteristics of IGZO. It is reported that IGZO has unique characteristics in that the mobility increases as the carrier concentration increases because the carrier transport in IGZO is governed by percolation conduction over the distribution of potential barriers around the conduction band edge [1]. Considering the relationship between the mobility and carrier concentration, a donor-like Gaussian function is introduced which behaves as an additional conduction carrier due to band bending caused by the gate bias stress.

Fig. 5 shows the proposed mechanism for band bending on the channel/dielectric interface. In general, the donor state is neutral if the Fermi level is above the state and becomes positively charged if the Fermi level is below the state [19]. Kamiya *et al.* reported that the donor states of a-IGZO are ~0.11 eV below the conduction band minimum [20]. Fig. 5 shows the two band bending diagrams when the positive gate bias is applied and the negative gate bias is subsequently applied. In the positive gate bias stress, each donor state is neutral because the Fermi level is above the states. However, when the negative gate bias is applied, the donor states are positively charged due to band bending. These positively charged donor states can be thought of as providing additional carriers for the conduction of the a-IGZO TFT, showing the rapid increase of $\mu_{\rm FE}$ during the negative gate bias stress.

In order to confirm this proposed conduction mechanism, the model for the negative gate bias stress is executed with the additional parameters. The acceptor-like subgap DOS parameters are also fixed due to the lack of significant change in $S_{\rm SUB}$.

It is assumed that, during the negative gate bias stress, $Q_{\rm it}$ is detrapped gradually by the opposite gate bias, and positively charged donor states are increased with increasing negative gate bias stress time. To confirm the assumption, an additional experiment is performed by directly applying the negative gate bias to the tested TFT. As shown in Fig. 6, the $S_{\rm SUB}$ and $V_{\rm th}$

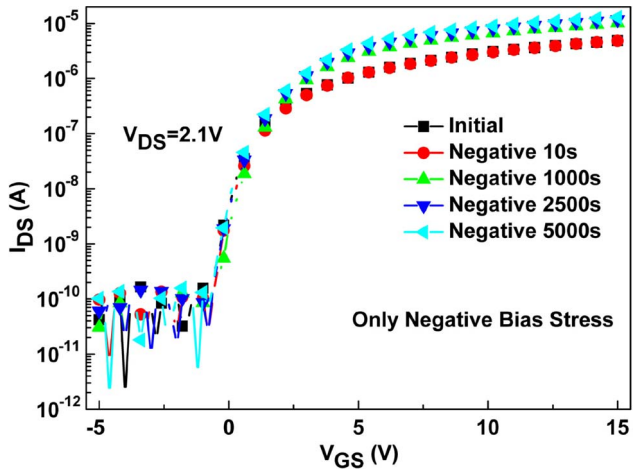

Fig. 6. Transfer characteristics of initial TFT with directly applying negative gate bias ($V_{\rm GS} = -30$ V).

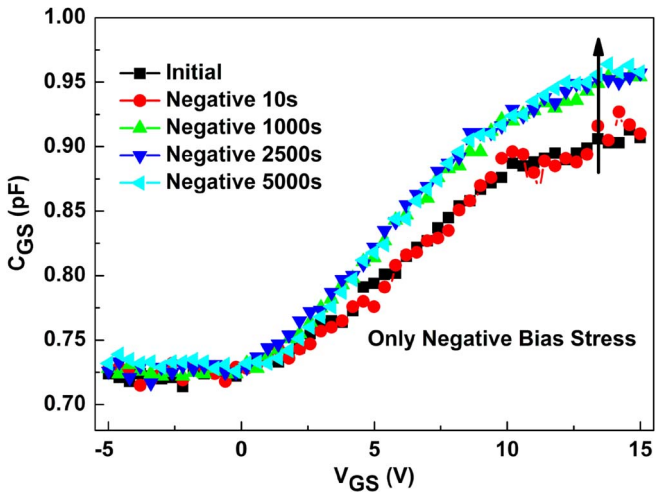

Fig. 7. Gate-to-source capacitance ($C_{\rm GS}$) versus $V_{\rm GS}$ with directly applying negative gate bias ($V_{\rm GS} = -30$ V).

almost remain the same in spite of the increase of the negative gate bias stress time which is similar with previously reported results [7]. However, it is observed that the current level is increased. By comparing Fig. 3 with Fig. 6, it can be concluded that the cause of the negative $V_{\rm th}$ shift in the subsequently negative-gate-bias-applied TFT is the detrapping of the $Q_{\rm it}$ during the positive gate bias stress.

The gate-to-source capacitance ($C_{\rm GS}$) with directly applying the negative gate bias is also measured to verify the increment of positively charged donor states, and the results are shown in Fig. 7.

It is observed that the maximum value of $C_{\rm GS}$ is increased as the negative gate bias stress time is increased. It is indicating that the positively charged donor states acting as the additional conduction carriers are increased. Thus, it is verified that the positively charged donor states are increased with increasing negative gate bias stress time.

The increase of positively charged donor states is represented by increasing $N_{\rm GD}$ as shown in (2). The increase of $N_{\rm GD}$ indicates the increase of the total donor states. In reality, it is assumed that positively charged donor states are gradually

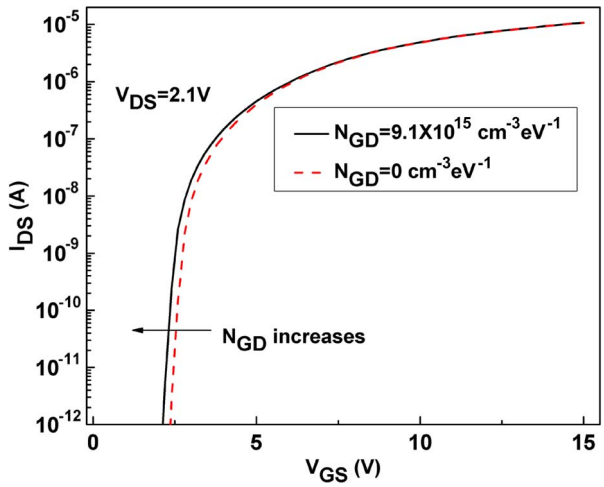

Fig. 8. Simulation of transfer characteristics with and without $N_{\rm GD}$.

increased with no change of the total donor states as the negative gate bias stress time increases. Due to the same Fermi level for all modeled transfer curves at the same $V_{\rm GS}$ because of the same band bending of the channel/dielectric interface region in simulation and modeling, $N_{\rm GD}$ increased in this paper can be represented by more positively charged donor states with fixed $N_{\rm GD}$. Thus, the total donor states which can be represented by $N_{\rm GD}$ are increased to reflect more positively charged donor states. In order to identify the effect of the increase in number of $N_{\rm GD}$ on the device characteristics in the absence of an increase in mobility, the simulation results with and without $N_{\rm GD}$ are shown in Fig. 8. It is shown that the increase of $N_{\rm GD}$ behaves as additional conduction carriers. The sensitivity analysis is also performed using the Silvaco optimizer simulation program to analyze the effects of mobility and $N_{\rm GD}$ numerically [11]. The sensitivity is calculated as the percentage change in a target value divided by the percentage change in a single input value. In this case, each effect of μ_n and $N_{\rm GD}$ on the transfer characteristics is calculated. As a result, it is found that the μ_n sensitivity is 630%, and the $N_{\rm GD}$ sensitivity is 320% for the sensitivity simulation of the negative gate bias stress for 5000 s. Based on the result from the sensitivity analysis, it is found that, even though the effect of μ_n is larger than that of $N_{\rm GD}$, $N_{\rm GD}$ cannot be ignored as a model parameter.

Based on the results shown in Fig. 3, the simulated values are comparably matched with the measured data. The donor-like Gaussian function $E_{\rm GD}$ in (2) is set to be 2.9 eV (because the energy bandgap of a-IGZO is set to be 3 eV), as reported in a previous work [20]. The extracted values of $Q_{\rm it}$, $N_{\rm GD}$, and $W_{\rm GD}$ are summarized in Table II. In Table II, the difference of $N_{\rm GD}$ ($\Delta N_{\rm GD}$) in between 1000 and 2500 s is larger than $\Delta N_{\rm GD}$ in between 10 to 1000 s, while the difference of μ_n ($\Delta\mu_n$) in between 1000 and 2500 s is smaller than $\Delta\mu_n$ in between 10 and 1000 s. It seems to be inconsistent that μ_n increases as $N_{\rm GD}$ increases. However, in this paper, $Q_{\rm it}$ and $N_{\rm GD}$ are both considered in the negative gate bias stress modeling due to the preceding positive gate bias stress test. In the simulation environment, like increasing $N_{\rm GD}$, the decrease of $Q_{\rm it}$ also results in the increase of current because $V_{\rm th}$ shifts to a negative position. In Fig. 3, it is shown that the difference

TABLE II
SUMMARY OF THE EXTRACTED PARAMETERS FOR NEGATIVE GATE BIAS STRESS

Negative gate bias stress time (second)	Qit (cm^{-2})	N_{GD} ($cm^{-3}eV^{-1}$)	W_{GD} (eV)
10	-8.0×10^{11}	4.8×10^{15}	0.1
1.0×10^{3}	-7.2×10^{11}	5.5×10^{15}	0.1
2.5×10^{3}	-6.8×10^{11}	8.0×10^{15}	0.1
5.0×10^{3}	-6.7×10^{11}	8.9×10^{15}	0.1
1.0×10^{4}	-6.7×10^{11}	9.1×10^{15}	0.1

of the $V_{\rm th}$ shift ($\Delta V_{\rm th}$) in between 10 and 1000 s is larger than $\Delta V_{\rm th}$ in between 1000 and 2500 s. Due to the combined effect of $Q_{\rm it}$ and $N_{\rm GD}$ in the negative gate bias stress, the tendency of $\Delta N_{\rm GD}$ and $\Delta\mu_n$ cannot be accurately matched.

IV. CONCLUSION

In this paper, the electrical instability in a-IGZO TFTs has been analyzed by testing, device modeling, and simulation. The TFT showed a parallel shift in $V_{\rm th}$ under the positive gate bias stress indicating the charge trapping of the channel/dielectric interface. When the negative gate bias stress was applied, the increase of $\mu_{\rm FE}$ was observed, and the mechanism was not investigated previously. In this paper, a donor-like Gaussian function has been proposed for the model, and the proposed mechanism of band bending on the channel/dielectric interface has been verified by the device modeling and simulation. Considering the reported IGZO unique characteristics, the tendency toward increasing mobility under the negative gate bias stress can be explained by the increase of positively charged donor states expressing additional conduction carriers. Therefore, it has been concluded that the proposed model sufficiently represents the electrical instability of a-IGZO TFTs by simply indicating the $Q_{\rm it}$ and the subgap DOS parameters.

REFERENCES

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, Nov. 2004.

[2] M. K. Kim, J. H. Jeong, H. J. Lee, T. K. Ahn, H. S. Shin, J. S. Park, J. K. Jeong, Y. G. Mo, and H. D. Kim, "High mobility bottom gate InGaZnO thin film transistors with SiO_X etch stopper," *Appl. Phys. Lett.*, vol. 90, no. 21, p. 212114, May 2007.

[3] R. L. Hoffman, B. H. Norris, and J. F. Wager, "ZnO-based transparent thin-film transistors," *Appl. Phys. Lett.*, vol. 82, no. 5, pp. 733–735, Feb. 2003.

[4] E. Fortunato, P. Barquinha, A. Pimentel, A. Goncalves, A. Marques, L. Pereira, and R. Martins, "Fully transparent ZnO thin-film transistor produced at room temperature," *Adv. Mater.*, vol. 17, no. 5, pp. 590–594, Mar. 2005.

[5] M. E. Lopes, H. L. Gomes, M. C. Medeiros, P. Barquinha, L. Pereira, E. Fortunato, R. Martins, and I. Ferreira, "Gate-bias stress in amorphous oxide semiconductors thin-film transistors," *Appl. Phys. Lett.*, vol. 95, no. 6, p. 063502, Aug. 2009.

[6] T.-C. Fung, K. Abe, H. Kumomi, and J. Kanicki, "Electrical instability of RF sputter amorphous In–Ga–Zn–O thin-film transistors," *J. Display Technol.*, vol. 5, no. 12, pp. 452–461, Dec. 2009.

[7] A. Suresh and J. F. Muth, "Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors," *Appl. Phys. Lett.*, vol. 92, no. 3, p. 033502, Jan. 2008.

[8] K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, "Origins of threshold voltage shifts in room-temperature deposited and annealed a-In–Ga–Zn–O thin-film transistors," *Appl. Phys. Lett.*, vol. 95, no. 1, p. 013502, Jul. 2009.

[9] S. I. Kim, J.-S. Park, C. J. Kim, J. C. Park, I. Song, and Y. S. Park, "High reliable and manufacturable gallium indium zinc oxide thin-film transistors using the double layers as an active layer," *J. Electrochem. Soc.*, vol. 156, no. 3, pp. H184–H187, Jan. 2009.

[10] J.-S. Park, T.-W. Kim, D. Stryakhilev, J.-S. Lee, S.-G. An, Y.-S. Pyo, D.-B. Lee, Y. G. Mo, D.-U. Jin, and H. K. Chung, "Flexible full color organic light-emitting diode display on polyimide plastic substrate driven by amorphous indium gallium zinc oxide thin-film transistors," *Appl. Phys. Lett.*, vol. 95, no. 1, p. 013503, Jul. 2009.

[11] *ATLAS User's Manual*, Silvaco Int., Santa Clara, CA, 2008.

[12] H.-H. Hsieh, T. Kamiya, K. Nomura, H. Hosono, and C.-C. Wu, "Modeling of amorphous $InGaZnO_4$ thin film transistors and their subgap density of states," *Appl. Phys. Lett.*, vol. 92, no. 13, p. 133503, Mar. 2008.

[13] K. Jeon, C. Kim, I. Song, J. Park, S. Kim, S. Kim, Y. Park, J.-H. Park, S. Lee, D. M. Kim, and D. H. Kim, "Modeling of amorphous InGaZnO thin-film transistors based on the density of states extracted from the optical response of capacitance-voltage characteristics," *Appl. Phys. Lett.*, vol. 93, no. 18, p. 182102, Nov. 2008.

[14] J.-M. Lee, I.-T. Cho, J.-H. Lee, and H.-I. Kwon, "Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in InGaZnO thin film transistors," *Appl. Phys. Lett.*, vol. 93, no. 9, p. 093504, Sep. 2008.

[15] M. J. Powell, "Charge trapping instabilities in amorphous silicon–silicon nitride thin-film transistors," *Appl. Phys. Lett.*, vol. 43, no. 6, pp. 597–599, Sep. 1983.

[16] F. R. Libsch and J. Kanicki, "Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors," *Appl. Phys. Lett.*, vol. 62, no. 11, pp. 1286–1288, Mar. 1993.

[17] C. van Berkel and M. J. Powell, "Resolution of amorphous silicon thin-film transistor instability mechanisms using ambipolar transistors," *Appl. Phys. Lett.*, vol. 51, no. 14, pp. 1094–1096, Oct. 1987.

[18] M. J. Powell, C. van Berkel, I. D. French, and D. H. Nicholls, "Bias dependence of instability mechanisms in amorphous silicon thin-film transistors," *Appl. Phys. Lett.*, vol. 51, no. 16, pp. 1242–1244, Oct. 1987.

[19] D. A. Neamen, *Semiconductor Physics and Devices*, 3rd ed. New York: McGraw-Hill, 2003, p. 482.

[20] T. Kamiya, K. Nomura, and H. Hosono, "Electronic structures above mobility edges in crystalline and amorphous In–Ga–Zn–O: Percolation conduction examined by analytical model," *J. Display Technol.*, vol. 5, no. 12, pp. 462–467, Dec. 2009.

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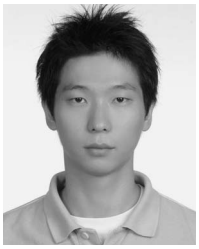

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