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Analysis of Buck Converters for On-Chip Integration With a Dual Supply Voltage Microprocessor

Volkan Kursun, Siva G. Narendra, Vivek K. De, and Eby G. Friedman

***Abstract*—An analysis of an on-chip buck converter is presented in this paper. A high switching frequency is the key design parameter that simultaneously permits monolithic integration and high efficiency. A model of the parasitic impedances of a buck converter is developed. With this model, a design space is determined that allows integration of active and passive devices on the same die for a target technology. An efficiency of 88.4% at a switching frequency of 477 MHz is demonstrated for a voltage conversion from 1.2–0.9 volts while supplying 9.5 A average current. The area occupied by the buck converter is 12.6 mm^2 assuming an 80-nm CMOS technology. An estimate of the efficiency is shown to be within 2.4% of simulation at the target design point. Full integration of a high-efficiency buck converter on the same die with a dual-$V_{\rm DD}$ microprocessor is demonstrated to be feasible.**

***Index Terms*—Buck converter, dc-dc converter, dual supply voltage, high efficiency, integrated inductors, low power, low voltage, modeling of dc–dc converters, monolithic dc–dc conversion, multiple supply voltages, power supply, supply voltage scaling, switching dc–dc converters, voltage regulator.**

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I. Introduction

Decreasing the power dissipation and current demand of high-performance microprocessors are the two primary reasons for implementing a dual-$V_{\rm DD}$ microprocessor [1]. Due to the quadratic dependence of the dynamic switching power and the more than linear dependence of the subthreshold and gate oxide leakage power on the supply voltage, power dissipation is significantly reduced when portions of a microprocessor operate at a lower voltage level. A linear relationship exists between the current demand and power consumption of a microprocessor. Reducing the maximum power consumption, therefore, reduces the maximum current required by a microprocessor, thereby decreasing the number of power and ground pads on a microprocessor die. In order to maximize this reduction in current, the lower voltage supply of a dual-$V_{\rm DD}$ microprocessor should be integrated on the same die with the microprocessor. Moreover, in order to fully exploit expected reductions in power and current, the energy overhead of an integrated dc–dc converter to produce a second voltage level must be minimized.

Buck converters are popular due to the high efficiency and good output voltage regulation characteristics of these circuits [2]–[5]. In single power-supply microprocessors, the primary power supply is typically an external (nonintegrated) buck converter. In a dual-$V_{\rm DD}$ microprocessor, the choices are either a second external dc–dc converter, or a monolithic (both active and passive devices on the same die as the load) dc–dc converter.

In a typical nonintegrated switching dc–dc converter, significant energy is dissipated by the parasitic impedances of the interconnect among the nonintegrated devices (the filter inductor, filter capacitor, power transistors, and pulse width modulation circuitry) [3]. Moreover, the integrated active devices of a pulsewidth modulation circuit are typically fabricated in an old technology with poor parasitic impedance characteristics.

Integrating a dc–dc converter with a microprocessor can potentially lower the parasitic losses as the interconnect between (and within) the dc–dc converter and the microprocessor is reduced. Additional energy savings can be realized by utilizing advanced deep submicrometer fabrication technologies with lower parasitic impedances. The efficiency attainable with a monolithic dc–dc converter, therefore, is higher than a nonintegrated dc–dc converter.

Fabrication of a monolithic switching dc–dc converter, however, imposes a challenge as the on-chip integration of inductive and capacitive devices is required for energy storage and output signal filtering. Integrated capacitors and inductors above certain values are not acceptable due to the tight area constraints that exist within high performance microprocessor integrated circuits (ICs). Another significant issue with integrated inductors is the poor parasitic impedance characteristics which can degrade the efficiency of a voltage regulator. The value, physical size, and parasitic impedances of the passive devices required to implement a buck converter, however, are reduced with increasing switching frequency [2]–[4]. Integrated capacitors of small value (used for decoupling and constrained by the available area on the microprocessor die) are available in high-performance microprocessors [6]. Furthermore, with the use of magnetic materials, a new integrated microinductor technology with relatively small parasitic impedances and higher cutoff frequencies (over 3 GHz) has recently been reported [7]. Therefore, employing switching frequencies higher than the typical switching frequency range found in conventional dc–dc converters permits the on-chip integration of active and passive devices of a buck converter onto the same die as a high-performance microprocessor.

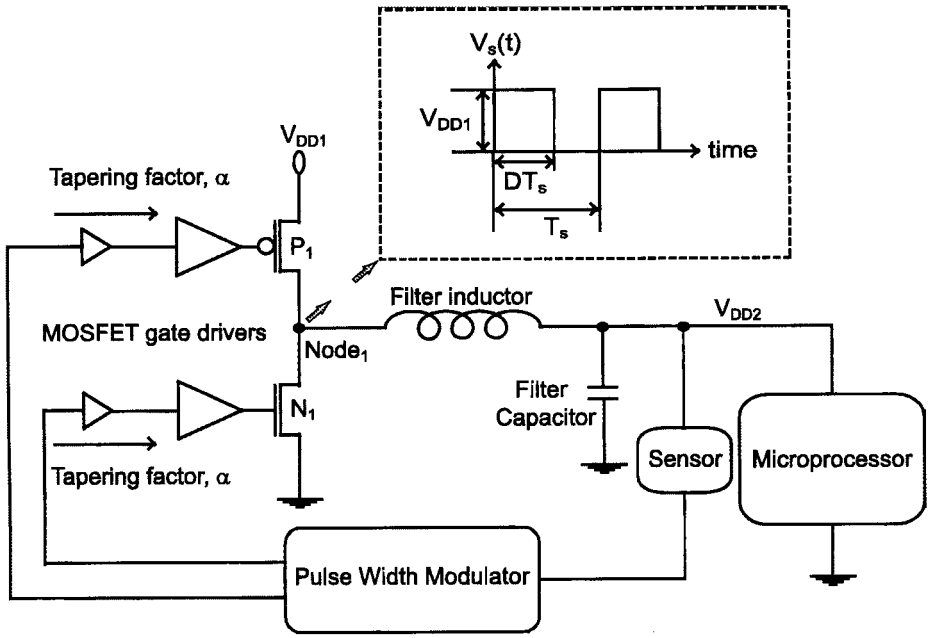

Fig. 1. Buck converter circuit.

The efficiency characteristics of a buck converter, however, change dramatically as the switching frequency is increased. The switching frequency of dc–dc converters has been, so far, limited to the range from a few kilohertz to a few megahertz [2], [3]. Based on oversimplified circuit models of switching dc–dc converters, a general assumption in the research community has been that a high switching frequency dc–dc converter is not feasible with the expectation that the efficiency would degrade significantly due to the increased power losses at high switching frequencies [2], [3]. The low switching frequency range utilized in typical nonintegrated dc–dc converters has been a result of this assumption rather than based on a study modeling the variation of the dc–dc converter efficiency as a function of the switching frequency. Comprehensive circuit models of the parasitic impedances of monolithic switching dc–dc converters are necessary in order to characterize an optimum circuit configuration with the maximum efficiency.

A parasitic model is presented in this paper to analyze the frequency dependent efficiency characteristics of a buck converter. A closed-form expression that characterizes the power consumption of a monolithic buck converter is proposed. The effects of scaling the active and passive devices and the related switching and conduction losses on the total power characteristics of a buck converter are examined. With the proposed buck converter energy model, a design space which characterizes the integration of both active and passive devices on the same die as a dual-$\mathrm{V_{DD}}$ microprocessor while maintaining high efficiency is determined for an 80-nm CMOS technology. An efficiency of 88.4% is shown for a voltage conversion from 1.2 to 0.9 V while supplying 9.5 A maximum current. The area of the buck converter at the target design point is 12.6 mm^2 which is primarily occupied by a 100-nF filter capacitor. Full integration of a high-efficiency buck converter on the same die as a dual-$\mathrm{V_{DD}}$ microprocessor is demonstrated to be feasible.

The basic operation of a buck converter is described in Section II. The proposed parasitic circuit model and a closed form expression of the average power dissipation of a buck converter are presented in Section III. With the proposed analytic model, the efficiency characteristics of a buck converter are investigated in Section IV. Simulation results at a target design point are presented in Section V. Finally, some conclusions are offered in Section VI.

II. Operation of a Buck Converter

A buck converter is a standard switching dc–dc converter circuit topology with high efficiency and good output voltage regulation characteristics. Buck converters are used to generate a regulated dc output supply voltage from a higher (possibly nonregulated) dc input voltage. A typical buck converter circuit is shown in Fig. 1.

The operation of a buck converter circuit behaves in the following manner. The power MOSFETs, labeled as $\mathrm{P_1}$ and $\mathrm{N_1}$ in Fig. 1, produce an ac signal at $\mathrm{Node_1}$ by a nonoverlapping switching action controlled by the pulse width modulator. The ac signal at $\mathrm{Node_1}$ is applied to a second-order low-pass filter composed of an inductor and a capacitor. The low-pass filter passes to the output the dc component of the ac signal at $\mathrm{Node_1}$. A small amount (assuming the filter corner frequency is much smaller than the switching frequency f_s of the power MOSFETs) of high-frequency harmonics generated by the switching action of the power MOSFETs also reaches the output due to the nonideal characteristics of the output filter.

The buck converter output voltage $V_{DD2}(t)$ is [2]

$$V_{DD2}(t) = V_{DD2} + V_{\mathrm{ripple}}(t) \tag{1}$$

where V_{DD2} is the dc component of the output voltage and $V_{\mathrm{ripple}}(t)$ is the voltage ripple waveform observed at the output due to the nonideal characteristics of the output filter. The dc component of the output voltage is [2]

$$V_{DD2} = \frac{1}{T_s}\int_0^{T_s} V_s(t)dt = DV_{DD1} \tag{2}$$

where $V_s(t)$ is the ac signal generated at $\mathrm{Node_1}$ and T_s, D, and V_{DD1} are the period, duty cycle, and amplitude, respectively, of $V_s(t)$. As given by (2), any positive output dc voltage less than V_{DD1} can be generated by a buck converter by varying the duty cycle D.

The power transistors are typically large in physical size with a high parasitic capacitance. To control the operation of the power transistors, a series of MOSFET gate drivers are used. The driver buffers are tapered [8], [11] as shown in Fig. 1. The gate driver buffers are controlled by a pulse width modulator (PWM). Using a fast feedback circuit, the PWM generates the necessary control signals for the power

MOSFETs such that a square wave with an appropriate duty cycle is produced at Node$_1$. During operation of the buck converter, the duty cycle and/or switching frequency are modified in order to maintain the output voltage at the desired value (output regulation) whenever variations in the load current and input supply voltage V_{DD1} are detected. Due to the strong dependence of the output voltage on the switching duty cycle [see (2)], precise output voltage regulation can be maintained by a buck converter with a fast feedback circuit [2].

The inductor current $i_L(t)$, output voltage $V_{DD2}(t)$, and capacitor current $i_C(t)$ waveforms are shown in Fig. 2. The output voltage ripple is exaggerated in Fig. 2 for better illustration. The amplitude of the output voltage ripple ΔV_{DD2} is maintained at a small level (less than 1%) as compared to the output dc voltage V_{DD2} in a typical buck converter.

The filter capacitance is chosen such that the impedance of the capacitor is much smaller than the load impedance. The ac component of the inductor current, therefore, passes through the filter capacitor while the dc component I passes through the load (see Fig. 2). The output voltage increases while the filter capacitor is being charged when the inductor current rises above I. Similarly, the output voltage falls while the filter capacitor is being discharged when the inductor current decreases below I.

Expressions for the inductor current ripple Δi and the amplitude of the output voltage ripple ΔV_{DD2} (see Fig. 2) are, respectively

$$\Delta i = \frac{(V_{DD1} - V_{DD2})\, D}{2Lf_s} \tag{3}$$

$$\Delta V_{DD2} = \frac{(V_{DD1} - V_{DD2})\, D}{16LC{f_s}^2} = \frac{\Delta i}{8Cf_s} \tag{4}$$

where L is the filter inductance, C is the filter capacitance, and f_s is the switching frequency.

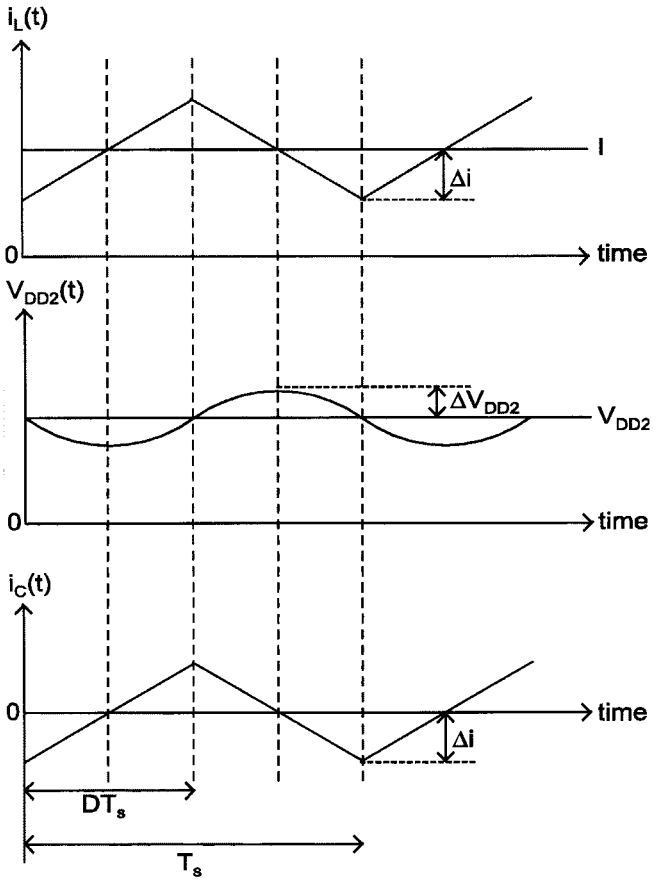

Fig. 2. Inductor current $i_L(t)$, output voltage $V_{DD2}(t)$, and capacitor current $i_C(t)$ waveforms.

III. Circuit Model of a Buck Converter

A circuit model has been developed to analyze the frequency dependence of the efficiency characteristics of a buck converter. The proposed circuit model for the parasitic impedances of a buck converter is shown in Fig. 3.

The power consumption of a buck converter is a combination of the conduction losses caused by the parasitic resistive impedances and the switching losses due to the parasitic capacitive impedances of the circuit components. The power consumption of the pulse width modulation feedback circuit is typically small as compared to the power consumption of the power train (the power MOSFETs, MOSFET gate drivers, filter inductor, and filter capacitor) [2], [3], [5]. Only the power dissipation of the power train components is, therefore, considered in the efficiency analysis.

MOSFET related power losses are analyzed in Section III-A. An analysis of the filter inductor related losses is presented in Section III-B. The filter capacitor related losses are discussed in Section III-C. An analytical expression for the total buck converter power dissipation is presented in Section III-D.

A. MOSFET Related Power Losses

The total power loss of a MOSFET is a combination of conduction losses and dynamic switching losses. The conduction power is dissipated in the series resistance of the transistors operating in the active region. The dynamic power is dissipated each switching cycle while charging/discharging the gate oxide, gate-to-source/drain overlap, and drain-to-body junction capacitances of the MOSFETs. In the following analysis it is assumed that the PWM control signals applied to P_1 and N_1 are nonoverlapping. There is, therefore, no short-circuit current path through P_1 and N_1 during the PWM signal transition. The short-circuit power dissipated in the gate drivers is also neglected assuming the transition times of the input signal applied at each power MOSFET gate driver is smaller than the output transition times [3], [8], [11].

The average power consumption of a power MOSFET and the related gate drivers is

$$P_{\rm MOS} = \frac{R_0}{W} i_{\rm rms}^2 + {\rm EWf_s} \tag{5}$$

$$E \cong \frac{\alpha}{\alpha - 1}(C_{\rm ox} + C_{\rm gs} + 2C_{\rm gd} + C_{\rm db})V_{DD1}^2 \tag{6}$$

where $P_{\rm MOS}$ is the total power consumed during a switching cycle of a power MOSFET (which includes the power dissipated by the MOSFET gate drivers), R_0 is the equivalent series resistance of a 1-μm-wide transistor, $i_{\rm rms}$ is the rms current passing through the power MOSFET, W is the width of the power MOSFET, α is the tapering factor of the power MOSFET gate drivers, $C_{\rm ox}$, $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm db}$ are the gate oxide, gate-to-source overlap, gate-to-drain overlap, and drain-to-body junction capacitances, respectively, of a 1-μm-wide MOSFET, and E is the unit energy (per 1-μm-wide power MOSFET) consumed during a full switching cycle of a power MOSFET (includes the energy dissipated in the gate drivers).

As given by (5), increasing the MOSFET transistor width reduces the conduction losses while increasing the switching losses. An optimum MOSFET width, therefore, exists that minimizes the total MOSFET related power. The optimum MOSFET width and power loss expressions for a target rms current and switching frequency are

$$W_{\rm opt} = \sqrt{\frac{R_0 i_{\rm rms}^2}{f_s E}} \tag{7}$$

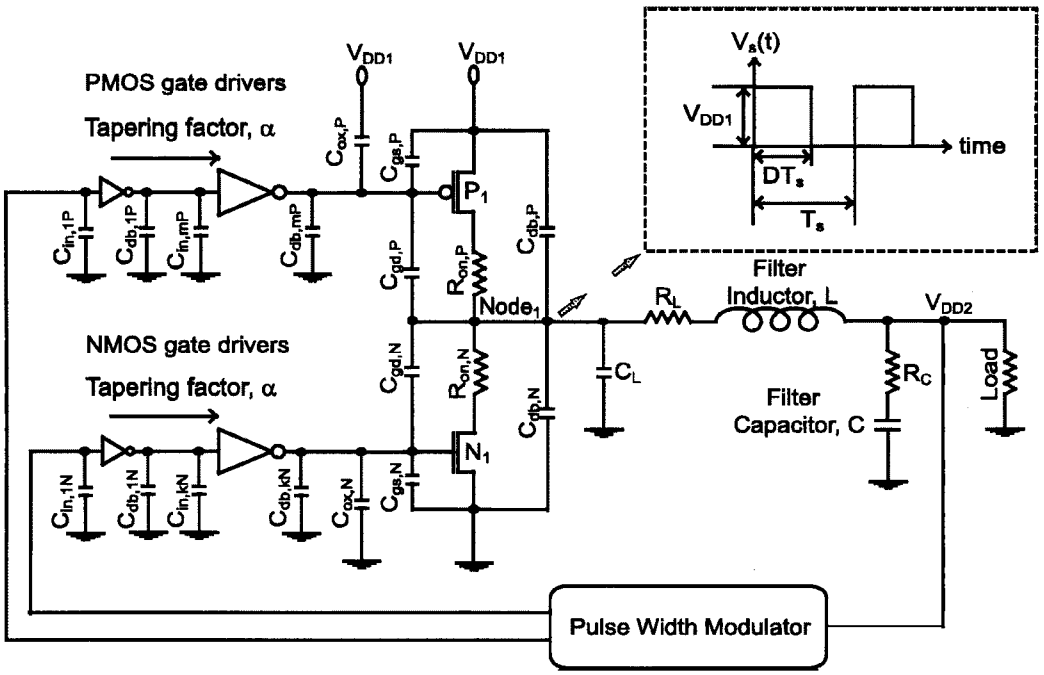

Fig. 3. Circuit model of the parasitic impedances of a buck converter.

$$P_{\mathrm{MOS}}(\min) = 2\sqrt{R_0 i_{\mathrm{rms}}^2 f_s E}. \tag{8}$$

As previously mentioned, it is assumed that the PWM signals for the power MOSFETs are nonoverlapping. The time period during which both N_1 and P_1 are cutoff is called the dead time. The rms currents through N_1 and P_1 (assuming a small dead time to switching period (T_s) ratio as compared to D) are

$$i_{\mathrm{rms}}(\mathrm{NMOS}) = \sqrt{(1-D)\left(I^2 + \frac{\Delta i^2}{3}\right)} \tag{9}$$

$$i_{\mathrm{rms}}(\mathrm{PMOS}) = \sqrt{D\left(I^2 + \frac{\Delta i^2}{3}\right)} \tag{10}$$

where I is the dc current supplied to the load.

Applying (8) for N_1 and P_1 and substituting the rms current expressions (9) and (10), an expression for the total MOSFET related optimized power consumption of a buck converter $P_{\mathrm{tot,MOS}}(\mathrm{opt})$ is

$$P_{\mathrm{tot,MOS}}(\mathrm{opt}) = a\sqrt{\left(I^2 + \frac{\Delta i^2}{3}\right) f_s} \tag{11}$$

$$a = 2\left[\sqrt{R_{0\mathrm{NMOS}}(1-D)E_{\mathrm{NMOS}}} + \sqrt{R_{0\mathrm{PMOS}} D E_{\mathrm{PMOS}}}\right]. \tag{12}$$

B. Filter Inductor Related Power Losses

Some portion of the total energy consumption of a buck converter is due to the series resistance and the stray capacitance of the filter inductor. Integrated spiral inductors have a high series resistance and other intrinsic problems associated with a planar design, which makes these inductors area inefficient [7]. Integration of a spiral inductor with sufficient inductance is, therefore, not feasible for a high-performance microprocessor. A novel low-resistance inductor has recently been reported [7]. Assuming the inductor parasitic impedances scale linearly with the inductance [10], the total power dissipated in the filter inductor is

$$P_{\mathrm{tot,inductor}} = b\left[\frac{I^2}{\Delta i f_s} + \frac{\Delta i}{3 f_s} + \frac{C_{L0} V_{DD1}^2}{R_{L0}\Delta i}\right] \tag{13}$$

$$b = \frac{(V_{DD1} - V_{DD2}) D R_{L0}}{2} \tag{14}$$

where C_{L0} and R_{L0} are, respectively, the parasitic stray capacitance and parasitic series resistance per nanohenry inductance.

C. Filter Capacitor Related Power Losses

The filter capacitance affects the total power consumption of a buck converter due to the effective series resistance (esr) R_C. Assuming the integrated capacitor is implemented utilizing the gate oxide capacitance of a MOSFET, the total power dissipation of a filter capacitor is

$$P_{\mathrm{tot,capacitor}} = d f_s \Delta i, \tag{15}$$

$$d = \frac{8 R_{0\mathrm{cap}} L_{\mathrm{cap}} C_0 \Delta V_{DD2}}{3} \tag{16}$$

where $R_{0\mathrm{cap}}$ is the effective series resistance of a 1-μm-wide MOSFET, C_0 is the gate oxide capacitance per $\mu\mathrm{m}^2$, and L_{cap} is the channel length of the MOSFET.

D. Total Power Consumption of a Buck Converter

Combining (11), (13), and (15), the total power consumption of a buck converter is

$$P_{\mathrm{buck}} = a\sqrt{\left(I^2 + \frac{\Delta i^2}{3}\right) f_s} + b\left[\frac{I^2}{\Delta i f_s} + \frac{\Delta i}{3 f_s} + \frac{C_{L0} V_{DD1}^2}{R_{L0}\Delta i}\right] + d f_s \Delta i \tag{17}$$

where a, b, and d are given by (12), (14), and (16), respectively.

The power dissipation of a buck converter is a strong function of the switching frequency and the inductor current ripple. As given by (17), a higher switching frequency increases the MOSFET and filter capacitor related losses while decreasing the filter inductor related losses. Similarly, the MOSFET and filter capacitor power losses increase with greater inductor current ripple. The relationship between the inductor losses and the inductor current ripple however is more complicated. Increased current ripple reduces the filter inductance required for a target switching frequency, which reduces the inductor parasitic impedances

and the related power loss. A higher current ripple, however, also increases the rms current through the filter inductor which causes the conduction losses of the inductor to be larger.

Depending upon the ratio of the inductor and MOSFET related components of the total power dissipation of a buck converter, the efficiency can actually increase with higher switching frequency and current ripple within a specified (f_s, Δi) range. This observation agrees with the analysis presented in Section IV.

IV. Efficiency Analysis of a Buck Converter

The efficiency of a buck converter is

$$\eta = 100 \times \frac{P_{\text{load}}}{P_{\text{load}} + P_{\text{buck}}} \tag{18}$$

where P_{load} is the average power delivered to the load and P_{buck} is the average total internal power consumption of a buck converter as given by (17).

The dc–dc converter efficiency is strongly dependent on the switching frequency f_s. The switching frequency is, therefore, a primary design variable in this analysis. High f_s is desirable for a monolithic buck converter due to the dependence of the filter inductance and capacitance on f_s as described by (3) and (4). As f_s is increased, values of L and C required to satisfy the target output voltage and current are reduced. Since the integration of the active and passive devices of a buck converter circuit is a primary concern in this analysis, a frequency range higher than the typical ranges found in conventional buck converters is used throughout the analysis. The range of switching frequency f_s is varied from 10 MHz–4 GHz.

As given by (17), another buck converter circuit parameter that strongly affects the circuit efficiency is the inductor current ripple Δi. For a target f_s, increasing Δi reduces the required filter inductance [see (3)]. The filter capacitance, however, must be increased to maintain the output voltage ripple ΔV_{DD2} within acceptable limits with increased Δi for a target f_s [see (4)]. An appropriate Δi, therefore, should be chosen that results in a filter inductance and capacitance suitable for on-chip integration.

In the following analysis, it is assumed that the two power supply voltage levels used in the microprocessor are 1.2 volts (V_{DD1}) and 0.9 volts (V_{DD2}). The average load current demand I is assumed to be 9.5 A. It is also assumed that the tapering factor α of the power MOSFET drivers is two for a worst case energy efficiency analysis. It should be noted that an optimal tapering factor of the power MOSFET gate drivers for energy efficiency is typically much greater than the tapering factor assumed in this analysis [11]. An 80-nm CMOS technology is assumed. The global maximum efficiency circuit configuration is discussed in Section IV-A. The effect of a reduced filter capacitance on the circuit configuration and the resulting efficiency characteristics of a buck converter are analyzed in Section IV-B. The allowable output voltage ripple ΔV_{DD2} is assumed to be 5 mV in Section IV-A and B. Another advantage of an integrated dc–dc converter is that a higher ΔV_{DD2} is acceptable as compared to a nonintegrated dc–dc converter, while satisfying the same load voltage and current specifications. The beneficial effects of increasing ΔV_{DD2} on the efficiency characteristics of a buck converter are examined in Section IV-C.

A. Circuit Analysis for Global Maximum Efficiency

The power dissipation and efficiency variation of a buck converter are shown in Fig. 4 for 0.1 amperes $\leq \Delta i \leq 9.5$ amperes and 10 MHz $\leq f_s \leq 4$ GHz. The "z" axis represents the power (in watts) and the efficiency (%) in Fig.4 (a) and (b), respectively. The MOSFET, filter inductor, and filter capacitor components of the total power dissipation of a buck converter are shown in Fig. 5. The "z" axis in Fig. 5 represents the power (in watts).

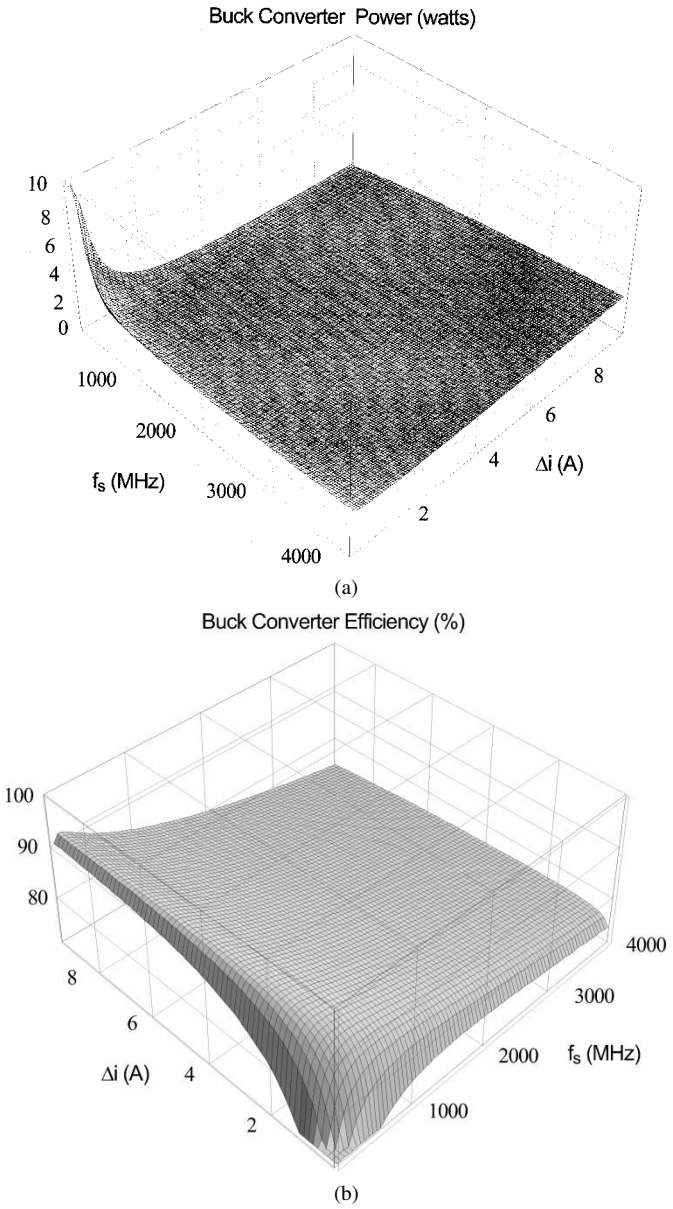

Fig. 4. Total power consumption and efficiency of a buck converter as a function of f_s and Δi. (a) Total power (watts). (b) Efficiency (%).

As shown in Fig. 5, the MOSFET and capacitor related power increases while the inductor power monotonically decreases with increasing switching frequency and inductor current ripple. The capacitor power, however, is negligibly small (less than 1%) as compared to the inductor and MOSFET power over the entire (f_s, Δi) range of analysis. The filter capacitor losses, although included in the analysis are, therefore, not further discussed in the paper. The efficiency of a buck converter is characterized by competing inductor and MOSFET losses. At low f_s and Δi, the buck converter power is primarily dissipated in the filter inductor. As the switching frequency and current ripple are increased, the inductance is dramatically reduced, lowering the parasitic losses of the inductor. The MOSFET power increases, however, with increasing f_s and Δi. At a certain range of f_s and Δi the inductor losses dominate the total losses. As shown in Fig.4 (a), the total power dissipation of a buck converter decreases with increasing f_s and Δi in the range dominated by the inductor losses.

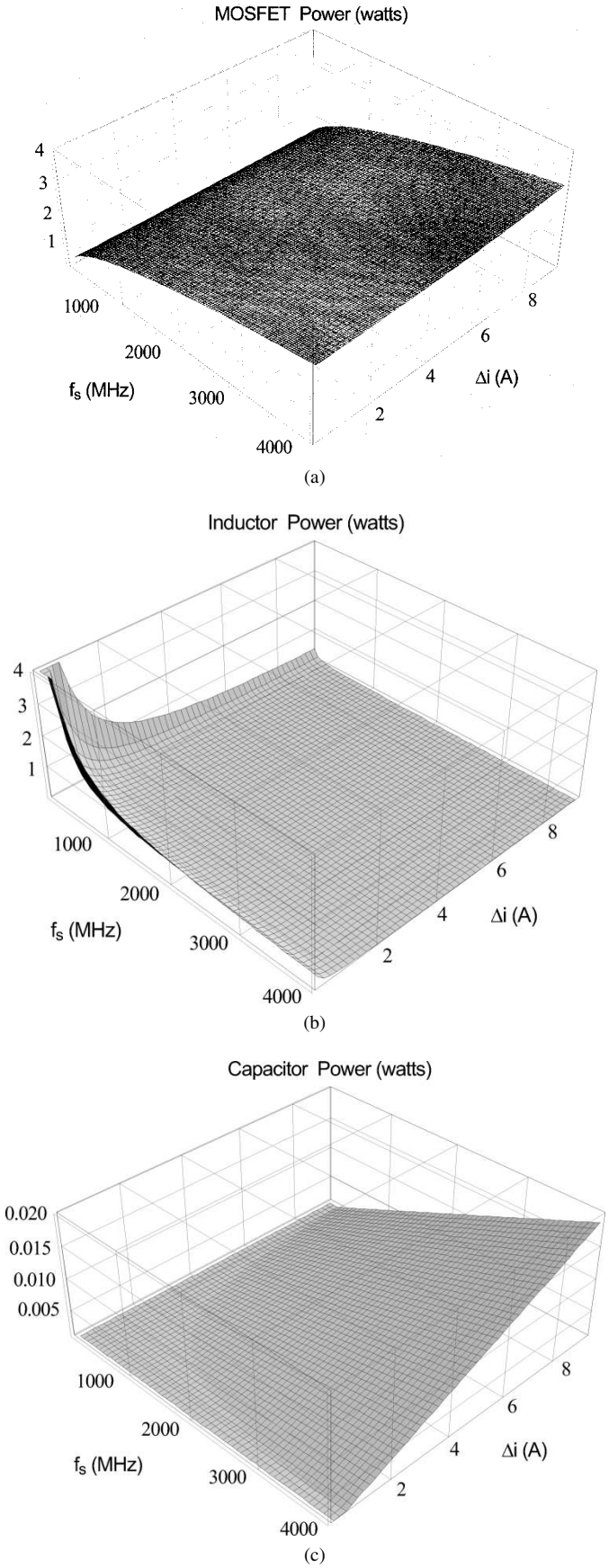

Fig. 5. Distribution of the total power dissipation of a buck converter among different circuit components. (a) MOSFET related power. (b) Filter inductor related power. (c) Filter capacitor related power.

TABLE I
MAXIMUM EFFICIENCY CIRCUIT CONFIGURATIONS OF A BUCK CONVERTER WITH DIFFERENT FILTER CAPACITANCES

C (nF)	η (%)	f_s (MHz)	L (pH)	W_{P1} (mm)	W_{N1} (mm)
1	74.7	3174	279	50.8	20.2
10	82.8	1227	187	81.7	32.5
100	88.4	477	124	131.9	52.5

After the peak efficiency is reached, increasing MOSFET losses begin to dominate the total power dissipation of a buck converter. Hence, the efficiency degrades with further increases in f_s and Δi.

An optimum switching frequency and inductor current ripple pair exists that maximizes the efficiency of a buck converter. The global maximum efficiency is 92% at a switching frequency of 114 MHz and a current ripple of 9.5 A. The required filter capacitor and inductance at this operating point are 2083 nF and 104 pH, respectively. This filter capacitor would occupy an unacceptably large area on a microprocessor die for the target technology. Fabrication of a monolithic dc–dc converter at this maximum efficiency operating point is, therefore, not feasible.

B. Circuit Analysis With Limited Filter Capacitance

Because of the area overhead of an integrated capacitor, the filter capacitance that can be integrated on a microprocessor die is limited. The filter capacitance is swept between 100 and 1 nF to evaluate the effects of a reduced filter capacitance on the circuit configuration and the efficiency characteristics of a buck converter. The circuit configurations at each operating point offering the highest efficiency (η) are listed in Table I.

As listed in Table I, an efficiency of 88.4% can be achieved with a 100 nF filter capacitance. The area occupied by the maximum efficiency configuration with a 100 nF filter capacitance is 12.6 mm^2. The maximum achievable efficiency is reduced to 74.7% as the filter capacitance is lowered to 1 nF. The reason for the increase in power dissipation with reduced filter capacitance is explained by the relationship between the filter inductor, filter capacitor, output voltage ripple, and the inductor current ripple, as described by (3) and (4). As the filter capacitance is reduced, the filter inductance and switching frequency are both increased to satisfy the output voltage and current requirements. Therefore, both the switching and conduction power dissipation of the power MOSFETs and the filter inductor increase with reduced filter capacitance, thereby, degrading the converter efficiency. Note that the conduction and switching components of the MOSFET power dissipation are equal at the optimum transistor width. Both power components increase due to increasing f_s and MOSFET series resistance R_{on} as the filter capacitance is reduced.

With this analysis, a design space is presented that supports full integration of a high-efficiency buck converter onto a microprocessor die. With further capacitor space available on the microprocessor die, the attainable efficiency increases toward the global maximum efficiency of 92% as described in Section IV-A. Another advantage of a higher filter capacitance is the lower-switching frequency requirement, thereby improving circuit reliability and making the design of the pulse width modulation circuitry less complicated.

C. Output Voltage Ripple Constraint

In an external (nonintegrated) dc–dc converter, as the current demand of the microprocessor varies during operation with changing circuit activity level, the voltage supplied to the load also varies due to

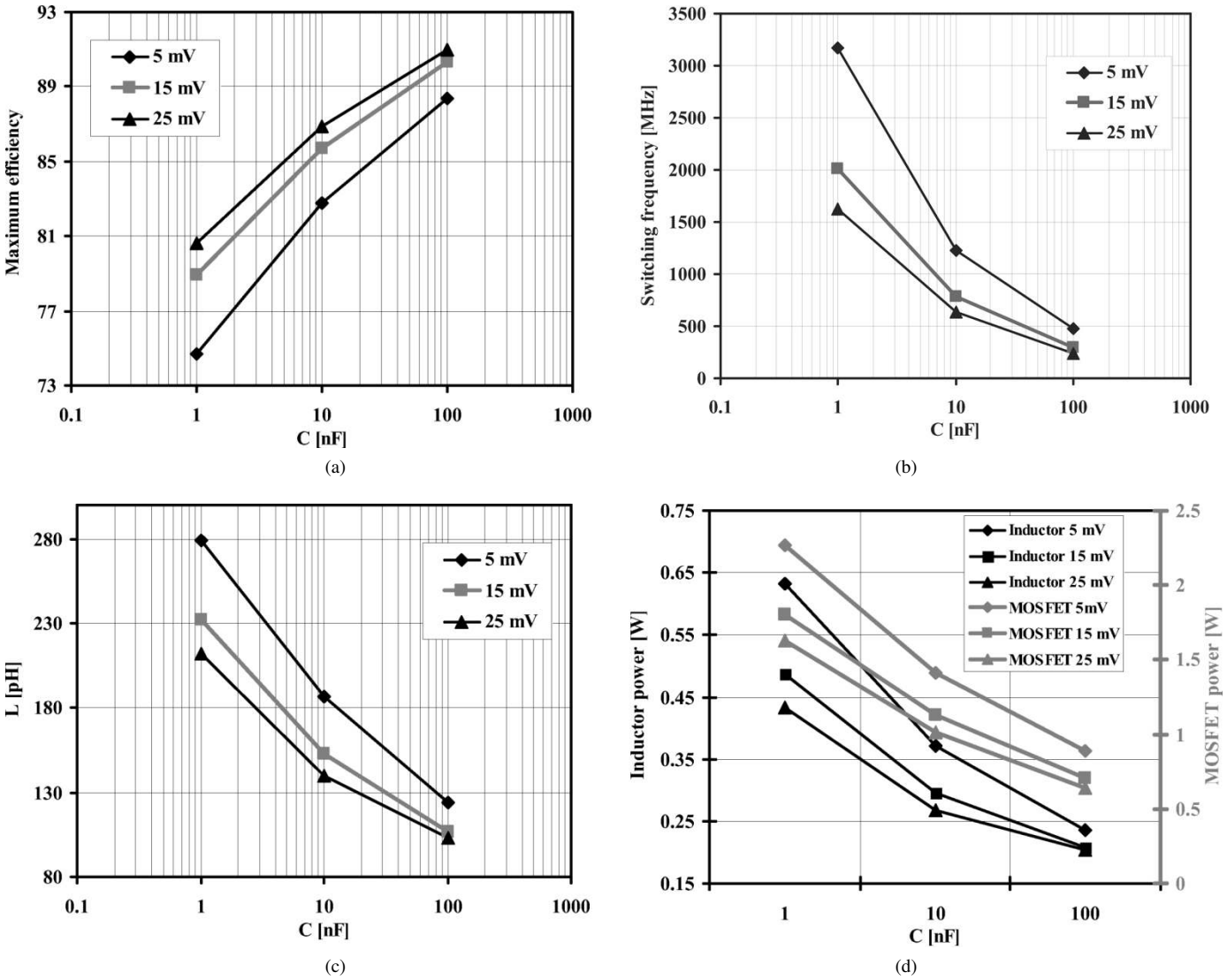

Fig. 6. Variation of circuit parameters and power dissipation of a buck converter with filter capacitance $C(1\text{ nF} < C < 100\text{ nF})$ and output voltage ripple $\Delta V_{DD2}(5\text{ mV} < \Delta V_{DD2} < 25\text{ mV})$. (a) Maximum efficiency. (b) Switching frequency. (c) Filter inductance. (d) Filter inductor and MOSFET components of the total power dissipation of a buck converter.

the resistance of the interconnect between the converter output and the microprocessor input. A droop window of 10% is, typically, allowed as the microprocessor current demand steps from a minimum (caused by standby leakage current) to a maximum. The external wiring (the interconnect between the converter output and the on-chip power distribution network) that exists in an external dc–dc converter does not occur in an on-die dc–dc converter. A larger portion of the acceptable 10% voltage drop window can therefore be applied to the output voltage ripple of an integrated dc–dc converter.

The effect of increasing the output voltage ripple on the circuit configuration and efficiency characteristics of a buck converter is examined in this section. The output voltage ripple ΔV_{DD2} is increased from 5 mV (the value assumed in Section IV-A and B) to 25 mV. The filter capacitance C is also increased from 1 to 100 nF. The maximum efficiency attainable with each ΔV_{DD2} and C pair are shown in Fig. 6 (a). The switching frequency and filter inductance of the buck converter circuit configuration offering the highest efficiency are shown in Fig. 6 (b) and (c), respectively. The filter inductor and MOSFET components of the total power dissipation of a buck converter are illustrated in Fig. 6 (d).

As shown in Fig. 6, increasing the output voltage ripple reduces the switching frequency and filter inductance required to satisfy the dc–dc converter output voltage and current specifications for a fixed filter capacitance. With decreased switching frequency and filter inductance, both the MOSFET and inductor related components of the total power dissipation of a buck converter are reduced, as shown in Fig. 6(d). The efficiency attained by a limited filter capacitance, therefore, increases by relaxing the output voltage ripple constraint. Moreover, as the required filter inductance is reduced, the die area required for the integrated filter inductor becomes smaller. Similarly, as the required switching frequency is reduced, the circuit reliability increases while the design of the pulse width modulation circuit becomes less complicated. As shown in Fig. 6, the maximum achievable efficiency increases by up to 7.9% as the output voltage ripple is increased from 5 to 25 mV. Similarly, the filter inductance and switching frequency required for a corresponding maximum efficiency configuration are reduced by 24% and 48.7%, respectively, as ΔV_{DD2} is increased from 5 to 25 mV.

V. Simulation Results

The buck converter circuit configuration that produces the maximum efficiency (see Table I) with a filter capacitance of 100 nF and an output

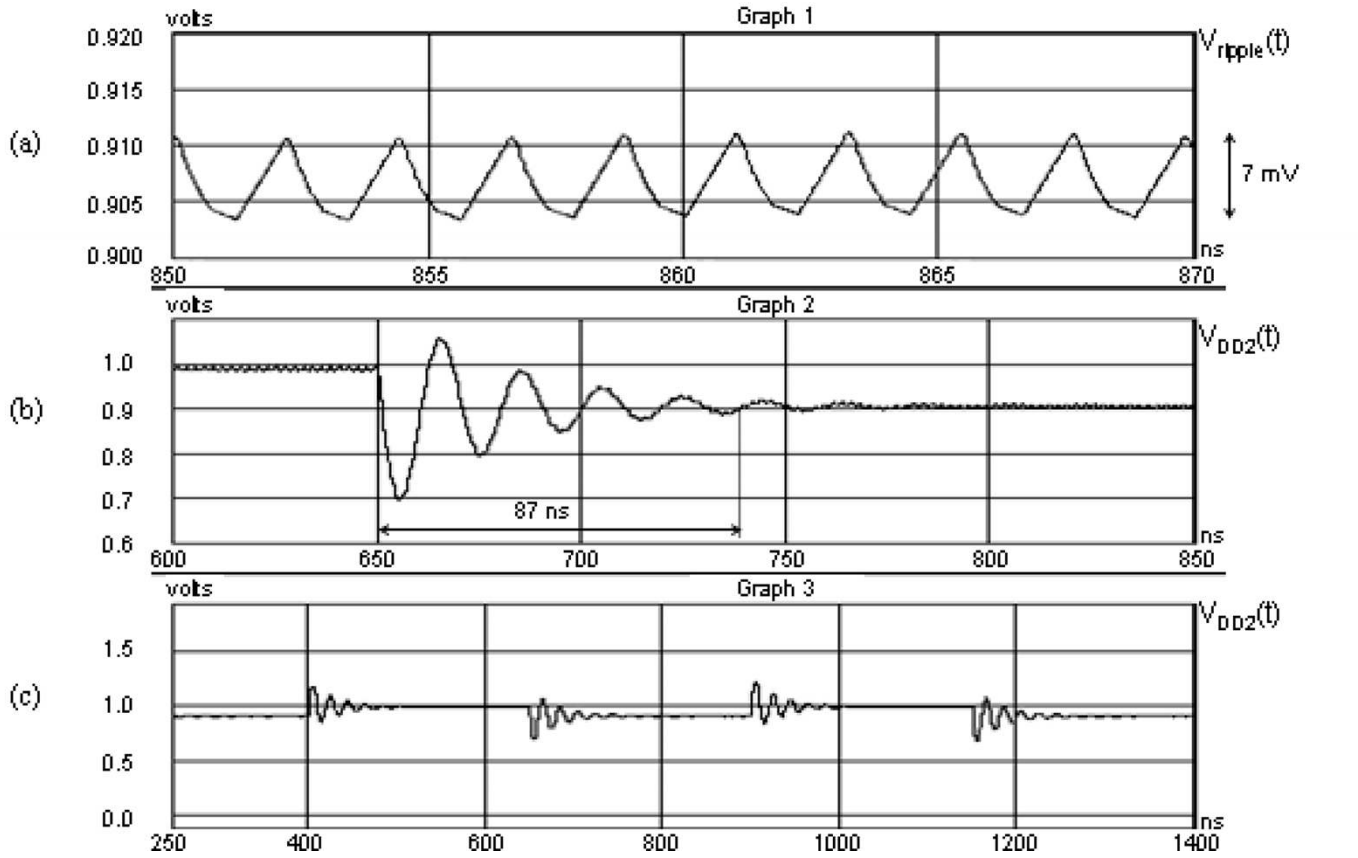

Fig. 7. Simulation waveforms of a buck converter for $C = 100$ nF. (a) Output voltage ripple $V_{\text{ripple}}(t)$. (b) Output response of a buck converter to a change in load current from $I_{\min}$ to I. (c) Output response of a buck converter to a step current changing between $I_{\min}$ and I.

voltage ripple of 5 mV is evaluated assuming an 80-nm CMOS technology. The analytical expression [see (17)] for the total power consumption of a buck converter is effective in estimating the circuit efficiency characteristics. The buck converter efficiency as determined by simulation at the target design point is 86%, which only differs by 2.4% from the efficiency determined from the analytic expression.

The converter output voltage (which supplies 9.5 A of dc current to the load) is shown in Fig. 7(a). The peak-to-peak output voltage ripple is actually lower than the analytic expectation of 10 mV. This behavior is noted since the voltage drop across the equivalent parasitic resistance of the power MOSFETs and the filter inductor has been neglected during the steady-state analysis used in the development of (3) and (4).

The response of the buck converter to changes in the current demand (between the minimum and the maximum) at the load has also been evaluated. A 10% output voltage window is allowed as the average current demand of the microprocessor swings from a minimum $(I_{\min})$ to a maximum (I). The minimum current demand $I_{\min}$ is caused by leakage current when the microprocessor is idle and is assumed to be 25% of the maximum current demand I [1]. The waveforms illustrating the dc–dc converter output response for a current step from $I_{\min}$ to I are shown in Fig. 7 (b) and (c). As shown in Fig.7 (b), the response time for the buck converter to settle within the allowed 10% voltage window after the microprocessor transitions to the maximum current mode from the idle mode is 87 ns. One solution that provides a stable voltage to the microprocessor until the buck converter output settles within the 10% window is to use several high-speed linear regulators distributed around the microprocessor die. These regulators are activated whenever the buck converter output voltage drops below the lower limit of the 10% window. The linear regulator circuits are intrinsically low-efficiency voltage converters [2], [3]. These large current steps, however, do not occur frequently and the linear regulators are only active for a brief amount of time (a worst case time of 87 ns) until the buck converter output settles within the 10% voltage droop window. The overall impact of these linear regulators on the energy dissipation of the microprocessor is, therefore, small.

VI. Conclusions

An analysis of the power characteristics of a standard switching dc–dc converter topology, a buck converter, is provided in this paper. A parasitic model of a buck converter is presented. With this model, a closed form expression for the total power dissipation of a buck converter is proposed. An analysis over a range of design parameters is evaluated, permitting the development of a design space for full integration of active and passive devices on the same die for a target CMOS technology.

Two major challenges for a monolithic switching dc–dc converter are the area occupied by the integrated filter capacitor and the effect of the parasitic impedance characteristics of the integrated inductor on the overall efficiency characteristics of a switching dc–dc converter. A high switching frequency is the key design parameter that enables the integration of a high efficiency buck converter on the same die as a dual-V_{DD} microprocessor.

It is shown that an optimum switching frequency and inductor current ripple pair that maximizes the efficiency of a buck converter exists for the target technology. The global maximum efficiency is 92% at a

switching frequency of 114 MHz and a current ripple of 9.5 A assuming an 80-nm CMOS technology. The required filter capacitance and inductance at this operating point are 2083 nF and 104 pH, respectively.

The effects of reducing the filter capacitance due to the tight area constraints on a microprocessor die have been examined. An efficiency of 88.4% is shown at a switching frequency of 477 MHz with a filter capacitance of 100 nF. The area occupied by the buck converter is 12.6 mm^2 and is dominated by the area of the integrated filter capacitance. The analytic model for the converter efficiency is within 2.4% of the simulation results at the target design point.

The output voltage ripple can be increased in a fully integrated dc–dc converter, offering the same 10% output voltage droop window as compared to a nonintegrated dc–dc converter. It is shown that the maximum attainable efficiency increases by up to 7.9% as the output voltage ripple is increased from 5 to 25 mV. Similarly, the filter inductance and switching frequency required for maximizing the efficiency of a buck converter are reduced by 24% and 48.7%, respectively, with increasing ΔV_{DD2}.

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