AN ANALYSIS OF CERTAIN ASPECTS OF FORCED COMMUTATED HVDC INVERTERS

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by

Aniruddha Gole

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ANIRUDDHA MADHUKAR GOLE

A thesis submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements of the degree of

MASTER OF SCIENCE

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ABSTRACT

Inverters used for HVDC application today are 'naturally' or 'line' commutated, which means that the line-line voltage on the ac side is used to force the current in the off-going valve to zero, thereby turning it off. In the 'forced' or 'artificially' commutated inverter, the valve current is forced to zero artificially, *i.e.*, without the use of the line-line voltage for this purpose.

By using forced commutation in HVDC inverters, it may be possible to reduce the inverter's reactive power requirement, and indeed, sometimes it is even possible to make the inverter supply reactive power.

Previous researchers have concluded that the series capacitor commutation scheme (out of the many schemes available for forced commutation) seems most promising, and have carried out certain investigations into the operation of such a series capacitor commutated inverter.

This investigation is an extension of previous work done, and covers factors such as harmonics, ac-side faults, the rate of change of firing angle and the possibility of inverting into weak ac systems.

The results indicate that the firing angle can be changed fast, that the system is immune to ac-side faults, and that it can operate satisfactorily into weak ac systems.

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a, b, c	phase sequence
c_a, c_b, c_c	capacitors in phases a, b, c
e_a, e_b, e_c	phase voltages
e_1, e_2	phase voltages involved in commutation from a typical phase 1 to phase 2.
i_a, i_b, i_c	phase currents
I_d	dc current
k	minimum number of steps needed to effect a firing angle change
ℓ	transformer inductance
P	real power
Q	reactive power
r	resistance of weak system
SCR	Short Circuit Ratio
S_0, S_1, etc.	switches
t	time
T_1, T_2, T_3 etc.	thyristors
v_a, v_b, v_c	phase voltages (same as e_a, e_b, e_c)
v_{c_1}, v_{c_2}	capacitor voltages involved in commutation from phase 1 to phase 2
V_d	dc voltage
X_c	capacitor reactance
X_ℓ	transformer/and or system reactance
α	firing angle
α_o, α_f	initial and final values of firing angle
μ	overlap angle
ω	angular frequency of supply voltage
δ	symmetrical angular change for α

CHAPTER 1

INTRODUCTION

1.1 Forced vs Natural Commutation

The thyristor valve is a device which requires the current to be brought to zero and a reverse bias across it in order to turn off when it is conducting. In the HVDC inverter this is usually provided by the line voltage itself, the process being known as 'natural' or 'line commutation'. Alternatively, this reverse biasing voltage could be derived from some other source (usually some capacitors precharged to proper voltages), the resulting commutation being called 'forced' or 'artificial' commutation.

Figure 1.1.1 shows the basic three-phase Graetz bridge used in HVDC rectification/inversion, and Fig. 1.1.2 shows the resulting waveform. The dc line is assumed to carry constant current (a justifiable assumption because of the high value of inductance in the dc circuit). The thyristors are pulsed according to their sequence, *i.e.*, 1, 2, ..., 6, each after a $60°$ interval. The firing angle α is measured from the phase voltage crossover. From Fig. 1.1.2 it can be seen that the current fundamental lags the ac voltage by an angle equal to $180° - \alpha$. The angle α cannot be increased to (or beyond) $180°$, because proper thyristor turn off requires that a reverse voltage exist across the thyristor for at least a minimum duration δ. Thus the maximum angle at which the bridge may be operated is given by $\alpha = 180° - \delta - \mu$ where μ (not shown in the figure) corresponds to the time required for current transfer from one phase to the other. μ is normally of the order $15°$ -

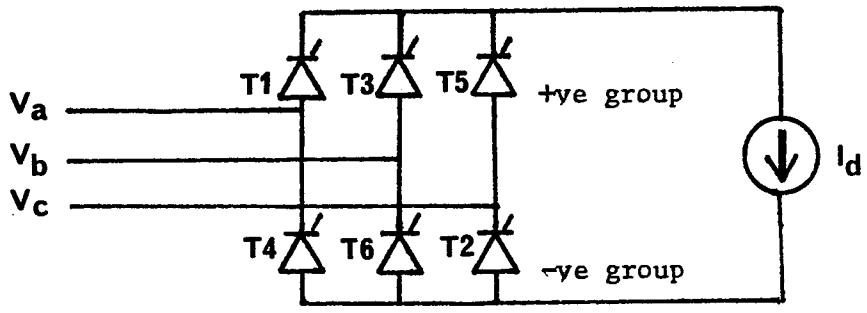


FIG 1.1.1 : THREE PHASE GRAETZ BRIDGE

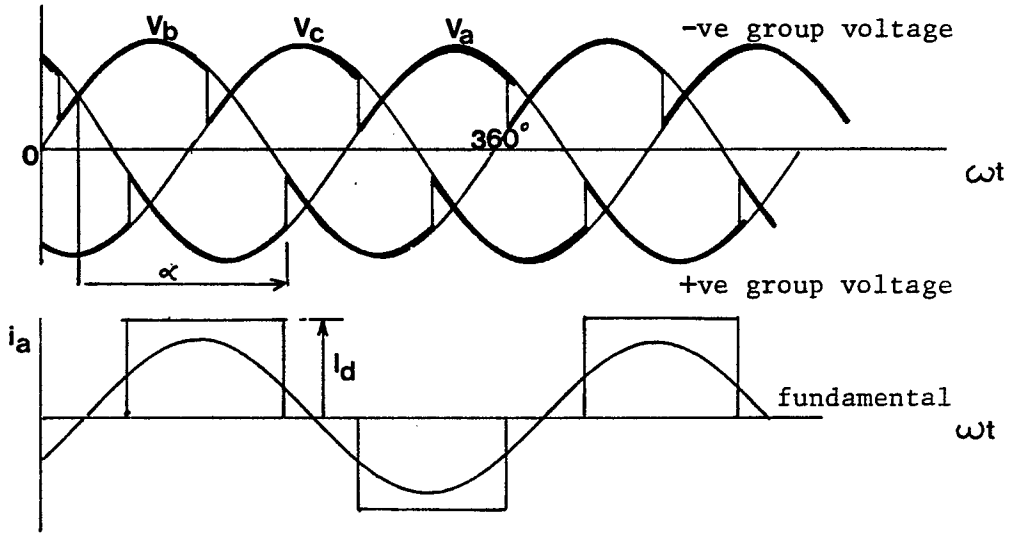
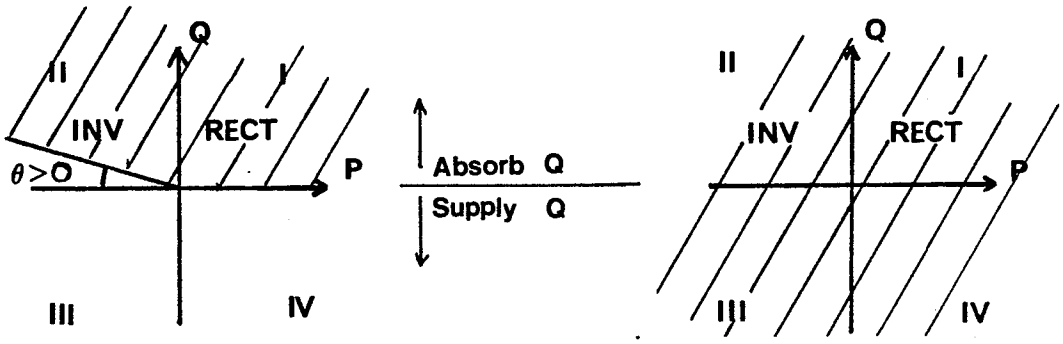


FIG 1.1.2 : VOLTAGE AND AC CURRENT WAVEFORMS.
(COMMUTATION REACTANCE IGNORED.)



a)NATURAL COMMUTATION b)FORCED COMMUTATION

FIG 1.1.3 : RANGES OF OPERATION

25° and arises due to the presence of finite inductance in the transformer windings. Hence α can be increased only to 150° - 155°, and this implies that the inverter must consume reactive power. A large requirement of reactive power means a drop in the system voltage, unless that reactive power is somehow supplied. In the case of the naturally commutated inverter, this reactive power may be as high as 60% of the real power. This is clear from the 4 quadrant diagram of Fig. 1.1.3(a) which shows the possible P (real power) and Q (reactive power) ranges for the naturally commutated inverter. In the inverter operation $Q = 0$ is not possible due to the extinction angle required.

In forced commutation, artificial means are used to keep the off-going thyristor reverse biased even when the line-line voltage has reversed. Thus, the firing angle may be greater than that possible under natural commutation, thereby resulting in a smaller reactive power requirement for the converter.

In fact, as shown in Fig. 1.1.3(b) reactive power (Q) supply is also possible and ideally it may be possible to operate in all four quadrants. Usually the load connected at the inverter station consumes Q. Thus, a Q supply from the inverter can be used to meet this demand, and hence allow for voltage control at the inverter bus.

Note that the 4 quadrant diagrams are drawn for inverter as well as rectifier operation because there is no reason why an inverter may not be operated as a rectifier, *i.e.*, with $\alpha < 90°$.

1.2 Why Forced Commutation?

The need for reactive power supply from the ac side is a serious drawback in the naturally commutated inverter, and this drawback is not present in the forced commutated one.

Thus with a forced commutated inverter, it is no longer necessary to invert into a strong ac system, and this may considerably increase the number of situations in which dc may be a favourable alternative over ac transmission. For example, the proposed Hong Kong-Macao link could have a force commutated converter at Macao. As the island of Macao has no generation potential and as ac links from mainland Hong Kong are impossible due to the presence of a body of water in between, HVDC transmission with static compensation at the receiving end has been proposed. But this receiving inverter may as well be a forced commutated one, thereby removing the need for any kind of reactive power compensation.

The forced commutated inverter has the feasibility of being used as a self-contained tap on an HVDC line, as it can invert into a load that has no voltage support on its ac side at all. Because it is completely solid-state it appears to be a favourable alternative to other proposed methods, such as the one by Bowles et al [1] which makes use of a dc motor - ac generator set running off the dc line to provide reactive power support. In fact recently, Sood et al [2] have done preliminary simulator tests to demonstrate inversion into lagging pf loads.

A forced commutated tap on a long HVDC line might have been a possible answer to the recently scrapped proposal of running an HVDC line between the Canadian province of Manitoba and the U.S. state of Nebraska. The proposal was cancelled due to the fact that the states of North and South Dakota could not get any power out of the line passing through them because of the inability of having a tap on the line.

Other advantages result which are a consequence of the type of forced commutation scheme used, and will be discussed in later chapters.

1.3 Requirements of a Forced Commutation Scheme

Some work has been carried out in the area of forced commutation [3,5]. The requirements that a forced commutated inverter must satisfy are thus summarized.

1. High reliability
2. Minimal stress on converter components
3. Fast change of firing angle (α) should be possible. The commutation circuit should not slow down the speed with which α can be changed. Fast control on α is required for good transient and fault performance.
4. Easy system recovery in case of fault

   The converter must resume normal operation after a fault is cleared. It should also be possible to connect/disconnect the converter to/from the system in minimum time.
5. Wide range of operation

   The converter should be able to operate over a wide range of power and current settings without commutation failure.

It may not be possible to meet all the above requirements equally well, but the system must conform to them as well as possible, without being unduly expensive.

1.4 Selection of Forced Commutation Scheme

A large number of schemes already exist [4] in the low power area, *i.e.*, in drives for ac machines. Most of these are quite complicated and are usually for voltage control, and have to operate over a large range of frequency. HVDC inverters do not have to satisfy this requirement, but they have to be extremely reliable over their operating current/power range. Thus, the requirements for high power and low power

inverters are somewhat different. Some schemes proposed for HVDC applications are reviewed briefly below; and it appears that the series commutated inverter is the best.

1.4.1 Forced Commutation in Two Steps

This scheme, shown in Fig. 1.4.1, has been recommended for application in HVDC inverters first by Bakharerski & Utevski [6], and also by Buseman [3]. The operation of this circuit may be summarized as follows:

Assuming T_1 and T_2 are conducting and T_3 is required to take over from T_1, T_7 is first fired. The capacitor has previously been charged in the direction shown, and thus T_7 goes into conduction, thereby applying the capacitor voltage across T_1 and the transformer inductance. Assuming the charge on C to be sufficient for turning off T_1, T_1 is turned off, and T_2 and T_7 continue conduction and charge C in the opposite direction. When C is sufficiently charged, T_3 is pulsed to take over from T_7, and hence the current transfer from T_1 to T_3 is accomplished. The same happens for all other transfers.

The obvious drawback of this circuit is the extra number of thyristors (over a naturally commutated bridge), high stresses (both voltage and dV/dt), because the capacitor has to be charged from full positive to full reversed voltage in a short time. A delta connected transformer winding is also a must to eliminate the inevitable 3^{rd} harmonic.

1.4.2 Forced Commutation in 1 Step [3]

This circuit is shown in Fig. 1.4.2. The capacitor is current charged as before, and each valve conducts for 60° at a time. The conduction pairs of thyristors are (4,3'), (4',5), (6,5'), (6',1), (2,1'),

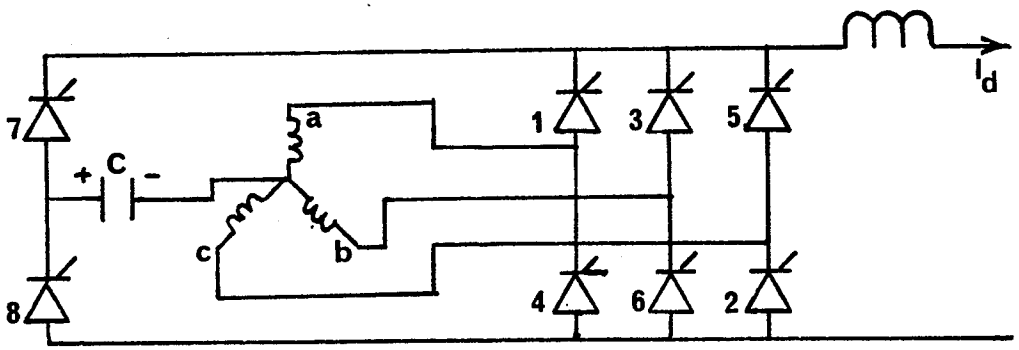


FIG 1.4.1: FORCED COMMUTATION IN 2 STEPS

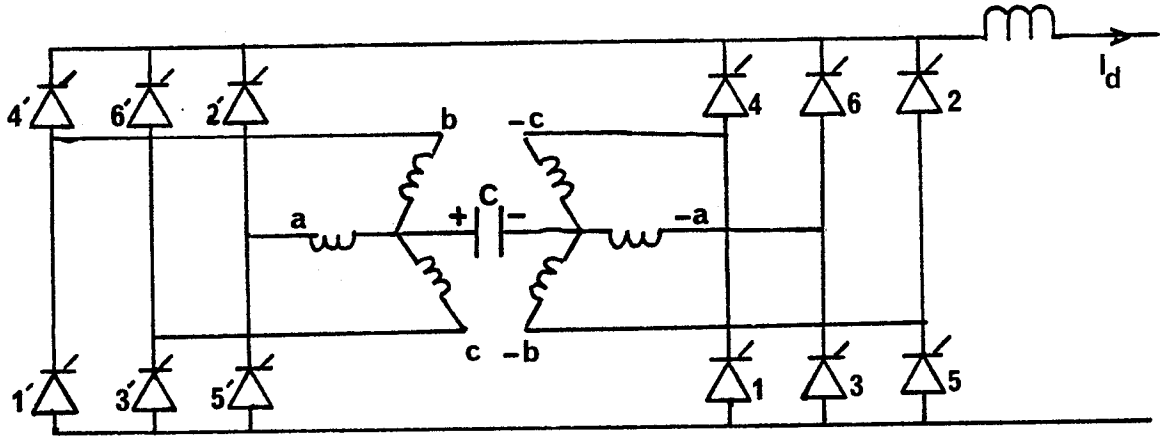


FIG 1.4.2 : FORCED COMMUTATION IN 1 STEP

(2',3) and so on in cyclic order. Consider the case when T_1' and T_2 are conducting and T_2', T_3 are to take over. Capacitor C has already been charged in a direction to forward bias T_2' and T_3. Thus, when T_2' and T_3 are pulsed, they conduct, and the capacitor voltage comes across T_1' and T_2 as a reverse bias. Thus T_1' and T_2 are extinguished.

This circuit, unlike the two stage commutated one, has the capacitor charging over a 60° interval, and thus stresses are reduced. However, the number of thyristors is twice that of a normal 3-phase Graetz bridge, and of comparable voltage and peak current ratings. Thus, the thyristor valves are underutilized.

1.4.3 Resonant Commutation [6,7]

In this method, a harmonic voltage of suitable phase angle is superposed on the fundamental voltage. This causes a delay in the zero crossover of the voltage, and hence it is possible to operate at near-unity power factors. This scheme however, requires larger smoothing reactors, than the corresponding natural commutation scheme. The resonant circuit's cost is comparable with the cost of capacitors required for static VAR supply for a normal inverter. The peak voltage value is also increased thereby causing valve stresses. Automatic tuning on the filters to compensate for slight supply frequency variations is also necessary.

1.4.4 Artificial Commutation through Voltage Injection

Gilsig and Freris [9] have discussed a scheme in which voltage pulses are injected in series with the source to suitably control the voltage during commutation. This scheme, as pointed out by the authors themselves, is of no practical value. They carried out the analysis only

to gain a better understanding of the commutation process.

1.4.5 The Series Commutated Inverter

This scheme, as pointed out by Buseman [3] is the most promising one, and is discussed in greater detail in the following section.

1.5 The Series Capacitor Commutated Inverter

This inverter is similar to an ordinary 3-phase Graetz Bridge, except for the series capacitors in each phase (as in Fig. 1.5.1). It has been shown [3,5] that this scheme is competitive with a naturally commutated inverter with static capacitors for VAR generation.

Its operation is now described with reference to Fig. 1.5.1. The dc current I_d is assumed constant (a reasonable assumption on account of the high inductance in the dc circuit). The firing sequence is the same as in a normal $3-\phi$ bridge. The firing angle (α) now may be greater than $180°$. Consider the instant when T_3 is to take over from T_1, when T_1 and T_2 are on and thus phases a and c are in conduction. The following events now take place:

1. The capacitors in phases a and c charge with the polarity shown.
2. When T_3 is fired to take over from T_1, the voltages on capacitors C_a, C_b are of the correct polarity for commutation. (Capacitor C_b has been charged to the proper voltage when T_6 was in conduction before T_2 took over.)
3. After the commutation is completed, T_3 and T_2 conduct, with the voltage on C_b decreasing and on C_c increasing with the constant current flowing through them. Thus the capacitors are charged to the voltages necessary for future commutations.

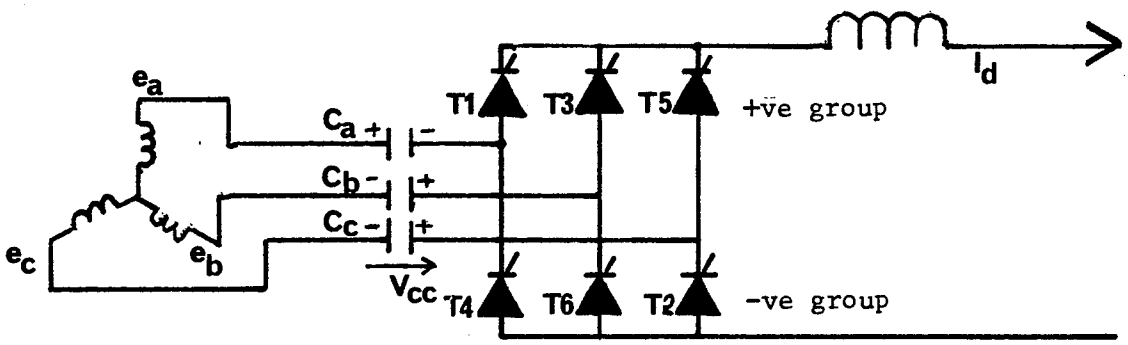
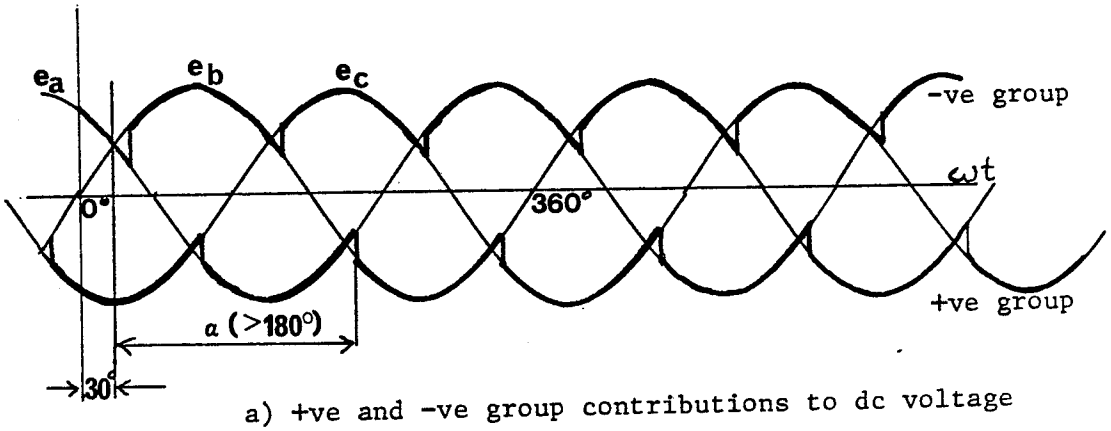
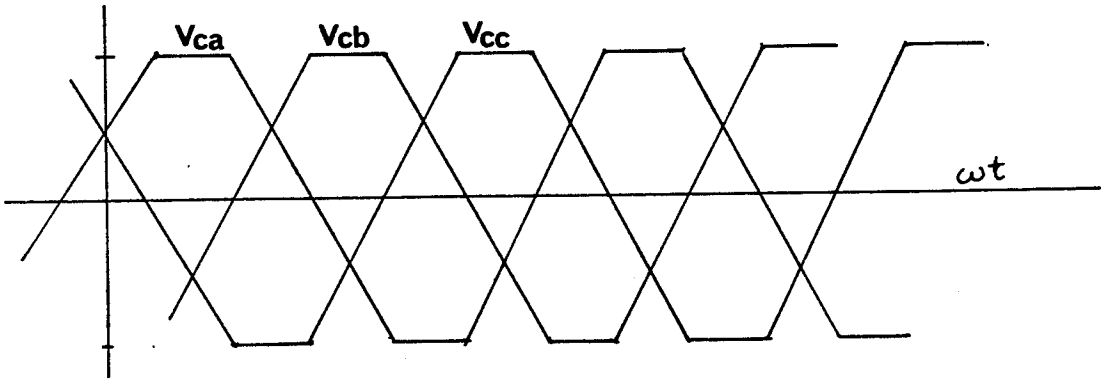


FIG 1.5.1: BASIC SERIES CAPACITOR COMMUTATED BRIDGE



a) +ve and -ve group contributions to dc voltage



b) Capacitor Voltages

FIG 1.5.2 : CONVERTER WAVEFORMS.
(TRANSFORMER REACTANCE NEGLECTED)

It is to be noted that it is the capacitor voltages (and not the line voltages) that essentially provide the commutation voltage, and so firing angles beyond 180° are possible. In this case, the line-to-line voltage subtracts from the sum of the capacitor voltages to give the net commutation voltage. Note that as the capacitors do not add any net dc voltage, the output dc voltage is essentially the same as that of a naturally commutated inverter firing at the same angle α. The resultant waveforms (ideal) are shown in Fig. 1.5.2 (a & b).

1.5.1 Reasons for selection of this circuit

Making certain assumptions about the relative costs, Buseman [3] has shown that this circuit is competetive with a naturally commutated system with static VAR supply, especially when operating at near unity power factors.

A preliminary glance at this method of commutation seems to indicate the following advantages.

i) The capacitor is current charged, and current, not voltage is the more or less constant quantity in dc systems. A voltage based forced commutation scheme (as used in ac machine control) would be prone to commutation failure as the commutation capacitors might not get charged to the proper voltages. Furthermore, a larger dc current requires a larger commutation voltage, and this happens automatically because the voltage on the capacitor is proportional to the current which charges it.

ii) No extra valves are required above the number required in a naturally commutated bridge.

iii) No special controls are required for steady-state operation other than those used in a normal 3-phase bridge.

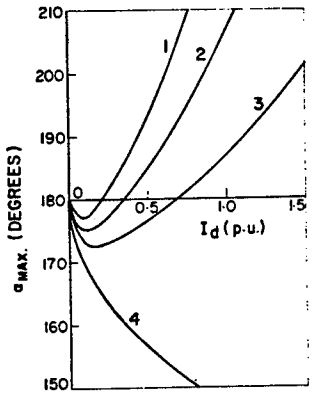
iv) Insulation coordination appears to be easy, due to the proximity of the transformer windings to the capacitors.

v) AC side harmonics, and dc side average voltage are almost the same as those in an ordinary Graetz bridge.

1.5.2 Previous work on this circuit

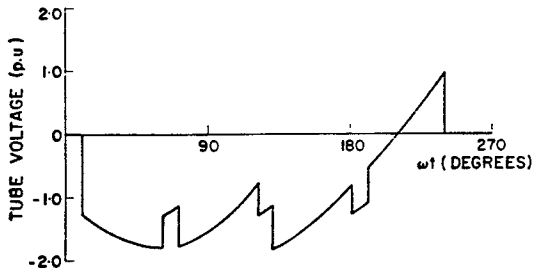
Apart from Buseman [3] mentioned earlier, J. Baron, J. Reeves and G.A. Hanley [5,8] have carried out some detailed investigations of the circuit's operation. They have covered the following aspects:

1. Detailed steady-state analysis of the bridge's operation.
2. Development of a hybrid p.u. system for analysis of a combined ac-dc system. They choose the dc current and ac side voltage as the base quantities. In conversion to actual system quantities, the $\sqrt{6}/\pi$ ac current/dc current approximation is used, *i.e.*, for 1 p.u. dc current, the ac current fundamental has a magnitude $\sqrt{6}/\pi$ p.u.
3. Ranges of operation (Fig. 1.5.3a). As the commutation voltage available is a function of current, and the success/failure of commutation a function of this voltage and the current, the maximum firing angle permissible is a function of the dc current.
4. Valve voltages and their peak values. (Fig. 1.5.3b and c). The ratings of equipment depend on the peak voltage they are supposed to withstand.
5. DC output voltages and powers. (Fig. 1.5.3d, and e).
6. Fault conditions such as commutation failure (Fig. 1.5.3f). The effect of commutation failure is more severe than in the case of a normal 3-phase bridge. In fact, the capacitors may sometimes not regain proper charge for successful commutation, and thus natural recovery may sometimes not be possible.



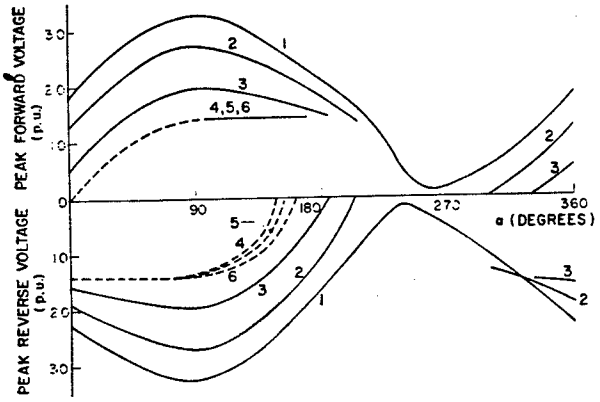
V_L = 1.0 per unit X_L = 0.111 per unit
Curve 1—X_c = 0.9 per unit
Curve 2—X_c = 0.7 per unit
Curve 3—X_c = 0.5 per unit
Curve 4—X_c = 0 per unit, natural

a) α_{max} as a function of I_d.



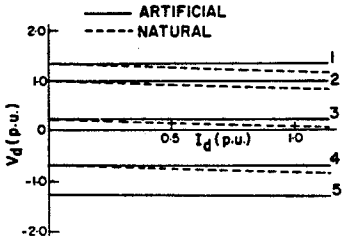
V_L = 1.0 per unit I_d = 1.0 per unit
X_L = 0.111 per unit X_c = 0.5 per unit
ωt = 0 at start of commutation α = 0°

b) Typical tube voltage waveform (computed).



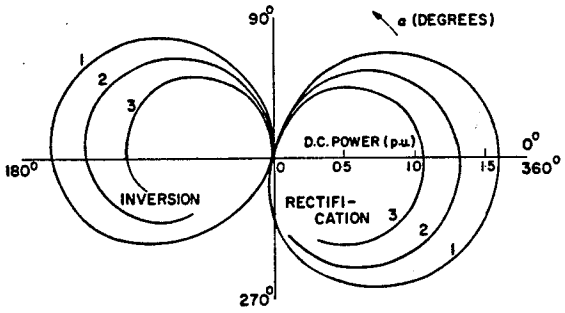
V_L = 1.0 per unit X_L = 0.111 per unit
X_c = 0.9 per unit
I_d = 1.0 per unit: 1—artificial, 4—natural
I_d = 0.7 per unit: 2—artificial, 5—natural
I_d = 0.3 per unit: 3—artificial, 6—natural

c) Peak tube voltages.



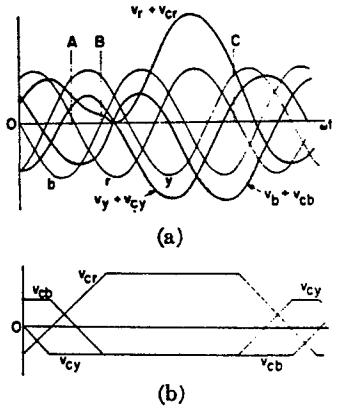
V_L = 1.0 per unit X_c = 0.7 per unit
Curve 1—α = 0°
Curve 2—α = 40°
Curve 3—α = 80°
Curve 4—α = 120°
Curve 5—α = 160°

d) Variation of V_d with I_d.



V_L = 1.0 per unit X_L = 0.111 per unit
X_c = 0.9 per unit
Curve 1—I_d = 1.2 per unit
Curve 2—I_d = 1.0 per unit
Curve 3—I_d = 0.8 per unit

e) Power characteristics.



f) Commutation failure of tube 6. (a) Phase-to-neutral and composite waveforms. (b) Capacitor voltage waveforms.

FIG 1.5.3 : CERTAIN RESULTS DUE TO BARON,REEVES AND HANLEY (5)

7. Analysis of faults such as arcbacks. (The problem of arcback is no longer important with solid-state devices.)
8. A simplified demonstration that inversion into purely resistive loads is possible with this type of inverter.
9. An outline of certain control requirements and possible strategies. They point out that techniques in which extinction angles are directly obtained should be used for determining the exact firing angle, rather than analog predictive techniques (which compute the extinction angle by feeding voltage/current information to an analog circuit). This is because of the uncertainty of the capacitor voltages which may vary during transients. Also pointed out is the possibility of using naturally and artifically commutated bridges in parallel so that a broader range of dc currents may be handled without unduly increasing the valve ratings.

1.6 Outline of the Thesis

As pointed out in the preceding sections, the series capacitor commutated inverter seems to be the best suited for HVDC applications and hence, it was felt that it deserved further study.

This thesis aims to extend the work of Baron et al to a more complete technical assessment. Thus in the course of this investigation, the following have been performed:

1. Development of a more detailed computer model for steady-state as well as transient studies.
2. Effect of ac side faults on converter operation.
3. Analysis of ac and dc side harmonics.
4. Determining the maximum rate of change of firing angle. The requirement of proper commutation voltage on capacitors dictates that

the firing angle may not be suddenly changed, as may be necessary during faults.

5. Operation into weak systems and a study of start-up.

The results indicate that the inverter is practically immune to ac side faults, that the firing angle can be changed quite fast, and that the inverter is particularly suitable for inversion into weak ac systems.

The next chapter discusses the analytical aspects of the problem and derives the necessary program flow charts. Chapter 3 discusses the results obtained for fault studies, and analysis of the rate of change of firing angle and harmonics. Chapter 4 concerns itself with inversion into weak ac systems. Finally, conclusions and recommendations are stated in Chapter 5.

CHAPTER 2

CIRCUIT ANALYSIS AND PROGRAM DEVELOPMENT

2.1 Introduction

This chapter describes how the programs used in the investigation were developed. The basic simulation routine is described first, and later sections show how other studies were incorporated into the simulation program. This chapter basically concerns itself with inversion into strong ac systems. A study of inversion into weak systems is presented in Chapter 4. The problems discussed here are:

1. Effect of ac side faults on operation.
2. Ac and dc side harmonics.
3. Determination of the maximum rate of change of firing angle.

Only the methodology is presented. Results are discussed in the next chapter.

2.2 The Basic Model

The following assumptions have been made:

1. Assumption of constancy of dc current (at least in the short run), because the high inductance in the dc circuit does not allow a high rate of change of current.
2. Neglect of snubber circuits and the possible effects of other overvoltage protection equipment on the converter.

These assumptions have been made because this study is meant to be indicative, and not a highly detailed one.

2.2.1 The basic philosophy

It was felt that a state variable model would lend itself to transient as well as steady-state solution. In this approach the 'state equation'* for the system is written in the form:

$$\dot{\underline{X}} = A\underline{X} + B\underline{u} \tag{1a}$$

$$\underline{Y} = C\underline{X} + D\underline{u} \tag{1b}$$

where $\underline{X}$ is the vector of state variables (minimal set of variables in terms of which all the other system variables may be determined, *e.g.*, inductor currents and capacitor voltages), $\underline{u}$ the vector of input quantities (*i.e.*, source voltages, dc current) and $\underline{Y}$ the vector of output quantities. Figure 2.2.1a shows the block diagram for the system described by equation 1.

The equation for the state variables is then solved as

$$\Delta\underline{X} = A\underline{X}\,\Delta t + B\underline{u}\,\Delta t \tag{2}$$

and $\underline{X}_{new} = \underline{X}_{old} + \Delta\underline{X}$, the process being continued with small Δt steps from start to finish.

Another advantage of this type of approach is that it allows sources to be of the most general type. For example, the 'source' may be another system with state equations: (See Fig. 2.2.1b)

$$\dot{\underline{Z}} = K\underline{Z} + H\underline{X} + J\underline{p} \tag{3}$$

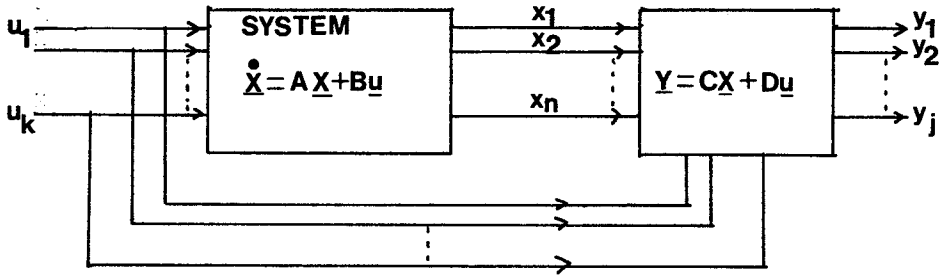
i.e.,

$$\Delta\underline{Z} = (K\underline{Z} + H\underline{X} + J\underline{p})\,\Delta t \tag{4}$$

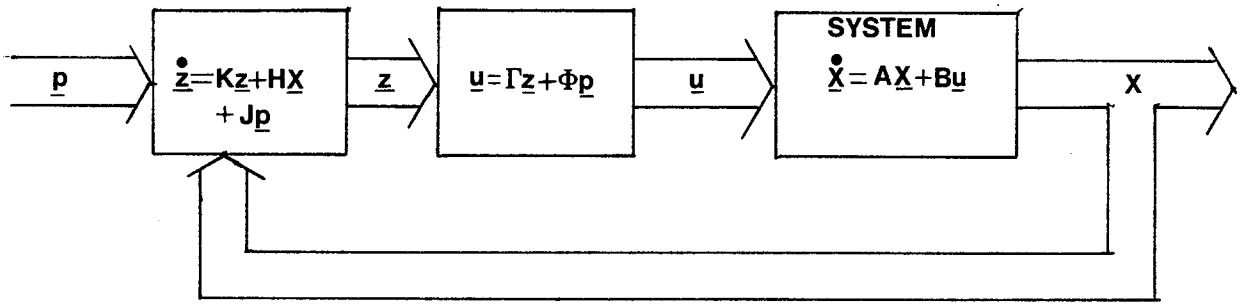
where $\underline{Z}$ is the source's own internal state vector, and the state variables of the inverter system ($\underline{X}$) as well as internal source inputs ($\underline{p}$) act together as inputs. Then the inputs to the inverter system may be

---

* For a review of the state variable concept, the reader is referred to reference [12].



a) BASIC SYSTEM



b) BASIC SYSTEM WITH ARBITARY "SOURCE"

FIG 2.2.1 : STATE VARIABLE REPRESENTATION

determined by the equation

$$\underline{u} = \Gamma \underline{Z} + \Phi \underline{p} \qquad (5)$$

The solution then proceeds as follows:

i) Initial values for $\underline{X}$ and $\underline{Z}$ are chosen say $\underline{X}(0)$, $Z(-1)$, where $\underline{X}(k)$ is short for $\underline{X}(k\Delta t)$, and so on.

ii) (4) is now solved to evaluate $\Delta \underline{Z}$, and hence the updated value for $\underline{Z}$. ($\underline{Z}(0)$ say).

iii) $\underline{u}$ is then obtained from (5)

i.e., $\underline{u}(0) = \Gamma \underline{Z}(0) + \Phi \underline{p}(0)$

iv) (2) is now solved for $\Delta \underline{X}$: and then the new $\underline{X}$ is obtained as:

$$\underline{X}(1) = (A\Delta t + I)\, \underline{X}(0) + B\, \underline{u}(0)\, \Delta t$$

v) This is then re-substituted in (4) to get $Z(1)$, from which $\underline{X}(2)$, etc. are calculated exactly as before. Finally, the following array is obtained:

$(\underline{X}(0), \underline{X}(1), \ldots\ldots)$ which gives the history of the system, and from which can be calculated other quantities of interest. This method of handling arbitrary sources is very convenient when considering the weak system (to be considered later).

A state equation solution, though convenient, is time consuming. In order to save time, a direct solution may be used between commutations, when the capacitors are being charged with a constant dc current. The state equation solution is carried out only during the commutation interval. This hybrid approach to the problem has the advantage of being universally applicable (to all types of sources) as well as of being fast.

A very important point which should not be missed is that given an initial condition, the state variable approach allows for a transient solution because the system array $(\underline{X}(0), \underline{X}(1), \ldots\ldots)$ gives the

complete history of the system. This is the aspect in which the author's solution method differs from previous ones [5, 8].

2.2.2 The circuit

As mentioned earlier, the state equation time stepped solution is used only during the commutation interval, and a direct solution during the constant charging interval between commutations. Figure 2.2.2 shows the model used during the commutation period. With respect to Fig. 1.5.1, assume that phases a and c were conducting (Thyristors 1 and 2), and now 3 is forced to take over from 1. As constant current keeps flowing in phase c, it is not included in the state variable calculations. Figure 2.2.2 has been relabled in terms of e_1, e_2, V_{c1}, V_{c2} etc., and not e_a, e_b, etc., because the analysis holds for commutation from <u>any</u> phase to <u>any</u> other, and so in the figure the subscript 1 stands for the off-going phase, and 2 for the oncoming phase. In terms of Fig. 2.2.2, we select the state variables to be the capacitor voltages (V_{c1}, V_{c2}) and the loop current (i). Knowing that $C_1 = C_2 = C$, $\ell_1 = \ell_2 = \ell$, we may write the state equations as:

$$\frac{d}{dt}\begin{bmatrix} V_{c1} \\ V_{c2} \\ i \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1/C \\ 0 & 0 & 1/C \\ 1/(2\ell) & -1(2\ell) & 0 \end{bmatrix}\begin{bmatrix} V_{c1} \\ V_{c2} \\ i \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & -1/C \\ 1/2\ell & -1/2\ell & 0 \end{bmatrix}\begin{bmatrix} e_1 \\ e_2 \\ I_D \end{bmatrix} \tag{6}$$

which is in the form

$$\dot{X} = A\underline{X} + B\underline{u}, \quad \text{with} \quad \underline{X} = \begin{bmatrix} V_{c1} \\ V_{c2} \\ i \end{bmatrix}, \quad \underline{u} = \begin{bmatrix} e_1 \\ e_2 \\ I_d \end{bmatrix}$$

and A and B the corresponding matrices.

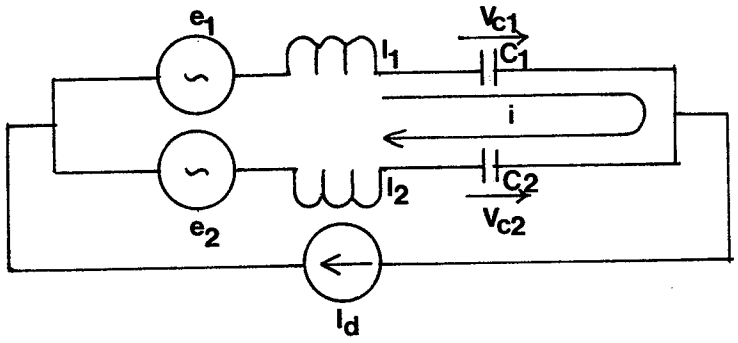


FIG 2.2.2 : EQUIVALANT CIRCUIT DURING COMMUTATION

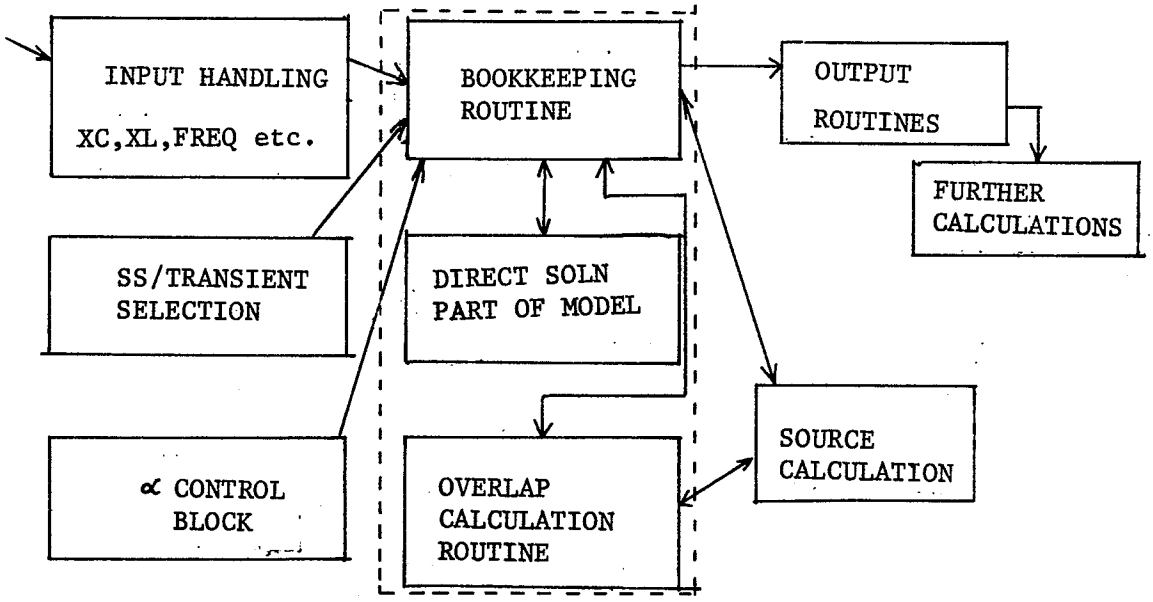


FIG 2.2.3 : PROGRAM BLOCK ORGANIZATION

The initial conditions are;

$$\begin{bmatrix} V_{c1} \\ V_{c2} \\ i \end{bmatrix}(0) = \begin{bmatrix} V_{c10} \\ V_{c20} \\ I_d \end{bmatrix} \tag{7}$$

The commutation ends at time t_1 when

$$i(t_1) = 0.$$

During the constant charge process, the current in the phase concerned is obviously I_d, and the capacitor state variable is directly solved for as (with the beginning of this period as the time origin).

$$V_c(t) = \frac{I_d}{C} t \tag{8}$$

This is the direct solution mentioned earlier.

Note that at every commutation, the phases that are conducting change, but the same state equations are applicable, of course with the proper initial conditions. Thus, there is need for a 'bookkeeping' routine which keeps track of the phases going off and coming into conduction, and gives the right initial conditions to the state equation/direct solution sections of the program. It is also the responsibility of the bookkeeping routine to load the proper matrices (capacitor voltages in all phases as a function of time, etc.).

2.2.3 The programming for this circuit

Figure 2.2.3 shows a block diagram of the organization of the overall program. The blocks are explained below:

i) A bookkeeping routine as explained above.

ii) An overlap routine with the time-stepped state equation solution as in equation 6.

iii) A direct solution block for periods between commutation.

iv) A source calculation program containing a state variable representation of the source (as explained before).

v) A selection for transient/steady-state (s.s.) solution. The selection is made through an integer variable ISS, which is set to 1 for the s.s. solution, 0 for a transient solution. If ISS = 0, the first 8 commutation intervals are recorded. If ISS = 1, then the simulation is continued until steady-state is reached, and the final waveforms over a period are stored. The block labelled 'α control', allows for a control of the firing angle during the simulation. This block is of made use of during the study of the rate of change of firing angle.

vi) Input/output Handling blocks.

Figure 2.2.4 shows a high-level flowchart of the entire process.

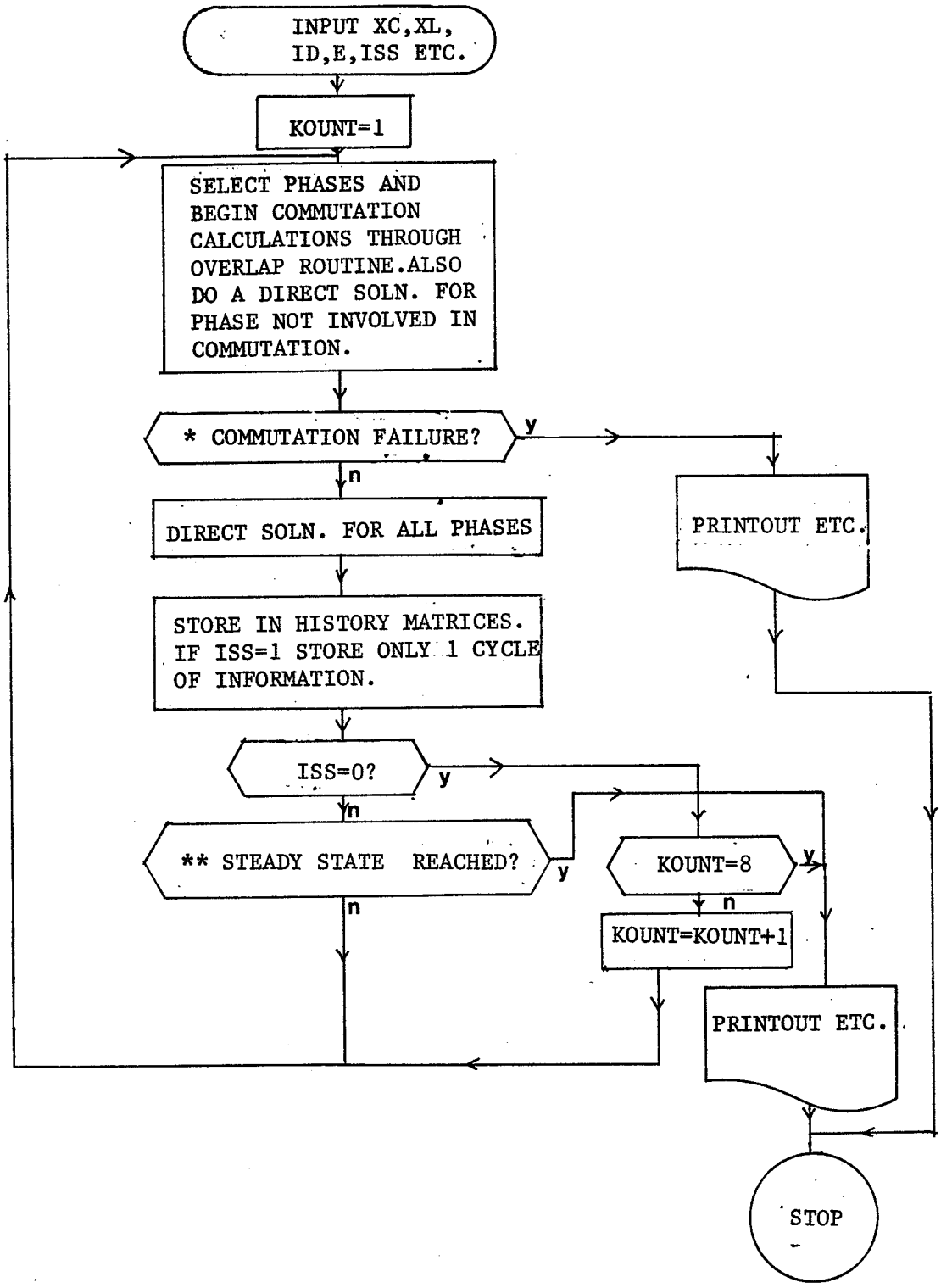
2.3 Fault Studies

As mentioned earlier, other kinds of faults such as commutation failure, arcback, etc., have been studied by J. Baron and others [5,8]. This study deals with ac side faults beyond the converter transformer only.

2.3.1 Fault types [7]

AC faults may be divided into 2 categories: near and distant, the effects of which are well known for the case of the normal 3-phase Graetz Bridge.

Distant faults are those that occur 'electrically far' from the converter, and have the effect of lowering the ac voltage available to the converter for commutation; and thus increasing the risk of



* COMMUTATION FAILURE CHECKED BY DETERMINING IF I IS INCREASING IN OVERLAP ROUTINE.

** SS. REACHED IF OVERLAP ANGLE IS ALMOST CONSTANT FOR THREE CONSECUTIVE ITERATIONS.

FIG 2.2.4 :HIGH LEVEL FLOWCHART FOR BASIC ROUTINE.

commutation failure.

Near faults are those which lead to a complete collapse of ac voltage at the inverter bus. For the naturally commutated inverter, these are the most severe type of faults and result in commutation failure in case the fault is a three phase one, and also if it is a single phase one and if it lies on the phase coming into conduction.

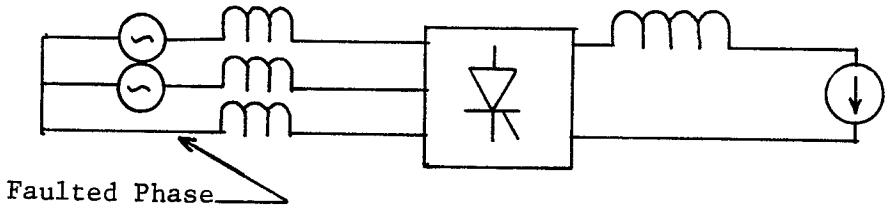
2.3.2 Program development

As they are expected to be the most severe ones, only near faults (both 1-phase and 3-phase) have been studied.

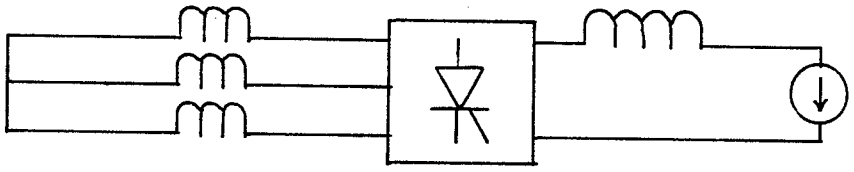
The fault to be simulated can be made to occur at any desired position in a cycle. The duration of the fault is controllable. The program used is essentially the same as the basic routine discussed earlier, except for a modified 'source' program. Source conditions are changed during fault times to represent a complete voltage collapse in the appropriate phase(s). Fault conditions are tracked through an integer variable JSTAT which is set to 0 for prefault conditions, to 1 during the fault and to 2 after the fault. As long as JSTAT is 1 the 'source' program keeps the phase voltages zero. JSTAT is kept at 1 until the fault period has elapsed.

If there is no commutation failure, the program increases the fault duration automatically, and does the simulation again. The process is continued until a commutation failure occurs. The corresponding fault duration has been termed the 'critical fault period' for their operating conditions; *i.e.*, it is the minimum fault duration for which the system collapses.

Figure 2.3.1 shows the equivalent source picture during faults, and fig. 2.3.2 is a flow diagram of the simulation.



a) SINGLE PHASE FAULT



b) THREE PHASE FAULT

FIG 2.3.1 : FAULT REPRESENTATION

2.4 Analysis of Harmonics

A study of the harmonics generated by the series capacitor commutated inverter is important from the point of view of determining the filter requirements. One can expect the dc voltage harmonics to be very high in this case due to the presence of the commutating capacitors, The ac current harmonics would be expected to be the same as in a naturally commutated inverter.

2.4.1 Voltage harmonics

Because of the 6-phase nature of the bridge, the dc voltage at the output (as in a naturally commutated bridge) is periodic with a period 1/6 times the ac fundamental period. This means that the harmonics present are multiples of the 6^{th}. Hence in the following analysis, $T = 1/6 \times (2\pi/\omega)$ has been chosen as the fundamental period of the waveform. Likewise, the calculated k^{th} harmonic with respect to this

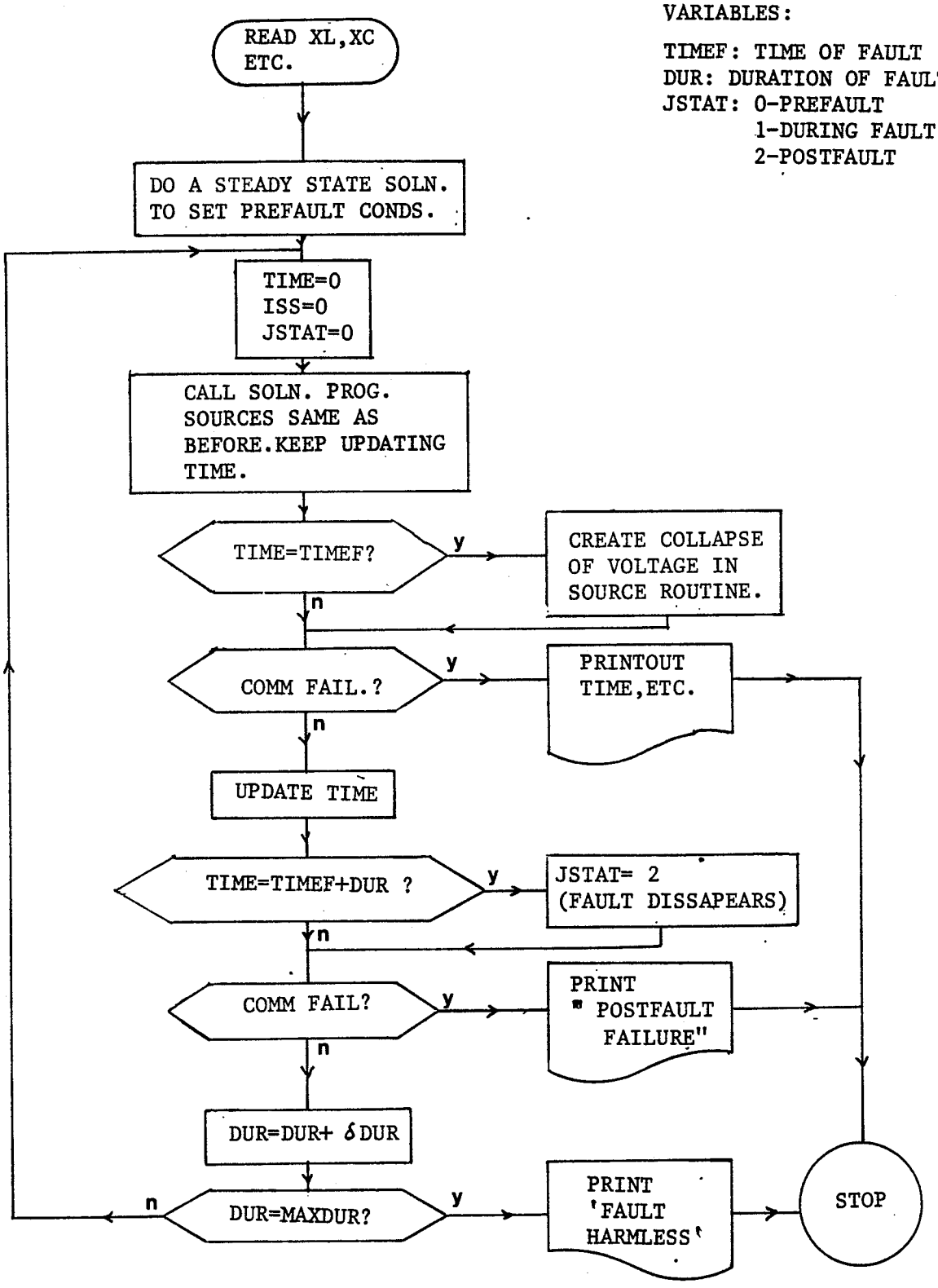


FIG 2.3.2 : FAULT STUDY: FLOWCHART

period, is actually the $6\,k^{th}$ harmonic with respect to the ac voltage frequency. If $V(t)$ is the voltage as a function of time, a Fourier Analysis gives the coefficients of the n^{th} harmonic (a_n, b_n) as

$$a_n = \frac{2}{T}\int_o^T V(t)\,\cos\frac{2\pi nt}{T}\,dt$$

$$b_n = \frac{2}{T}\int_o^T V(t)\,\sin\frac{2\pi nt}{T}\,dt \qquad (9)$$

and the average (dc) value given by

$$a_o = \frac{1}{T}\int_o^T V(t)\,dt \qquad (10)$$

In this study, $V(t)$ was available as a vector $[V(1), \ldots\ldots V(k) \ldots\ldots]$ where $V(k)$ is the value of $V(t)$ at the k^{th} instant of time, *i.e.*, $V(k\Delta t)$, where Δt is the step length after which voltages are evaluated. Thus, (9) and (10) above may be approximated as:

$$a_n \simeq \frac{2}{T}\,\Delta t \sum_{m=0}^{N} V(m)\,\cos\left(\frac{2\pi nm}{T}\,\Delta t\right)$$

$$b_n \simeq \frac{2}{T}\,\Delta t \sum_{m=0}^{N} V(m)\,\sin\left(\frac{2\pi nm}{T}\,\Delta t\right) \qquad (11)$$

$$a_o \simeq \frac{\Delta t}{T} \sum_{m=0}^{N} V(m) \qquad (12)$$

with $\quad T = 1/6(2\pi/\omega)\,, \quad N = \text{integer}[2\pi/(6\omega\Delta t)]$.

The net harmonic content in the $6\,k^{th}$ harmonic is then

$$c_n = \sqrt{a_n^2 + b_n^2} \qquad (13)$$

Thus, the procedure used to obtain harmonics makes use of the 'basic' program to find $V(k)$, and then makes use of (11), (12) and (13) to evaluate the harmonics.

2.4.2 Current harmonics

The procedure is similar to that used for voltage harmonics, and involves first obtaining the current as a function of time over one period, in vector form and then numerically integrating it to obtain the Fourier coefficients. The period T, however is now $2\pi/\omega$. Another difference is that the even harmonics need not be calculated because the waveform is anti-symmetric w.r.t. the half period, *i.e.*, $i(t) = -i(t - T/2)$. Also, the triplen harmonics (3^{rd}, 9^{th}, etc.), need not be calculated because the star connected transformer winding should eliminate these. However, their calculation has been retained because zero values are an added information that the procedure used is correct.

Figure 2.4.1 gives the flowchart for harmonic calculations.

2.5 Rate of Firing Angle Change

It is important to know the rate at which firing angle may be changed from the point of view of having fast control on the inverter. This is not so easily possible in this case because of the requirement of proper capacitor voltages for commutation. In this analysis, it is assumed that the firing angle α is changed from its initial value α_o to its final value α_f in a linear fashion. The situation is shown in fig. 2.5.1, and may be expressed quantitively as:

$$\alpha = \alpha_o \quad , \text{ for } t \leq t_o$$

$$\alpha = \alpha_o + \frac{(\alpha_f - \alpha_o)}{k} \times n \quad , \quad t_o < t \leq t_f \qquad (14)$$

in the n^{th} commutation interval

$$\alpha = \alpha_t \qquad t_f < t$$

Thus, the firing angle α is changed in k steps to its final value. Note that it does not make sense to say α is changed continuously, rather than in discrete steps, because α is a constant in every commutation interval.

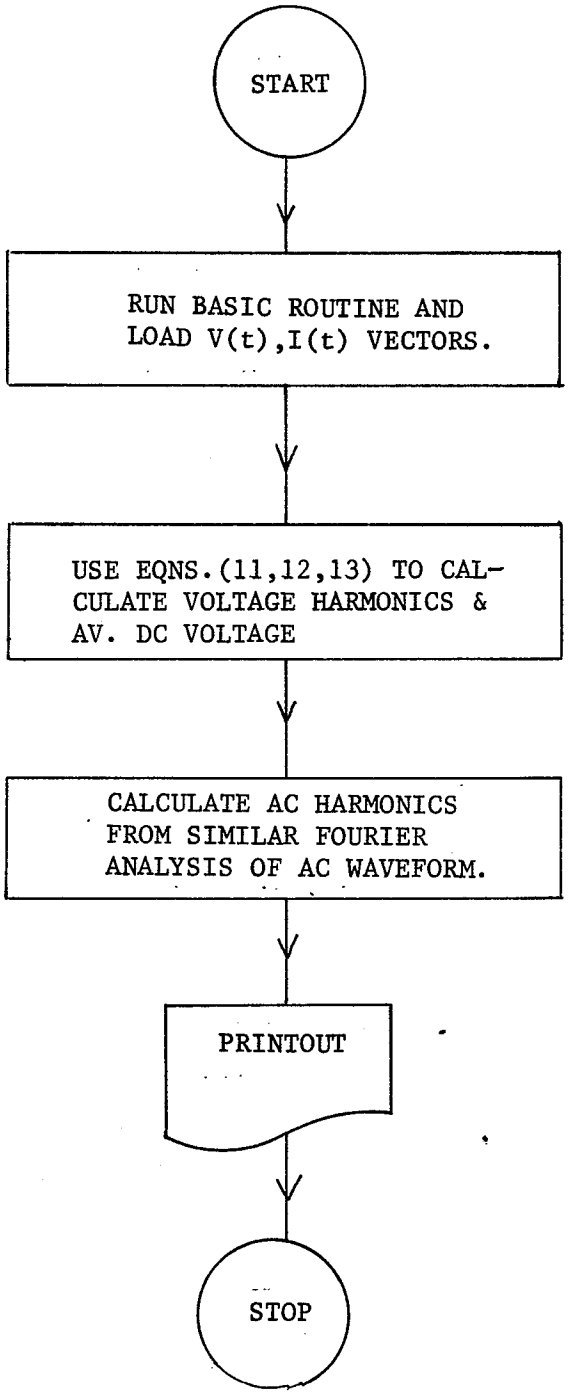


FIG 2.4.1 :HIGH LEVEL FLOWCHART FOR HARMONIC CALCULATIONS.

The aim is to find the smallest value of k possible so that the transfer takes place in the smallest number of steps.

The program, which is flow charted in Fig. 2.5.2 operates as follows:

1. A starting value for k, *i.e.*, $k = k_s$, is selected.
2. The steady-state/transient selection variable ISS (see Sec. 2.2.3) is set to 1 for a steady-state analysis, and a steady-state solution is obtained, and stored in memory.
3. The transient solution is now asked for by re-setting ISS to 0, and the angle α changed in k steps from α_o to α_f.
4. ISS is set to 1, and the system allowed to stabilize to its new steady-state value at $\alpha = \alpha_f$.
5. If there is commutation failure during steps 3 and 4 the same two steps (3 and 4) are repeated with k replaced by $k + 1$.
6. The process is continued until at some value of k, commutation failure does not occur. This value of k gives the minimum number of steps in which α may be changed.

The starting value $k = k_s$ is normally selected to be $k_s = 1$, but for $\alpha_0 - \alpha_f \geq 60°$, *i.e.*, for a retardation of firing angle; we select

$$k_s = \text{integer } [\frac{\alpha_o - \alpha_f}{60°}] + 1 \qquad (15)$$

where the first term stands for a truncation of $(\alpha_o - \alpha_f)/60°$ to an integer value. This is done because choosing any smaller value for k_s would mean effecting the change in negative time.

2.6 Per Unit System

In order to make the studies universally applicable, a per unit system is necessary. This is not so easily done for an HVDC converter as

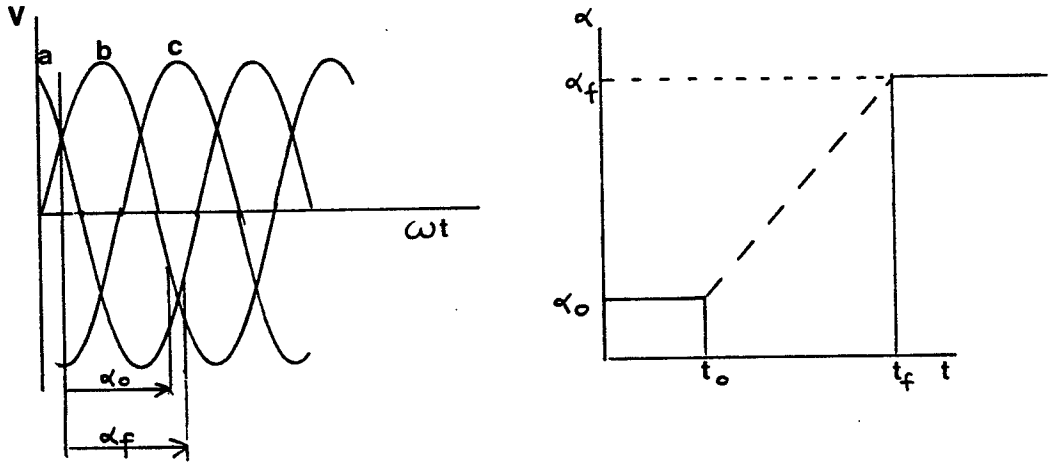
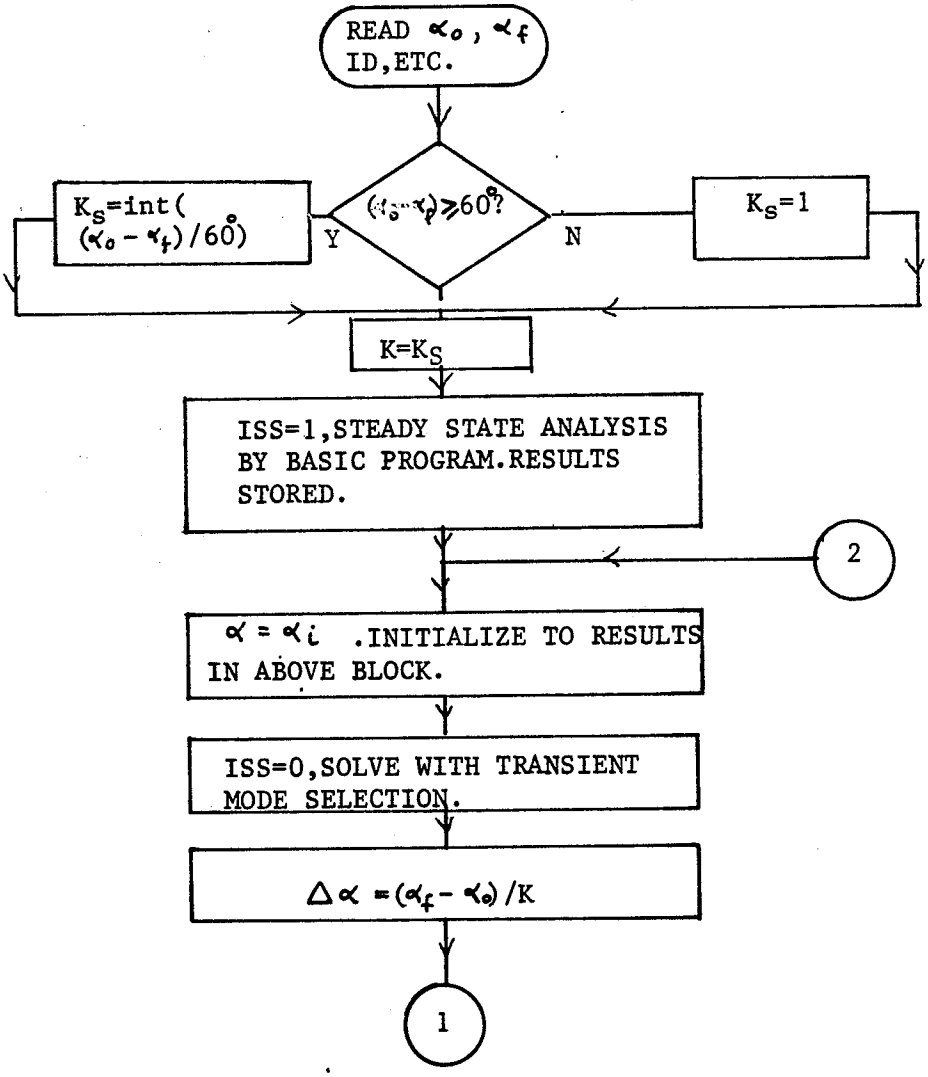


FIG 2.5.1 : CONTROL OF FIRING ANGLE



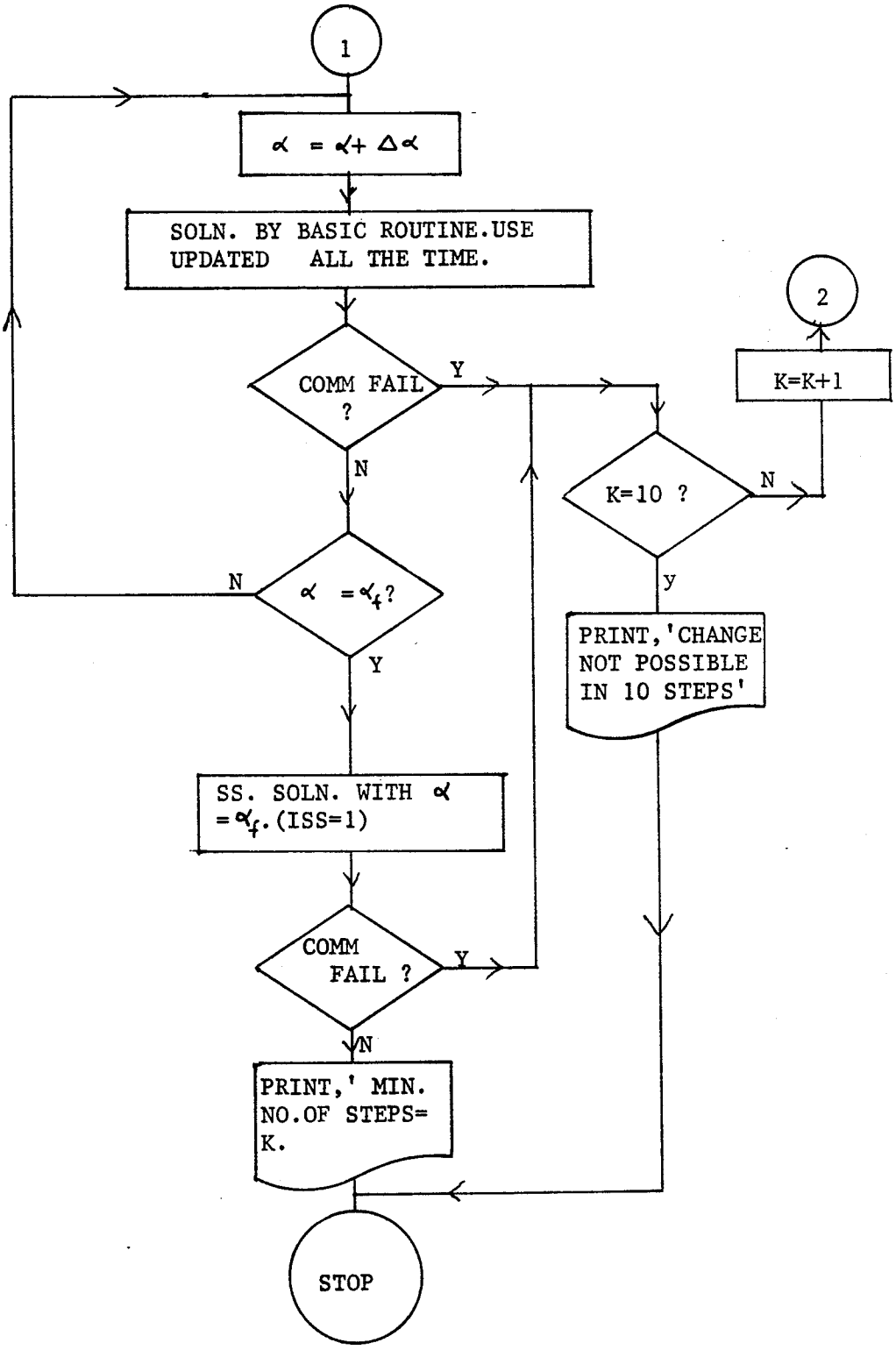


FIG 2.5.2: FLOWCHART FOR FIRING ANGLE CHANGE STUDIES.

it is for example, for a transformer. The voltages and currents on either side of the transformer satisfy the relation:

$$I_s^* V_s = I_p^* V_p ,$$

i.e., the complex power on the primary and secondary sides are constant. Thus, any arbitrary base quantities (V_{bs}, I_{bs}, V_{bp}, I_{bp}) may be chosen on the secondary and primary sides, as long as they satisfy the relation

$$V_{bs} I_{bs} = V_{bp} I_{bp}$$

i.e., constancy of complex power.

In the case of a converter there is no complex power on the dc side. It is the real power on the ac and dc sides that is invariant. Thus, a p.u. system base is selected which gives this invariance. Thus, the dc line current and the ac side voltage are chosen as base quantities. This is reasonable because then under normal conditions the system handles 1 p.u. voltage and current though not 1 p.u. power.

Now the ac base current may be selected as the ac current which flows when the system handles rated current and voltage at rated power. The ratio between ac base current to dc base current may then be used to and from conversion to actual system quantities. In this analysis, this ratio has been assumed to be $\sqrt{6}/\pi$, which is the ratio when there is no overlap. This is done because under normal operating conditions the overlap angle is small. Anyway, the analysis is more concerned with a study of general behaviour and hence this approximate relation is quite adequate. For example, a 0,14 per transformer leakage reactance on the ac side would now be 0,18 p.u. ($0,14 \times \pi/\sqrt{6}$) in the new p.u. representation.

In the chapters to follow, the results of the programs developed in this chapter are discussed. While doing the solutions, all the equations

derived have been converted to p.u. quantities. The results are thus all in p.u.

The flowcharts given here are only high level flowcharts. For detailed flowcharts, program listings and user information on the programs, the reader is referred to another technical report by the author [11].

CHAPTER 3

PROGRAM RESULTS AND DISCUSSION

3.1 Introduction

As mentioned in Chapter 2, a basic program was developed which could do a steady-state, transient, or combined solution for the operation of the series capacitor commutated inverter. This program assumes the same model as Reeves et al [5], (though a different method of solution) and consequently, as verified, yields the same steady-state solutions that Reeves et al obtained. However, the program has the capability of being used for transient studies as well. This chapter discusses the transient studies such as fault studies and rate of change studies, as well as a steady-state harmonic analysis carried out using the basic model. The program developments have already been discussed in the previous chapter; here, only the results are analyzed.

3.2 Fault Studies

The program discussed in Section 2.3 was run to obtain the 'critical fault time' (the maximum period for which the fault may remain on the bus without causing commutation failure) for near ac faults. Near faults, which are the most severe kind of ac faults - at least for the naturally commutated inverter, are faults in which there is a complete collapse of ac voltage in the faulted phase(s). The results indicate that for normal operating conditions, the inverter is practically immune to ac side faults.

3.2.1 Cases studied

The following cases were studied:

3-phase faults: Effect of I_d on the critical fault time for varying X_c.

1-phase faults: a) Effect of I_d on critical fault time for varying X_c.

b) Effect of I_d on critical fault time for varying α.

The results are shown in Figs. 3.2.1 and 3.2.3 a and b.

3.2.2 Discussion of results

3 - ϕ Faults

1. It should be noticed that the fault affects inverter operation only if present during the commutation interval. Since the voltage build up on the capacitors (which is necessary for commutation) is dependent mainly on the dc current's magnitude, a fault that occurs in between commutations will not change the situation until the coming commutation. During the commutation, the sole effect of the fault will be to lower the voltage in the faulted phases. Hence, if the inverter can successfully operate over one commutation interval, it will continue to do so even if the fault remains on the line indefinitely, because the conditions during the next commutation will be identical to the ones during the previous commutation as the fault does not affect capacitor charging.

2. Unlike the case of the normal 3-phase Graetz bridge, a sustained voltage collapse need not mean commutation failure. This is so because the forced commutated inverter generates its own commutation voltage, and does not rely on the ac system voltage for commutation, except at very low values of currents with firing angles less than 180°. In fact for firing angles in excess of 180°, a 3-phase fault improves commutation, because the source voltage which subtracts from

the capacitor voltage, is now absent. In fact, in the study, abnormally low values for X_c (< 0.7 p.u.) and high values for voltage (1.2 p.u.) had to be chosen to cause commutation failure (Fig. 3.2.1) over the entire range of operating currents, even for an indefinitely sustained voltage collapse.

A normally designed system would have $X_c > 0.7$ p.u., and $V_\ell = 1$ p.u., and hence would be immune to 3-phase faults.

Figure 3.2.1 also shows that the critical time increases for increasing X_c, and is infinite for $X_c > 0.7$ p.u.

Single Phase Faults

1. As explained above, since the commutation voltage is mainly derived from charging the capacitors, the operation of the forced commutated inverter is more stable than that of the naturally commutated one, even for single phase faults. Figure 3.2.2 shows the phase voltages V_a, V_b, V_c. V_{ba} is the source's contribution to the commutation voltage during normal operation. For a fault on phase a V_b is the voltage available, and for a fault on phase b, it is $-V_a$. An inspection of Fig. 3.2.2 and the corresponding voltage available yields the results shown in Table 3.2.1. The underlined items represent the more severe cases. It is assumed that all faults occur at the start of a commutation.

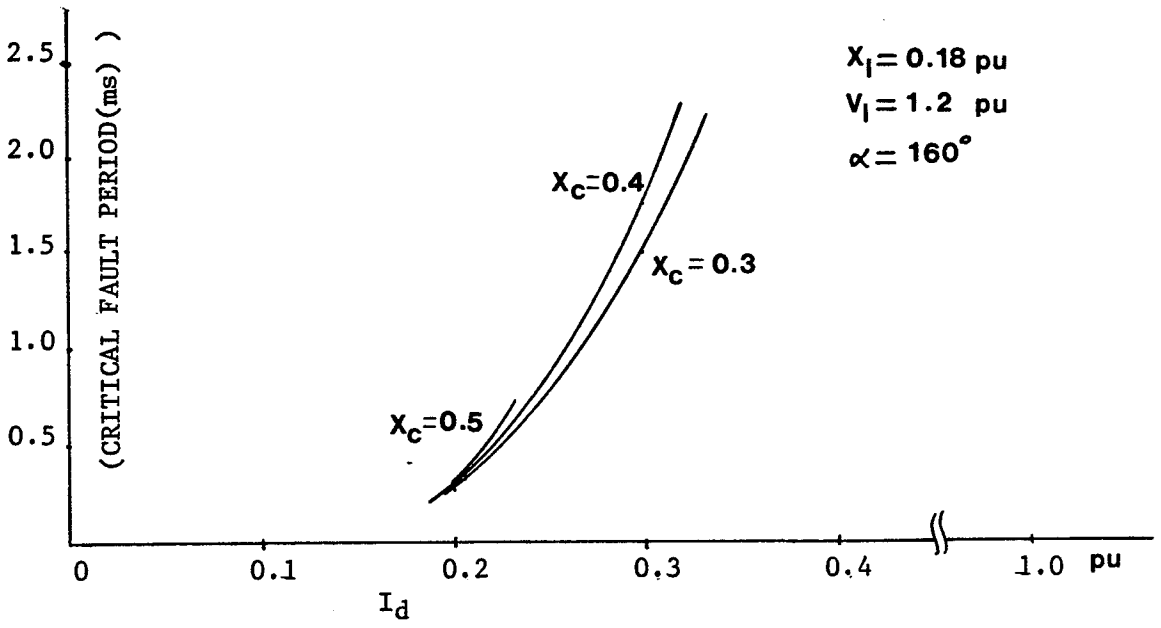


FIG 3.2.1 : EFFECT OF 3-PHASE FAULTS ON COMM.FAILURE.

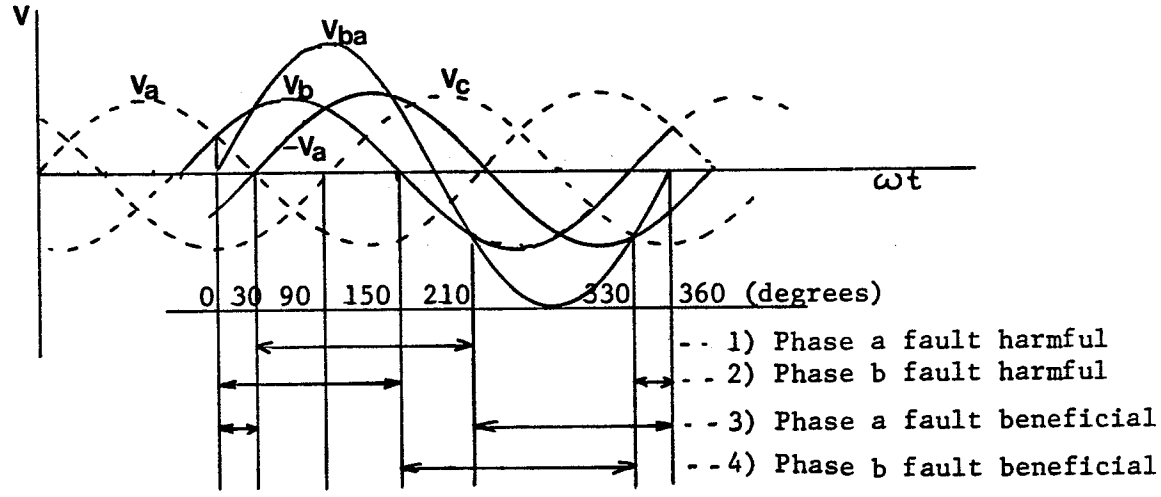


FIG 3.2.2 : 1-PHASE FAULTS: EFFECT OF FAULT POSITION

Firing Angle	Effect of a phase 'a' fault	Effect of a phase 'b' fault
$0° < \alpha \leq 30°$	beneficial (to commutation)	harmful
$30° < \alpha \leq 90°$	harmful	harmful
$90° < \alpha \leq 150°$	harmful	harmful
$150° < \alpha \leq 210°$	harmful	beneficial
$210° < \alpha \leq 330°$	beneficial	beneficial
$330° < \alpha \leq 350°$	beneficial	harmful

TABLE 3.2.1: EFFECT OF $1 - \phi$ FAULTS

Thus it is seen that there are certain ranges of firing angle in which a fault actually improves commutation.

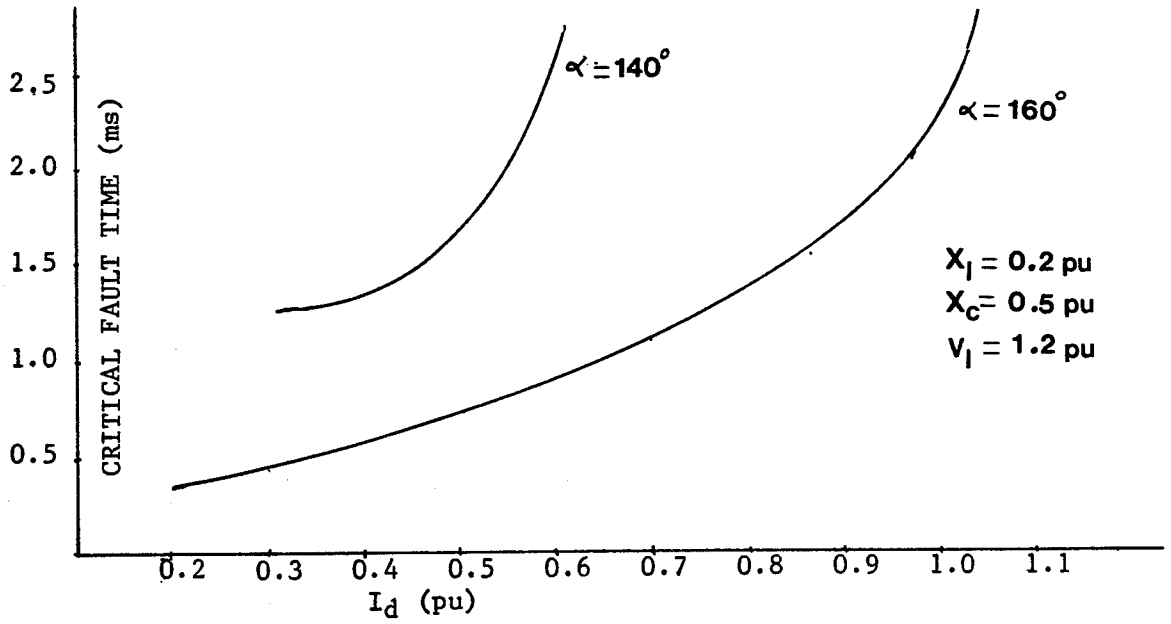
2. For inverter operation $(90° < \alpha < 270°)$, it is seen that a fault on phase a is the most harmful (for commutation from phase a to b), and thus it is the fault that has been studied.

3. As seen from Fig. 3.2.3(a), a fault at $140°$ is less critical than one at $160°$, something to be expected on account of the smaller source voltage available for commutation at $180°$.

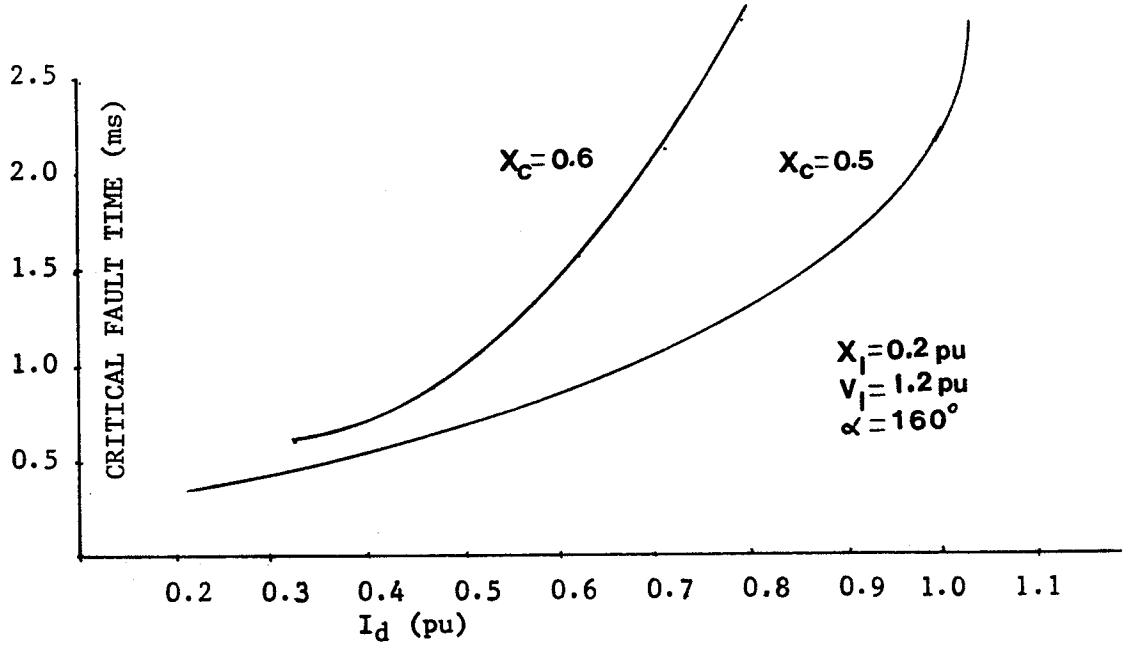
4. Figure 3.2.3(b) shows that as X_c increases, the severity of the fault decreases. In fact it is possible to have failure-free operation for a sustained fault for $X_c > 0.8$ over the entire region of operation.

Conclusion

The values for which the graphs have been drawn are quite different from those probable on an actual inverter, which would have a much larger X_c and an ac system voltage of about 1 p.u., and consequently would be extremely secure from ac side faults.



a) CRITICAL FAULT TIME AS A FUNCTION OF DC CURRENT FOR VARYING FIRING ANGLE.



b) CRITICAL FAULT TIME AS A FUNCTION OF DC CURRENT FOR VARYING CAPACITOR REACTANCE.

FIG 3.2.3 : EFFECT OF 1-PHASE FAULTS ON COMM. FAILURE

3.3 Results of Study on Harmonics

The following studies were carried out based on the program outlined in Section 2.4.

1. Dependence of ac current harmonics on dc current.
2. Dependence of dc voltage harmonics on dc current.

Literature on HVDC inverters usually depicts the dependence of the harmonics on the overlap angle. Here, dc current, and not the overlap angle has been chosen as the varying quantity. This is so because the dc harmonics are mainly due to the presence of the commutation voltage on the capacitors. The maximum capacitor voltage is directly proportional to the dc current, and in fact may be considerably different for two cases in which the overlap angles are the same but the dc currents are different. Hence it is the dc current magnitude that primarily affects the dc voltage harmonics, and hence the selection of dc current as the horizontal axis in the graphs. Figure 3.3.2 shows typical ac current and dc voltage waveforms, Figures 3.3.3 and 3.3.4 show the dependence of current and voltage harmonics on dc current.

3.3.1 Current harmonics

Unlike the voltage harmonics, the current harmonics depend mainly on the overlap angle. This is so, because for zero overlap angle the ac waveform is essentially a squarewave which has a fixed harmonic content. Any deviation of the harmonic content from that of a square wave is due to the presence of a finite overlap angle, and to a first degree of approximation is a function only of the overlap angle. The greatly simplified derivation below shows that for operation in the vicinity of 180° (the inverter will normally be operating in this vicinity) the overlap angle is independent of the dc current. It is assumed that the

capacitor voltage is approximately constant during commutation - a reasonable assumption especially if the commutation period is small. The argument is based on Fig. 3.3.1 below:

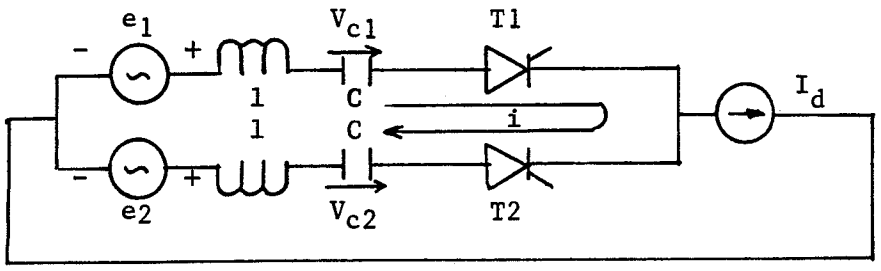


FIG 3.3.1 : COMMUTATION FROM PHASE 1 TO PHASE 2

We have (with i as the loop current as shown)

$$V_{c_1} + e_1 - V_{c_2} - e_2 - 2\ell \frac{di}{dt} = 0 \qquad (1)$$

Now $e_1 \simeq e_2$ as $\alpha \simeq 180°$

and $|V_{c_1}| = |V_{c_2}| = k\, I_d$ because the capacitor peak voltage is directly proportional to the dc current. As V_{c_1} and V_{c_2} are opposite in sign, and V_c has the positive sign, we have

$$2\ell \frac{di}{dt} \simeq -2k\, I_d \qquad (2)$$

or $$i(t) = \frac{-k}{\ell} I_d\, t + I_d \qquad (3)$$

where we have used the initial condition

$$i(0) = I_d.$$

As commutation is complete at $t_f = \mu/\omega$ where μ is the overlap angle, we have

$$i(t_f) = 0 = \frac{-k}{\ell} I_d\, \mu/\omega + I_d \qquad (4)$$

or $$\mu = \ell\omega/k \qquad (5)$$

which is independent of I_d!

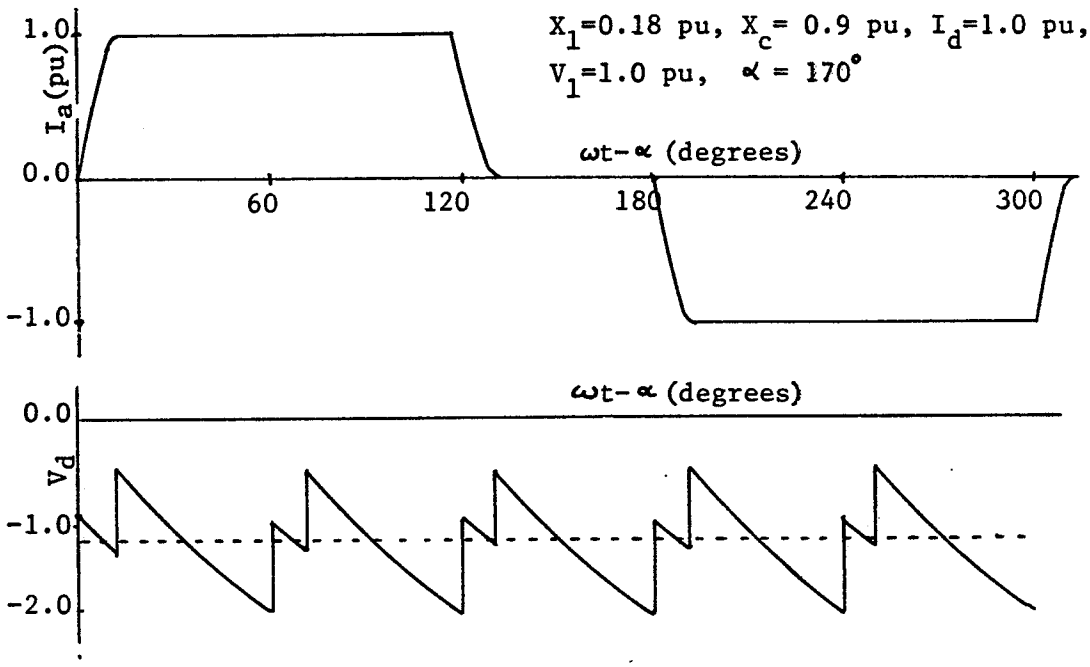


FIG 3.3.2 : AC CURRENT AND DC VOLTAGE WAVEFORMS

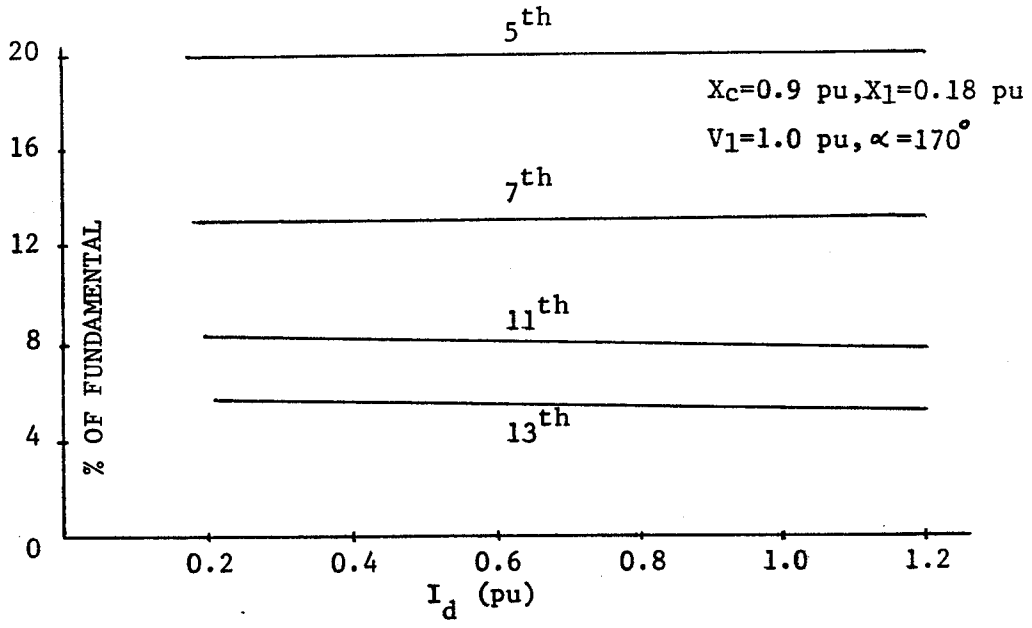


FIG 3.3.3 : CURRENT HARMONICS AS A FUNCTION OF DC CURRENT

This means that the harmonics are constant with I_d. This is verified in Fig. 3.3.3. It can also be seen that (as expected) for small overlap angles, the harmonics are approximately those in a square wave (33% for 3^{rd}, 20% for 5^{th}, 14.3% for 7^{th}, etc.). This constancy of harmonic content over the entire range of operating currents means that ac side filters designed for a specific operating current would perform equally well at any operating current.

3.3.2 Voltage harmonics

As seen in Fig. 3.3.2, the voltage waveform is rich in harmonics, mainly due to the voltage across the commutation capacitors (which is constantly changing due to the charging dc current). This fact is reflected in Fig. 3.3.4 which shows a 6^{th} harmonic of up to 46% of the dc voltage, and a 12^{th} and 24^{th} harmonics reaching up to 10 - 12% of the average dc voltage. Note also that the 24^{th} harmonic is greater than the 18^{th}, and crosses the 12^{th}.

The 6^{th} and 18^{th} harmonics may be filtered out by having 12 pulse (2 bridge) operation (as is almost always the case). Even then, the 12^{th} and 24^{th} harmonics are large and hence, expensive filter equipment would be required. This may make the capacitor commutated inverter unsuitable as a major inverter. For a small tap on an HVDC line (with a voltage drop of about 10 - 15% of the major converter's dc voltage), however, from the dc line's point of view, the resulting harmonics are small. Such a scheme is shown in Fig. 3.3.5.

3.4 Results: Firing Angle Change Studies

Using the program developed in Section 2.5, the following studies on the rate of change of firing angle were carried out:

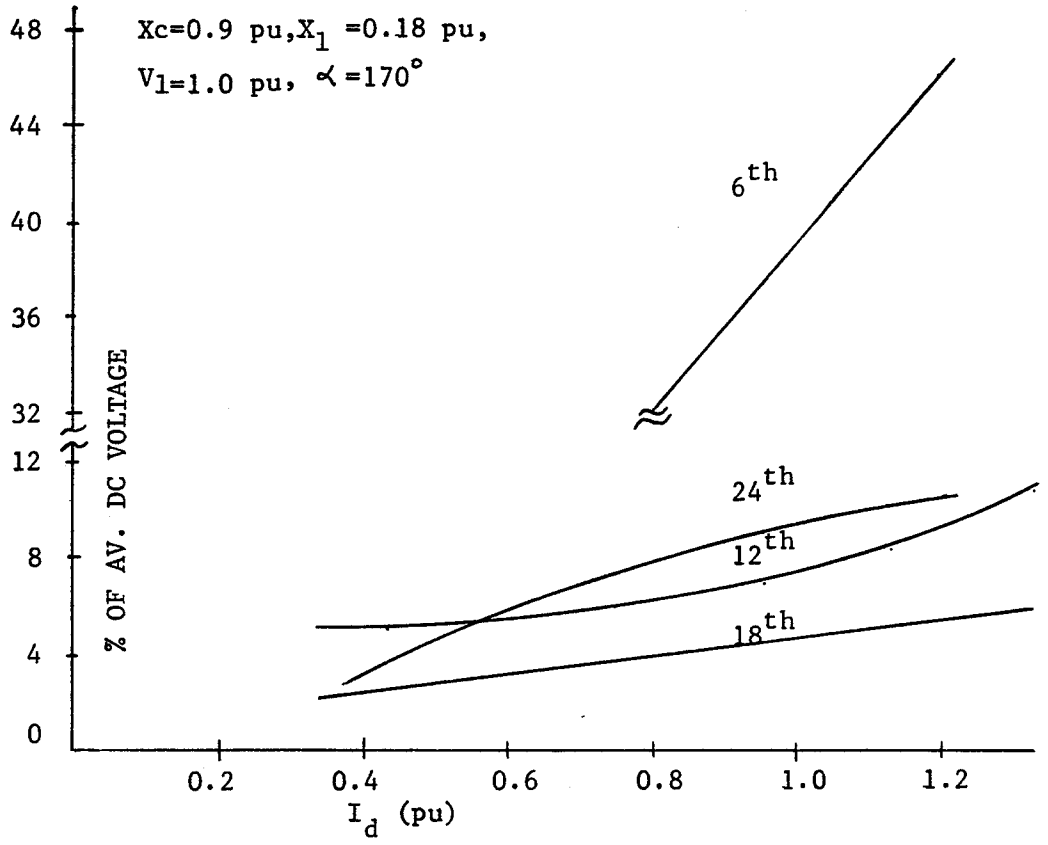


FIG 3.3.4 : DC VOLTAGE HARMONICS

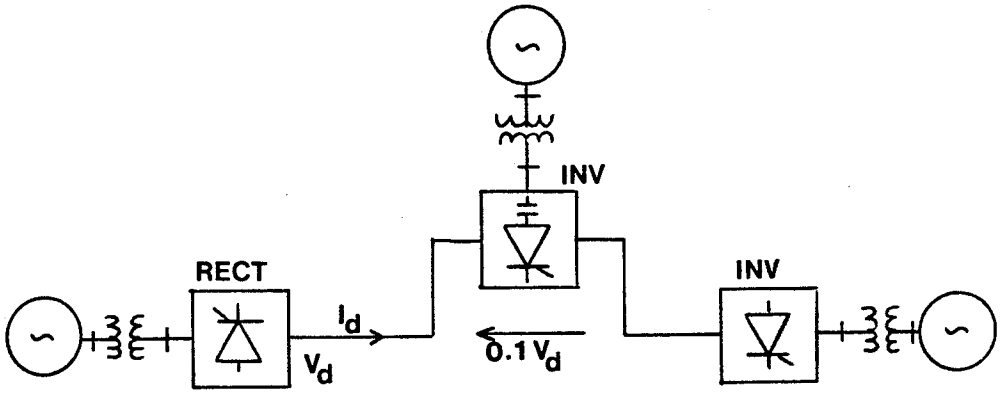


FIG 3.3.5 : SERIES TAPPED HVDC SCHEME (INVERTER)

1. Keeping X_c constant, the dependence of k (the minimum number of steps in which commutation may be achieved) on I_d was observed.
2. Keeping I_d and X_c constant, the dependence of k on $(\alpha_f - \alpha_o)$ - the net change in firing angle was observed.

The results are shown in Figs. 3.4.1 and 3.4.2.

Figure 3.4.1 shows the dependence of k on I_d for a firing angle change from 160° to 200° and also from 200° to 160°. The figure suggests that a reduction of angle (200° → 160°) can be made within 2 steps (~ 1/3 cycle), but that it may take up to 6 steps (~ 1 cycle) for an increase in firing angle.

It also shows that the angle may be changed faster for a larger dc current. This seems generally consistent with the observation of Reeve et al [5] (and easily verifiable with the 'basic' model) that commutation is much easier for larger dc currents (for currents larger than about 0.5 p.u. - see Fig. 1.5.3(a)).

Figure 3.4.2 shows the number of steps required for a symmetrical firing angle change of $\pm\delta°$ around 180°. As is to be expected, the number of steps increases with increasing δ. Note that small firing angle changes (±10°) can be made in 1 step (*i.e.*, instantaneously), and this permits the inverter to be used for power modulation, etc.

The analysis of firing angle rate of change gives an indication of the type of information required in designing a controller for firing angle changes. For effecting fast changes, a table of the required values of k for different operating conditions and desired angle changes may be stored in a digital controller's memory (possibly in associative memory). The required k would then be fetched and the controller would effect the change in k steps.

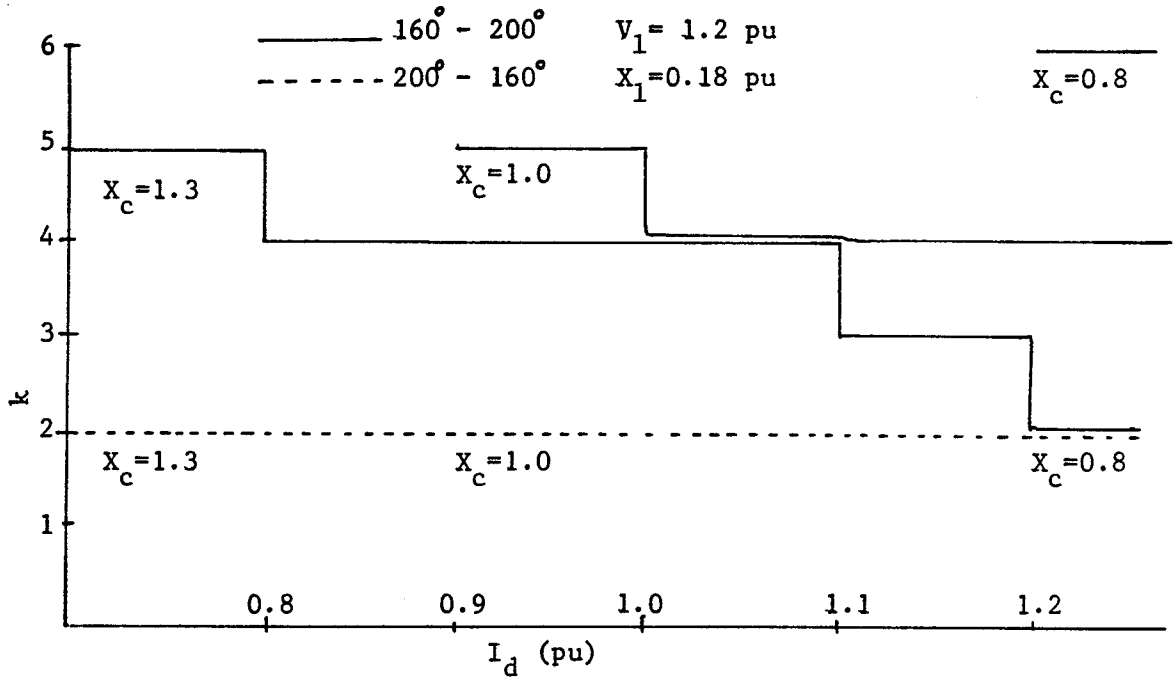


FIG 3.4.1 : VARIATION OF MAX. RATE OF FIRING ANGLE CHANGE WITH DC CURRENT

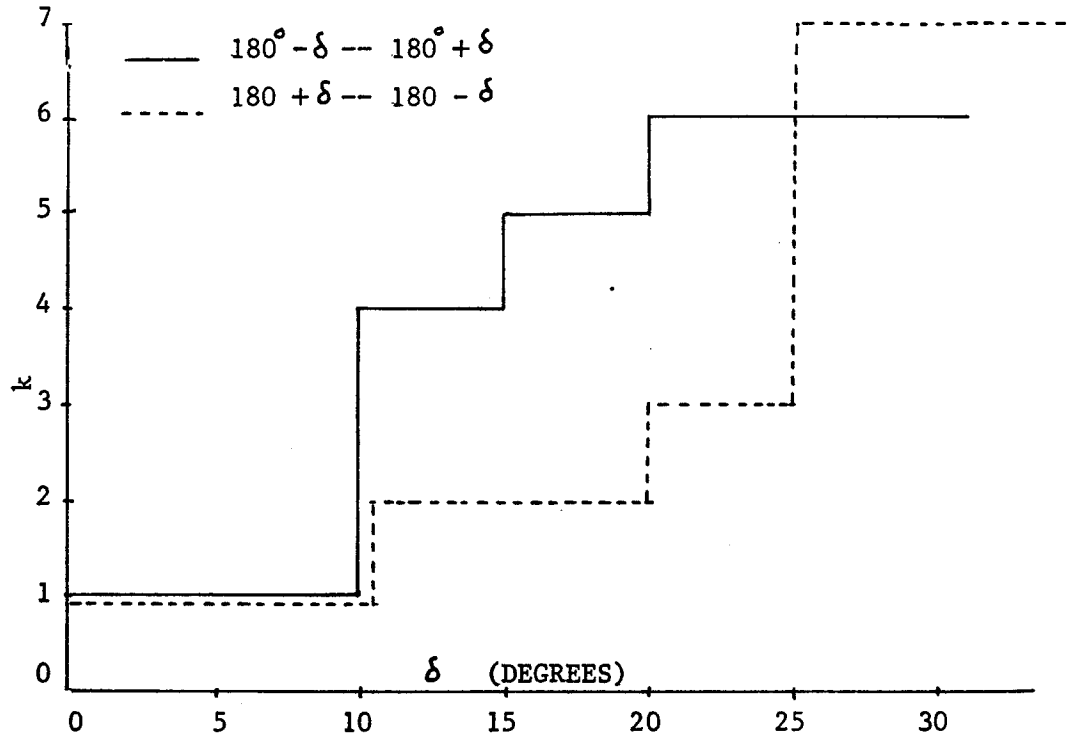


FIG 3.4.2 : VARIATION OF MAX. RATE OF FIRING ANGLE CHANGE WITH δ, FOR A SYMMETRICAL CHANGE AROUND 180°

3.5 Summary of Chapter

The conclusions of these studies are now summarized here.

1. The inverter was found to be practically immune to ac side faults, and would operate satisfactorily even for a complete voltage collapse.
2. The ac harmonics were found to be of the same order of magnitude as in the naturally commutated inverter, and were observed to be fairly independent of the operating dc current.
3. The dc harmonics were found to be higher than in the naturally commutated counterpart. The high 24^{th} harmonic would need large filter requirements. For a small (to the order to 10% of the line's dc voltage) tap on the dc line, these harmonics would be small in comparison to the line's rated voltage.
4. The firing angle can be changed reasonably fast - in most cases within a cycle. Small changes, especially for operation around 180°, may be made instantaneously. The analysis also suggests the kind of information required to design a firing angle change controller for the inverter.

CHAPTER 4

INVERSION INTO WEAK SYSTEMS

4.1 Introduction

This chapter looks into the possibility of using the inverter to operate into a system of low short-circuit capacity, *i.e.*, a system with very little generation of its own, and a large (inductive) impedance. This could correspond, for example, to the case of an isolated tap on an HVDC line. A normal 3-phase bridge would be unable to operate into this system because of the lack of reactive power support, but a forced-commutated bridge might be able to do so. Therefore, to investigate this very attractive aspect, the inverter and a simplified load were simulated in a digital computer program. Results indicate that such operation is indeed possible.

The simulation programs include a program for steady-state analysis, as well as one concerned with the important problem of start-up. The report discusses a start-up strategy and demonstrates that it does work.

The programs used are based on the basic program developed in Chapter 2, and fully utilize the available options of selectable sources and selectable modes of solution (transient/steady-state).

The study is, of course, meant only to be indicative. The load representation is simple and does not include the effect of filters and overvoltage protection equipment that would inevitably exist in any actual installation. Even so, the results derived are encouraging and show that the problem is worth looking into in more detail.

4.2 System Representation

The choice of an adequate representation for a weak ac system is a difficult one. Firstly, the results obtained from such a representation should conform to the large number of possible weak systems. Secondly, it should be simple enough to be used with ease. Therefore, for lack of anything better, the circuit of Fig. 4.2.1 is used for representation purposes. This is the usual practice today [10]. It is a Thevenin representation, with the Thevenin impedance as two equal inductors in series with a resistor across one of them. The values are chosen so as to give appropriate SCR, and a phase angle of 75° - 85°. In this study, the angle has been chosen to be 80°, the SCR to be 2 p.u. The resulting component values are then ℓ = 0.33 p.u., r = 0.9 p.u. Assuming a rated

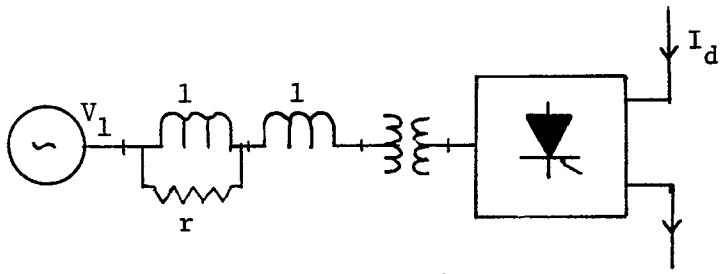


FIG 4.2.1 : THE WEAK SYSTEM

voltage of 10% of the ac voltage of the major converter of the system, these values would then be ℓ = 0.033 p.u., r = 0.09 p.u.

4.3 The Computer Model

As the basic program developed in Chapter 2 requires a 'source' voltage, it is required to treat the circuit in Fig. 4.2.1 as an ideal voltage source. This is done in the following manner.

1. The inductance in series with the transformer is lumped together with the transformer inductance.
2. The voltage that is now required is the one marked V_s in Fig. 4.3.1. The currents are as marked in the figure. i is the current in the

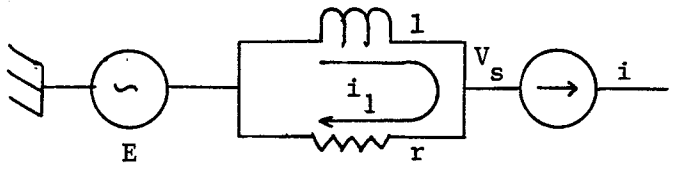


FIG 4.3.1 : VOLTAGE TO BE SOLVED FOR

phase when it is in conduction. Thus:

$i = I_d$ during the constant charge phase.

and $i = 0$ when the phase is not conducting.

Thus except during commutation, i is a constant.

The relevant loop equation is

$$\frac{di_1}{dt} = (i - i_1)\frac{r}{\ell} \tag{1}$$

As i is a constant except during commutations, (1) can be solved to give

$$i_1 = (1 - e^{(-rt/\ell)})i \tag{2}$$

During the commutation interval (1) may be rewritten as

$$di_1 = \frac{r}{\ell}(i - i_1)dt \tag{3}$$

where dt is the time step involved in a numerical solution. Assuming that dt is sufficiently small, i may be assumed essentially constant during each step. Thus Equ. (3) yields approximately the same solution as Equ. (2) and in general, therefore

$$i_1 = (1 - e^{-rt/\ell})i \tag{4}$$

where the origin for t is taken as the instant when i is known. The voltage required, V_s, is then given by

$$V_s = (i_1 - i)\,r + E \tag{5}$$

Note that the routine to solve for V_s also updates the value of i_1 through equation (4). Hence, even when V_s is not required in the main program, this routine must be called when any 'time' elapses in the simulation, just to keep the source currents right.

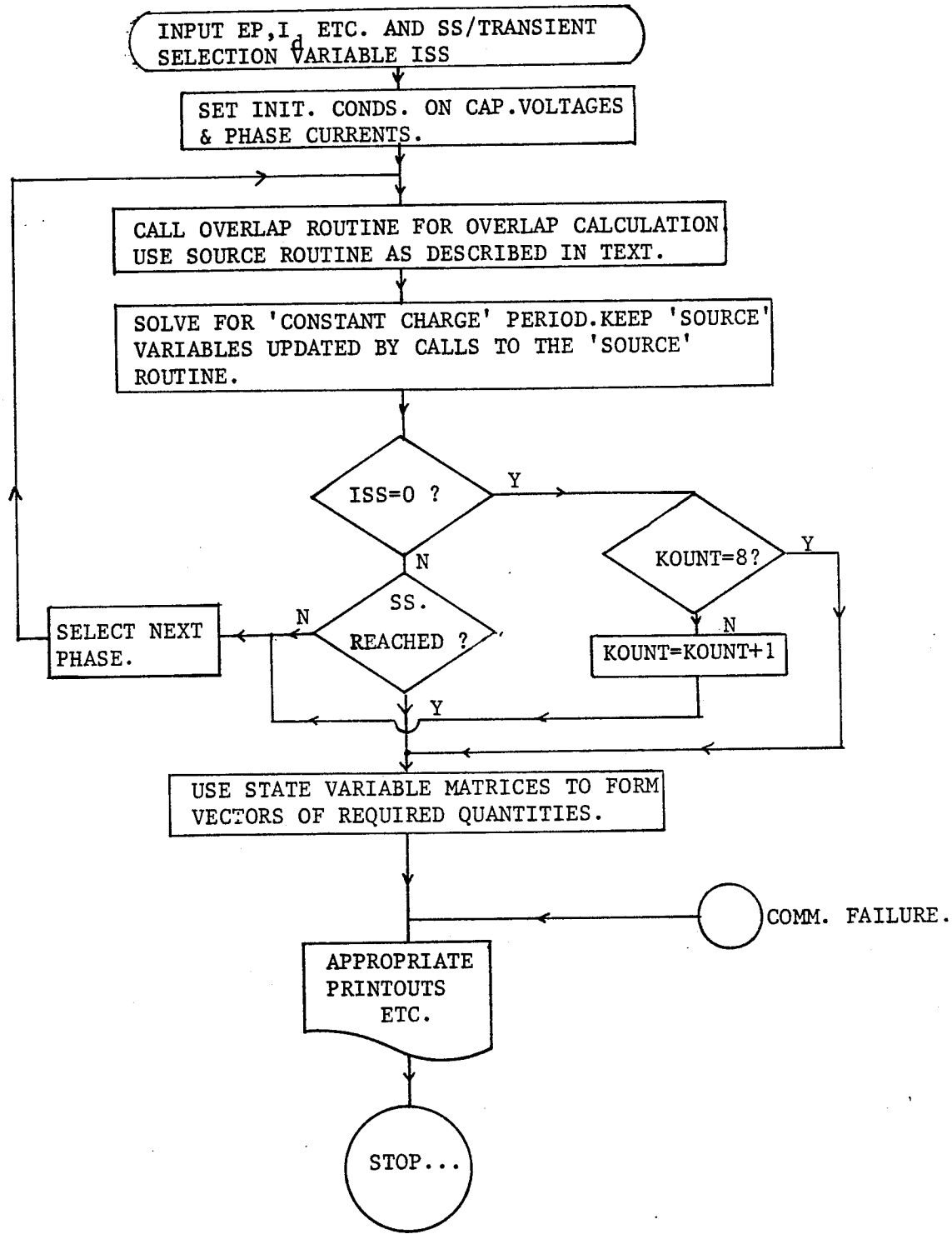


FIG 4.3.2 : FLOWCHART FOR INVERSION INTO WEAK SYSTEMS

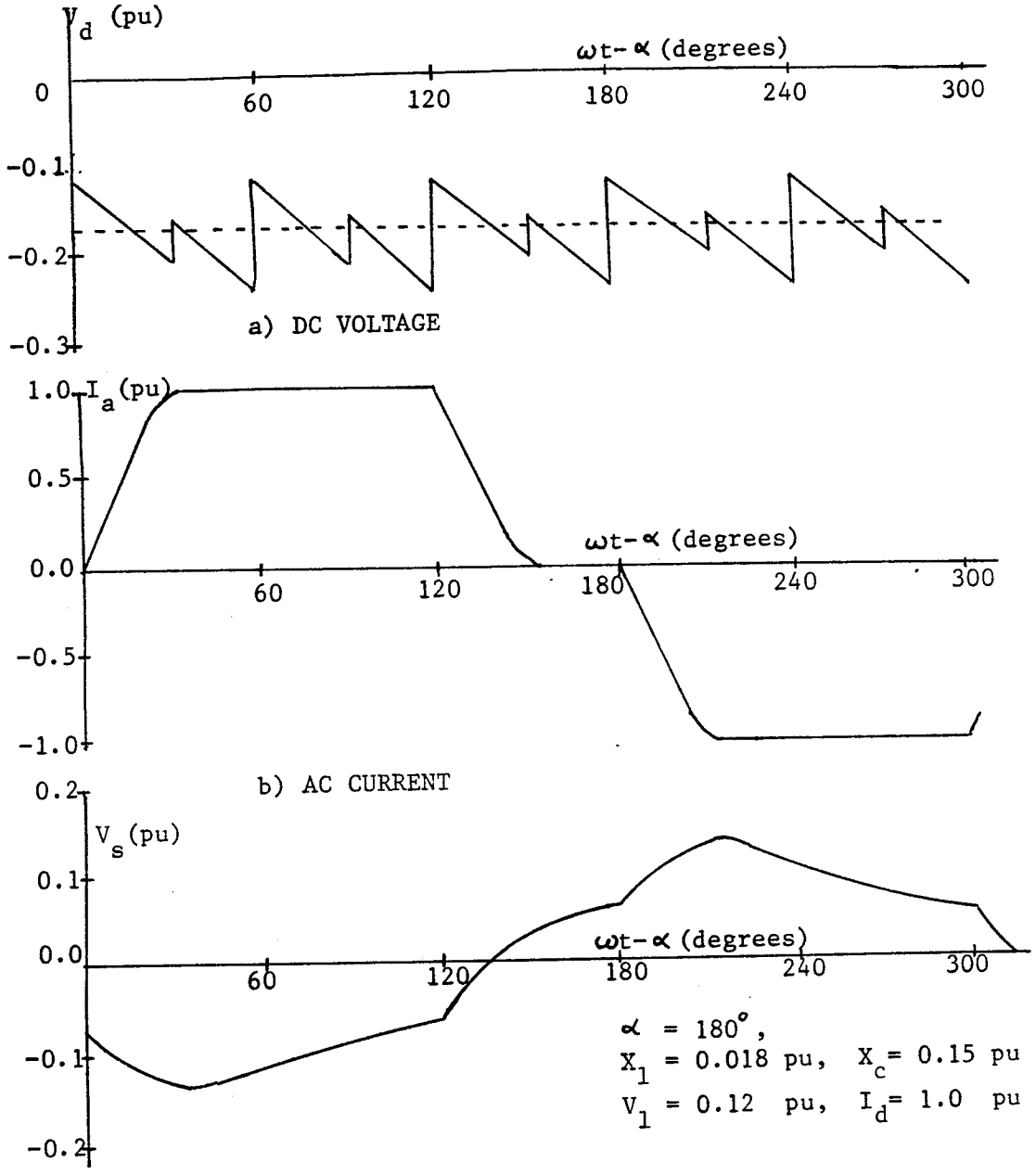
The program, as flowcharted in Fig. 4.3.2 is very similar to the basic program of Chapter 2, and differs mainly in the way the source voltages are calculated. Equations (4) and (5) are used in the source voltage calculations. Some amount of bookkeeping is also required to insert the proper initial phase current i_1 for each of the phases during the 'source' calculations.

4.4 Results of the Study

It was observed that steady-state operation for $\alpha = 180°$ was possible over a wide range of dc currents (with $X_c = 0.15$ p.u., $X_L = 0.018$ p.u.) - right from 0.4 p.u. to 1.4 p.u. For lower currents (right up to 0.1 p.u.), operation was possible with some voltage support from the supply. Thus the system could operate at $I_d = 0.1$ p.u. with a firing angle $\alpha = 160°$.

The waveforms obtained for operation at rated conditions ($V_L = 0.12$ p.u., $I_d = 1.0$ p.u., $\alpha = 180°$) are shown in Fig. 4.4.1, which shows (a) dc voltage, (b) ac current and (c) the voltage V_s discussed in Section 4.3.

Particularly noticeable is the high overlap angle (about 30°). In a normal Graetz Bridge operating in the vicinity of a 180° firing angle, such a large value of overlap angle would mean commutation failure. But for the forced-commutated inverter which derives its commutation voltage from its own capacitors and not from the supply, this is not the case. This high overlap angle though undesirable from the point of view of maximum utilization of the thyristors, nevertheless means lower di/dt stresses and the smoother waveforms probably have a lower harmonic content. Also, the dc voltage waveform is less jagged than it would have been for a lower value of overlap angle, and thus it too, has a lower harmonic content.



c) V_s AS OUTPUT BY THE SOURCE ROUTINE.

FIG 4.4.1 : INVERTER WAVEFORMS FOR OPERATION INTO THE WEAK SYSTEM

4.5 Investigations Into Start-up

The inverter described in this chapter would probably be used as a tap on an HVDC line used to invert into a weak system. Such a tap should be able to operate without affecting the main system. It should be possible, therefore, to start the tapped inverter even when the dc line is carrying the full (1 p.u.) dc current. This is unlike the case of a point to point transmission scheme in which the system can be started with zero current, and the current can then gradually be built up to its rated value.

Figure 4.5.1 shows a possible scheme to do this. The sequence of events is now described:

1. At $t < 0$, switch S_0 is in the closed state and carrying full dc current.
2. At $t = 0$ S_1 and S_2 are now closed, T_1 and T_2 pulsed, and S_0 opened.

   Note that it is possible to open S_0 because an alternate current path has been created. The inductance in the circuit has been shorted out, and the voltage across S_0 is the voltage across C_a and C_c, which is zero at $t = 0$, and increases linearly with time (constant current charging).
3. When C_a is charged to a sufficient voltage, T_3 is fired and takes over from T_1, because of the voltage on C_a.
4. When commutation is complete, S_1 is opened. Note that it can be opened extremely fast because it is carrying zero current (dead switch).
5. Likewise, T_4 is fired to take over from T_2 and S_2 opened after the current through it has fallen to zero.

Normal operation continues hereafter. Note that S_1 and S_2 are dead only for about 1/6 cycle (3 ms) and must be opened within that time otherwise the phase would come into conduction again. This time can be doubled by using a diode in series with the switch. The diodes used could be lossy because their purpose is to prevent a current through S_1 (S_2) when T_4 (T_5) conducts. This gives a time of about 6 ms which should be enough to open a dead switch.

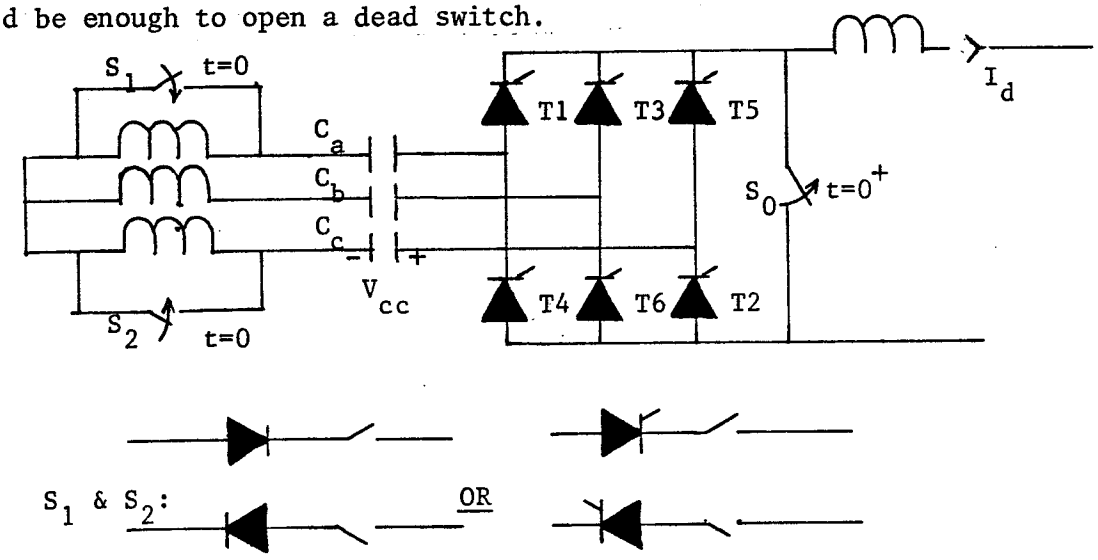


FIG 4.5.1 : STARTUP OF INVERTER

The above time can be increased somewhat, depending on the permissible overvoltage allowed on the capacitors. This time can of course be increased indefinitely if thyristors are used instead of switches, but this would increase the cost of the inverter.

At this point a few comments are in order.

a) It is important to notice that only dead switches are being opened. It would be impossible to open a current carrying switch in as short a period as 6 ms, but it may be possible to open a dead switch (as opposed to a circuit breaker) in that time. In fact, the order of time required would be that of closing a circuit breaker (not opening it), which could well be in the order of a few ms.

b) It appears that the transformer phases are being shorted during the start-up sequence. This is true, however it should be remembered that the system is weak and has a very low short circuit capacity - in fact it could well be a dead load. The resulting short circuit currents are, therefore, of small magnitude and could be tolerated, especially since the switches are closed for an extremely short period. Also, such a tap would probably be the major supplier of power to its ac system and the system would be dead anyway when the tap is inoperational.

The Program

To see whether start-up as described above is actually possible, a simulation using the program developed in Section 4.3 is carried out. The flowchart is given in Fig. 4.5.2. The only modifications to the program of Section 4.3 are:

1) The variable ICOM counts the number of commutations.
2) For ICOM = 1 or 2, the commutation inductance ℓ is reduced to account for the shorted inductance in one of the phases. Also, the appropriate source voltages and inductor currents are maintained at zero - representing this shorted phase.
3) Normal operation continues after the second commutation (ICOM $\geq$ 3). The inductance is reset back to its original value, and the source calculations proceed as in the program of Section 4.3, until the system either converges or fails due to commutation failure.

As in previous programs, the steady-state/transient selection variable ISS can be set to zero to observe the capacitor waveforms over the first 10 commutation intervals.

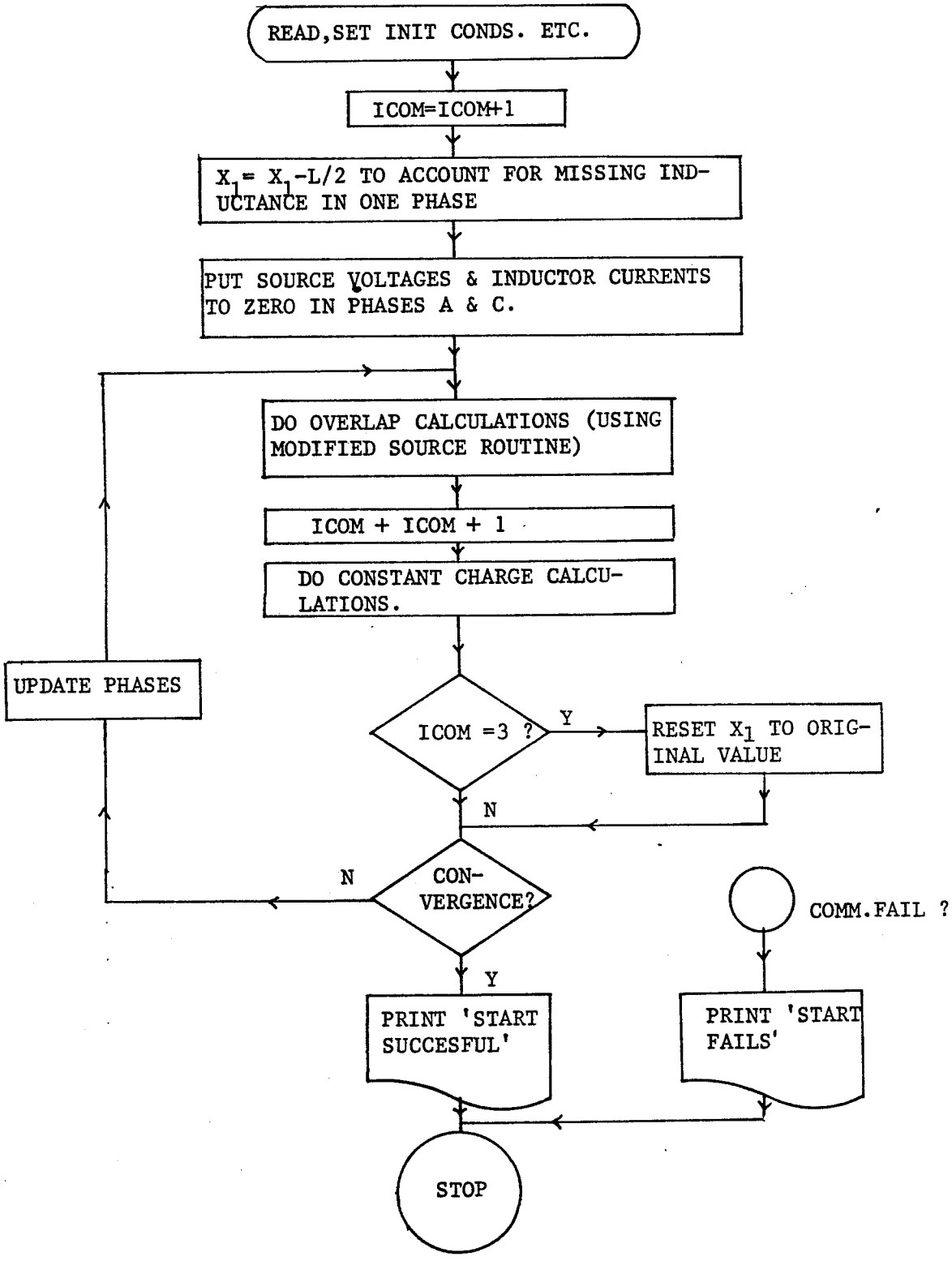


FIG 4.5.2 : FLOWCHART FOR STARTUP INTO WEAK SYSTEM

Results

Start-up simulations were carried out for the cases where

a) The weak system was completely dead - *i.e.*, without any generation.

b) With the Thevenin voltage behind the weak system impedance (see Fig. 4.2.1) as 0.12 p.u.

In the first case (a) it was observed that start-up was possible over the entire current range (I_d = 0.1 p.u. to 1.4 p.u.). For the case (b) however, start-up was possible only with some voltage support from the ac system (*i.e.*, by starting operation at $\alpha < 180°$). It was observed that at lower values of currents, start-up was easier than at higher values. Table 4.5.1 shows the required firing angle and initial capacitor voltage for start-up. It was found that for starting at I_d around 1.0 p.u., the initial voltage on the capacitors was of critical importance, and a voltage larger or a little smaller than that in Table 4.5.1 would cause commutation failure.

I_d (p.u.)	Maximum allowed value for α for successful start	Initial Voltage on Capacitors (if critical) (pu)
1.4	$\leq 120°$	0.12
1.2	$\leq 120°$	0.11
1.0	$\leq 120°$	0.10
0.8	$\leq 120°$	0.09
0.6 - 0.1	$\leq 130°$	Not critical

TABLE 4.5.1 RESULTS OF START-UP TESTS

The capacitor waveforms at start-up are shown in Fig. 4.5.3. The waveforms correspond to start-up on 1 p.u. dc current, 0.12 p.u. ac voltage (12% tap) and a firing angle of 120°. Once the system starts up, the firing angle may quickly be changed to the desired one, which in most cases would be in the neighbourhood of 180°.

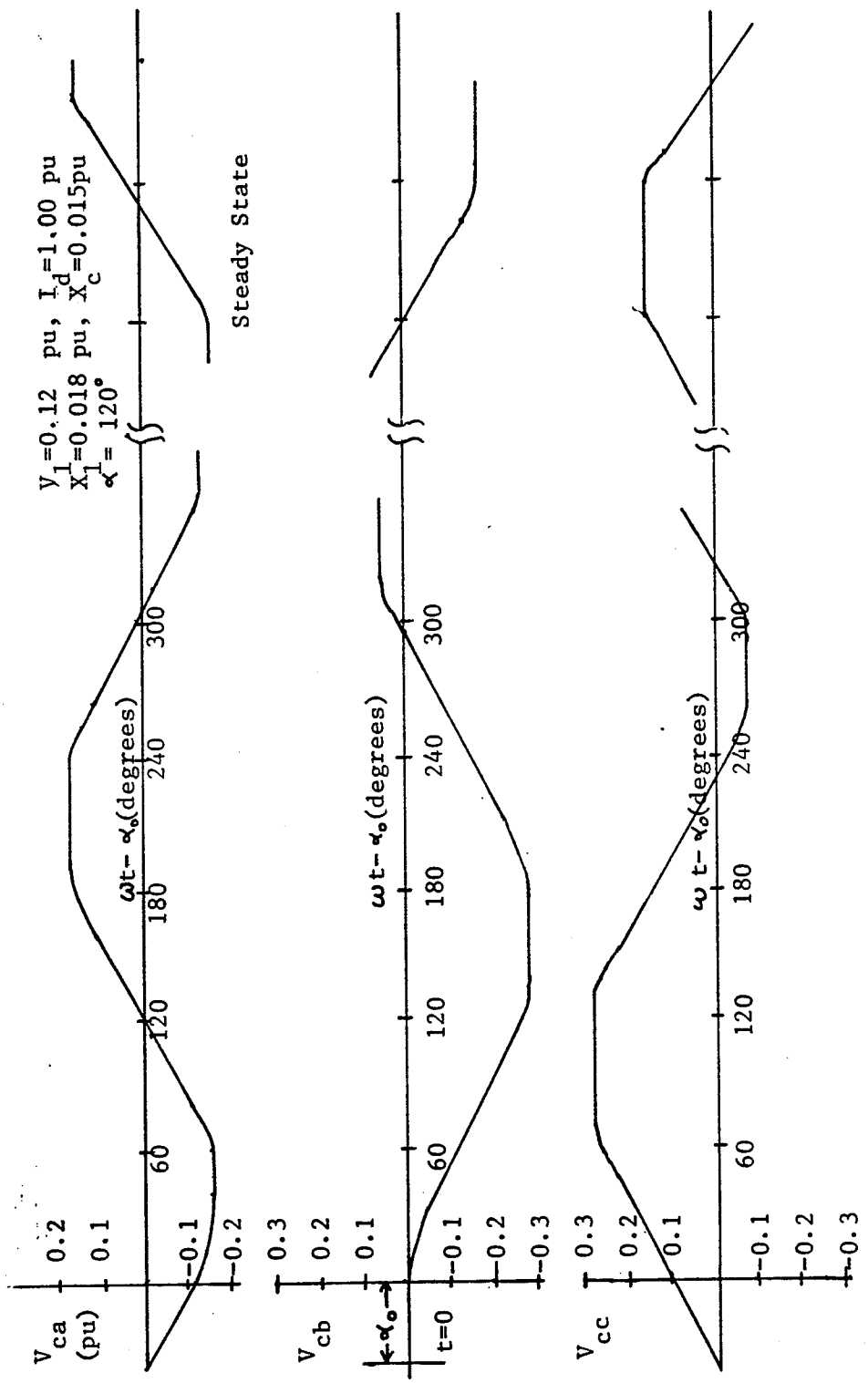


FIG 4.5.3 : CAPACITOR WAVEFORMS AT STARTUP

4.6 Conclusions

1. The inverter can operate over a wide range of currents, into a weak ac system.
2. Start-up over a wide range of currents is possible with some voltage support from the ac system.
3. It is more difficult to start the inverter at higher dc currents. A lower value of α is required, and the first charging of the capacitors is critical. Thus, a controller which determines when to fire T_1 and T_2 for the first time must have this information.
4. A number of simplifications have been made in the representation of the load. An actual system, designed with filters and other circuits on the ac side, would have a somewhat different behaviour from the simplified system. Thus the numerical results of Table 4.5.1 and of Figs. 4.4.1 and 4.5.3 are meant only to be indicative.

The flowcharts given here are meant to explain the general concept only. For detailed flowcharts, program linkings and so on, the reader is referred to the technical report [11] which deals with these.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

Listed here are the important conclusions of the thesis, and recommendations for carrying on from where this project ends.

5.1 Conclusions

1. The hybrid state-equation, direct solution approach to analyzing the inverter operation is effective in studying a wide range of operating conditions. It allows an extension of previous steady-state studies to transient studies and generalized source representations. The direct solution part of it means a saving of time and memory on the digital computer.

2. The forced-commutated inverter produces rather large harmonics in its dc voltage. This may be a problem if it is used as a major converter.

3. The inverter is immune to ac side faults. A discussion of converter faults and some dc side faults has been carried out by Reeves et al [5], and the effect of these faults does not appear to be catastrophic. Thus, the inverter's behaviour under faults seems to be quite reasonable.

4. The immunity to ac side faults (and ac voltage uncertainties in general) make it suitable for operation into weak systems, where due to the lack of large amounts of generation, there could be some amount of fluctuation of ac voltage in the system.

5. An investigation of operation into weak system shows that such operation is possible over a wide range of operating conditions. At rated conditions, no reactive power support from the ac system is required. In fact a reactive power demand can be met.

It appears that the inverter can be started up when carrying full load current; using the strategy discussed in Section 4.5. In general, some amount of voltage support from the ac system is indicated when inverting into a system with generation. Start-up into a dead load is also possible over the entire dc current range.

5.2 Recommendations

1. A more detailed quantitive study of the operation should be carried out. For this more complete modelling of the inverter is necessary. This would consist of inclusion of filters and protection equipment, the effect of ferroresonance in the transformer, and so on. Also, when studying weak systems, more detailed representation should be used.

2. An economic analysis should be performed to assess the practicality of such a scheme. Even if the scheme is found to be uneconomical at the present time, lowering semiconductor costs and progress in technology could make it viable at a later date.

3. The inverter and the entire system should be evaluated from the point of view of reliability.

4. Construction of a real time simulator with a microprocessor based controller with which:
   a) System operation for various configurations may be studied.
   b) Operating strategies developed through the digital computer simulation may be programmed and tested.

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