# Analysis of Clock-Jitter Effects in Continuous-Time $\Delta\Sigma$ Modulators Using Discrete-Time Models

Philip M. Chopp and Anas A. Hamoui

***Abstract*—This paper proposes a simple discrete-time (DT) modeling technique for the rapid, yet accurate, simulation of the effect of clock jitter on the performance of continuous-time (CT) $\Delta\Sigma$ modulators. The proposed DT modeling technique is derived from the impulse-invariant transform and is applicable to arbitrary-order lowpass and bandpass CT $\Delta\Sigma$ modulators, with single-bit or multibit feedback digital-to-analog converters (DACs) employing delayed return-to-zero (RZ) or non-return-to-zero (NRZ) rectangular pulses. Its accuracy is independent of both the power spectrum of the clock jitter and the loop transfer function of the $\Delta\Sigma$ modulator.**

**The proposed DT modeling technique is validated (for both independent and accumulated clock-jitter errors) against accurate simulations in SIMULINK, using behavioral blocks developed to directly simulate RZ or NRZ DACs with clock jitter. It is subsequently applied to various CT $\Delta\Sigma$ modulator architectures (lowpass and bandpass, with single-bit and multibit DACs) to study the relative effectiveness of different feedback-DAC pulsing schemes (NRZ, RZ, RZ with fixed on-time, and RZ with fixed off-time) in minimizing the modulator sensitivity to clock jitter. The performance of each architecture is compared as a function of clock jitter, thereby offering a valuable reference for selecting a rectangular feedback-DAC pulse shape when designing CT $\Delta\Sigma$ analog-to-digital converters.**

***Index Terms*—Analog-to-digital (A/D) conversion, behavioral modeling, clock jitter, continuous-time (CT), impulse-invariant transform, sigma-delta ($\Sigma\Delta$) modulation.**

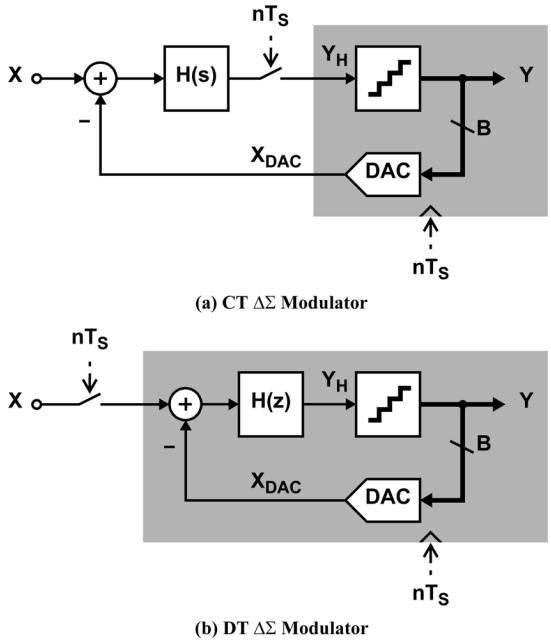


Fig. 1. Block diagrams of (a) a CT $\Delta\Sigma$ modulator and (b) a DT $\Delta\Sigma$ modulator.

## I. Introduction

CONTINUOUS-TIME (CT) $\Delta\Sigma$ modulators [Fig. 1(a)] benefit from a number of architectural advantages over their discrete-time (DT) counterparts [Fig. 1(b)]. These include a greater potential for low-power and high-speed operation and an inherent suppression of aliasing and sampling errors [1], [2]. The principal disadvantage of CT $\Delta\Sigma$ modulators is their high sensitivity to clock jitter [3]–[6]. Clock jitter introduces errors into: 1) the forward path, as *sampling errors* at the quantizer input and 2) the feedback path, as *time-delay errors* in the output pulses of the feedback digital-to-analog converter (DAC). Sampling errors are subject to the same noise shaping as quantization errors and, therefore, do not affect the system performance. However, time-delay errors (which are added directly to the input signal by the feedback DAC) are not suppressed by the $\Delta\Sigma$ loop and, hence, can significantly reduce the achievable performance of a CT $\Delta\Sigma$ modulator.

This paper proposes a simple DT modeling technique for the rapid, yet accurate, simulation of the effect of the time-delay errors that are generated in the feedback path of a CT $\Delta\Sigma$ modulator due to clock jitter. The proposed DT modeling technique is based on the impulse-invariant transform, which is a standard method for translating the frequency response of a CT filter into an equivalent DT representation [7]. This transform has proven to be a useful design technique for CT $\Delta\Sigma$ modulators [5], [8], allowing designers to take advantage of the numerous tools available for designing DT $\Delta\Sigma$ modulators.

The proposed DT modeling technique provides a high degree of flexibility, as its accuracy is independent of: 1) the order and noise-shaping characteristics (lowpass or bandpass) of the $\Delta\Sigma$ modulator; 2) the pulsing scheme (RZ or NRZ) and number of bits in the feedback DAC; and 3) the power spectrum of the clock jitter.

This paper also develops DAC behavioral blocks to accurately simulate the effect of clock jitter on the feedback-DAC pulses of a CT $\Delta\Sigma$ modulator, using the SIMULINK tool. These blocks, developed for DACs with delayed return-to-zero (RZ) or non-return-to-zero (NRZ) rectangular pulses, accurately simulate the

Manuscript received February 20, 2008; revised June 15, 2008. First published October 31, 2008; current version published June 19, 2009. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada and the Fonds Québécois de la Recherche sur la Nature et les Technologies. This paper was recommended by Associate Editor H. Schmid.

The authors are with the Department of Electrical and Computer, Engineering, McGill University, Montreal, QC H3A 2A7, Canada (e-mail: anas.hamoui@mcgill.ca).

Digital Object Identifier 10.1109/TCSI.2008.2008501

effect of clock jitter by directly generating time-delay errors according to a specified jitter spectrum. In this paper, these DAC behavioral blocks are used to confirm the accuracy of the proposed DT modeling technique.

Previously published work has analyzed the effect of clock jitter on either single-bit lowpass [3] or single-bit bandpass [4] CT $\Delta\Sigma$ modulators, employing RZ or NRZ feedback-DAC pulses, or multibit lowpass [9] CT $\Delta\Sigma$ modulators, employing NRZ feedback-DAC pulses. Reduced clock-jitter sensitivity has been demonstrated in CT $\Delta\Sigma$ modulators that employ RZ feedback-DAC pulses with a fixed on-time [10] or that utilize a switched-capacitor-resistor (SCR) feedback DAC [5].

In this paper, the proposed DT modeling technique is applied to analyze the effect of clock jitter on both single-bit and multibit configurations of bandpass and lowpass CT $\Delta\Sigma$ modulators, including high-order architectures with optimally spread noise-transfer-function (NTF) zeros. Four types of delayed rectangular feedback-DAC pulses are considered: 1) standard NRZ; 2) standard RZ; 3) RZ with a fixed on-time duration; and 4) RZ with a fixed off-time duration.

This paper is structured as follows. The proposed DT technique for clock-jitter modeling is described in Section II and its accuracy is demonstrated in Section III. The proposed DT modeling technique is then applied in Section IV to analyze the effect of clock jitter on various CT $\Delta\Sigma$ modulator architectures for different feedback-DAC pulsing schemes.

## II. Proposed DT Modeling Technique

The impulse-invariant transform of a CT loop filter $H(s)$ yields a DT loop filter $H(z)$ with an identical impulse response and, hence, equivalent noise-shaping characteristics [8]. This paper proposes using the impulse-invariant transform to map the *time-delay errors* due to clock jitter in the feedback-DAC pulses of a CT $\Delta\Sigma$ modulator [Fig. 1(a)] into *coefficient errors* in the loop transfer function $H(z)$ of an equivalent DT $\Delta\Sigma$ modulator [Fig. 1(b)]. This is made possible by the fact that both the start and end times of the rectangular pulses, generated by the feedback DAC of the CT $\Delta\Sigma$ modulator, are available as parameters in the impulse-invariant transform.

Consider a feedback DAC that generates rectangular pulses of the types illustrated in Fig. 2. Here, $\alpha$ represents the time delay between the start of the sampling period and the rising edge of the DAC pulse, whereas $\beta$ represents the time delay between the start of the sampling period and the falling edge of the DAC pulse [8]. Time references $\alpha$ and $\beta$ are normalized with respect to the sampling-clock period $T_S$. Ideally

$$\beta < 1 + \alpha, \qquad \text{for RZ pulses} \tag{1}$$
$$\beta = 1 + \alpha, \qquad \text{for NRZ pulses.} \tag{2}$$

Furthermore, an ideal NRZ pulse incorporating an excess loop delay of $\tau_d$ has $\alpha = \tau_d/T_S$. Using this notation, clock jitter can be represented as an additive timing error on the *nominal* edges $\alpha$ and $\beta$ of the rectangular DAC pulses as

$$\hat{\alpha}(n) \equiv \alpha + \Delta\alpha(n) \qquad \hat{\beta}(n) \equiv \beta + \Delta\beta(n) \tag{3}$$

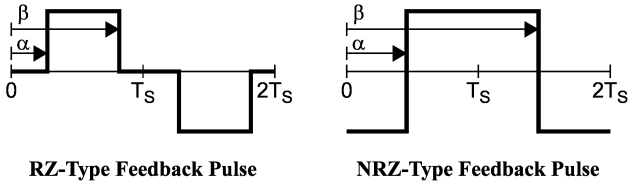


Fig. 2. Timing of the delayed rectangular pulses generated by the feedback DAC of a CT $\Delta\Sigma$ modulator. Here, $T_S$ is the sampling clock period.

where $\hat{\alpha}$ and $\hat{\beta}$ represent the timing of the *jittered* edges of the rectangular DAC pulse, while time-delay errors $\Delta\alpha$ and $\Delta\beta$ depend on the power spectrum of the clock jitter. Here, it is assumed that

$$\hat{\alpha}(n) > \hat{\beta}(n-1) - 1, \qquad \text{for RZ pulses} \tag{4}$$
$$\hat{\alpha}(n) = \hat{\beta}(n-1) - 1, \qquad \text{for NRZ pulses.} \tag{5}$$

In subsequent discussions, time index $n$ (which specifies time $t = nT_S$) will be dropped for simplicity.

To model CT timing errors in the DT domain, the proposed DT modeling technique develops a series of $z$-domain error-mapping terms, which translate the *time-delay errors* $\Delta\alpha$ and $\Delta\beta$ in the feedback-DAC pulses of a CT $\Delta\Sigma$ modulator into *coefficient errors* in the loop transfer function of an equivalent DT $\Delta\Sigma$ modulator. In the following, the second-order error-mapping term is derived.

### A. Derivation of the Second-Order Error-Mapping Term

Consider a DT loop transfer function $H(z)$. To develop its equivalent CT loop transfer function $H(s)$ using the impulse-invariant transform, the first step is to split $H(z)$ into its constituent terms by way of a partial fraction expansion. An example of a second-order term that can result from such an expansion is

$$H_2(z) = \frac{k_2}{(z-1)^2}. \tag{6}$$

If $\alpha$ and $\beta$ represent the start and end times of the feedback-DAC pulses (Fig. 2), then $H_2(z)$ in (6) can be transformed into the CT domain using a $z \rightarrow s$ impulse-invariant transform with *nominal* pulse-edge timing $\alpha$ and $\beta$, as

$$H_2(s) = \frac{r_1(sT_S) + r_2}{(sT_S)^2} \tag{7}$$

where

$$r_1 = (1/2)k_2((\alpha + \beta - 2)/(\beta - \alpha))$$
$$r_2 = k_2(1/(\beta - \alpha))$$

The objective here is to modify the *nominal* loop transfer function $H_2(z)$, such that the loop response of the DT $\Delta\Sigma$ modulator is identical to the loop response of its equivalent CT $\Delta\Sigma$ modulator, when the feedback-DAC pulses of the CT $\Delta\Sigma$ modulator are degraded by time-delay errors due to clock jitter.

Assume that the $\alpha$ and $\beta$ edges of the rectangular feedback-DAC pulses are perturbed by time-delay errors $\Delta\alpha$ and $\Delta\beta$, as per (3). Then, $H_2(s)$ in (7) can be transformed back into

TABLE I
ERROR-MAPPING TERMS FOR POLES AT $z = 1$

| Nominal term | Error-mapping term |
|---|---|
| $H_1(z) = \dfrac{k_1}{z-1}$ | $\widehat{H_1}(z) = \dfrac{k_1}{z-1} + \dfrac{\Delta k_{11}}{z-1}$<br>$\Delta k_{11} = k_1(\Delta\beta - \Delta\alpha)/(\beta - \alpha)$ |
| $H_2(z) = \dfrac{k_2}{(z-1)^2}$ | $\widehat{H_2}(z) = \dfrac{k_2}{(z-1)^2} + \dfrac{\Delta k_{22}}{(z-1)^2} + \dfrac{\Delta k_{21}}{z-1}$<br>$\Delta k_{22} = k_2(\Delta\beta - \Delta\alpha)/(\beta - \alpha)$<br>$\Delta k_{21} = -(1/2)k_2(\Delta\alpha + \Delta\beta)$ |
| $H_3(z) = \dfrac{k_3}{(z-1)^3}$ | $\widehat{H_3}(z) = \dfrac{k_3}{(z-1)^3} + \dfrac{\Delta k_{33}}{(z-1)^3} + \dfrac{\Delta k_{32}}{(z-1)^2} + \dfrac{\Delta k_{31}}{z-1}$<br>$\Delta k_{33} = k_3(\Delta\beta - \Delta\alpha)/(\beta - \alpha)$<br>$\Delta k_{32} = -(1/2)k_3(\Delta\alpha + \Delta\beta)$<br>$\Delta k_{31} = (1/12)k_3[(\beta - \alpha)(\Delta\beta - \Delta\alpha) + 3(\Delta\alpha + \Delta\beta)]$ |

TABLE II
ERROR-MAPPING TERMS FOR POLES AT $z = z_p$

| Nominal term | Error-mapping term |
|---|---|
| $H_{p1}(z) = \dfrac{k_{p1}}{z - z_p}$ | $\widehat{H_{p1}}(z) = \dfrac{\delta k_{p1}}{z - z_p}$<br>$\delta k_{p1} = k_{p1}(z_p^{\beta-\Delta\alpha} - z_p^{\alpha-\Delta\beta})/(z_p^{\beta} - z_p^{\alpha})$ |
| $H_{p2}(z) = \dfrac{k_{p2}}{z - z_p} + \dfrac{k_{p2}^*}{z - z_p^*}$<br>$= \dfrac{k_{p21}z - k_{p22}}{z^2 - 2Re\{z_p\}z + 1}$ | $\widehat{H_{p2}}(z) = \dfrac{\delta k_{p21}z - \delta k_{p22}}{z^2 - 2Re\{z_p\}z + 1}$<br>$k_{p2} = (k_{p22} - k_{p21}z_p)/(z_p^* - z_p)$<br>$\delta k_{p2} = k_{p2}(z_p^{\beta-\Delta\alpha} - z_p^{\alpha-\Delta\beta})/(z_p^{\beta} - z_p^{\alpha})$<br>$\delta k_{p21} = 2Re\{\delta k_{p2}\}$<br>$\delta k_{p22} = 2Re\{\delta k_{p2}z_p^*\}$ |

the DT domain using an $s \rightarrow z$ impulse-invariant transform with *jittered* pulse-edge timing $\hat{\alpha}$ and $\hat{\beta}$ as

$$\hat{H}_2(z) = \frac{c_1}{(z-1)} + \frac{c_2 z + c_3}{(z-1)^2} \tag{8}$$

where

$$\begin{aligned} c_1 &= r_1(\hat{\beta} - \hat{\alpha}) \\ c_2 &= (1/2)r_2[\hat{\beta}(2 - \hat{\beta}) - \hat{\alpha}(2 - \hat{\alpha})] \\ c_3 &= (1/2)r_2(\hat{\beta}^2 - \hat{\alpha}^2) \end{aligned}$$

The expression for $\hat{H}_2(z)$ in (8) can be rewritten as

$$\hat{H}_2(z) = \frac{k_2}{(z-1)^2} + \frac{\Delta k_{22}}{(z-1)^2} + \frac{\Delta k_{21}}{(z-1)} \tag{9}$$

where $k_2$ is the coefficient of $H_2(z)$ in (6), while $\Delta k_{21}$ and $\Delta k_{22}$ are jitter-induced coefficient errors defined in Table I. Observe that the first term of the *jittered* transfer function $\hat{H}_2(z)$ in (9) is equal to the *nominal* transfer function $H_2(z)$ in (6). The second and third terms represent errors introduced by time-delay errors $\Delta\alpha$ and $\Delta\beta$ due to clock jitter. Therefore, $\hat{H}_2(z)$ in (9) maps time-delay errors, generated in the feedback-DAC pulses of the CT $\Delta\Sigma$ modulator, into coefficient errors in the loop transfer function of an equivalent DT $\Delta\Sigma$ modulator, which was the stated objective.

The above DT modeling technique can be explained intuitively as follows. Using the *nominal* pulse-edge timing $\alpha$ and $\beta$ in the $z \rightarrow s$ impulse-invariant transform reflects the nominal design procedure, as in (7). Subsequent introduction of jitter-induced time-delay errors $\Delta\alpha$ and $\Delta\beta$ in the feedback-DAC pulses creates a mismatch between the CT loop transfer function $H_2(s)$ and its equivalent DT loop transfer function $H_2(z)$. This mismatch can be modeled in the DT domain by performing an $s \rightarrow z$ impulse-invariant transform using the *jittered* clock-edge timing $\hat{\alpha}$ and $\hat{\beta}$, as in (8).

Observe that the above simplified derivation may not appear to be formally correct, as it seemingly involves taking the Laplace and $Z$ transforms of a time-varying impulse response, yet this simplified approach produces correct results, since the time-varying terms $\Delta\alpha(n)$ and $\Delta\beta(n)$ can be shifted from the impulse response to the input of the loop filter $\hat{H}(z)$ and, hence, are not actually processed by the Laplace and $Z$ transforms. This is demonstrated through a more rigorous derivation presented in Appendix I.

### B. DT Simulation of Clock-Jitter Errors in CT $\Delta\Sigma$ Modulators

Table I presents the error-mapping terms for modeling the effect of jitter-induced time-delay errors on first-, second-, and third-order terms of a loop transfer function with coincident poles at dc ($z = 1$). Table II presents the error-mapping terms for a first-order term with a general pole at $z = z_p$ and for a second-order term with complex-conjugate poles at $z = z_p$ and $z = z_p^*$. It is assumed here that all poles of the loop transfer function (i.e., zeros of the NTF) are placed on the unit circle (i.e., $|z_p|^2 = 1$) for optimal noise-shaping performance [12]. All error-mapping terms were derived using the procedure described above.

The error-mapping terms presented in Tables I and II can be utilized for the DT simulation of the effect of time-delay errors (due to clock jitter) in the feedback path of a CT $\Delta\Sigma$ modulator, as follows.

1) If starting with a prototype DT loop transfer function $H(z)$ [Fig. 1(b)], perform a partial-fraction expansion of $H(z)$. If starting with a CT loop transfer function $H(s)$ [Fig. 1(a)], perform an $s \rightarrow z$ impulse-invariant transform to obtain the equivalent DT loop transfer function $H(z)$ and then perform a partial-fraction expansion of $H(z)$. Replace each term in the *nominal* function $H(z)$ with the corresponding error-mapping term in Table I or II to obtain the *jittered* function $\hat{H}(z)$.
2) Implement the loop transfer function $\hat{H}(z)$ in a DT $\Delta\Sigma$ modulator architecture and simulate it using a general-purpose simulator (e.g., SIMULINK).

Observe that, in a CT $\Delta\Sigma$ modulator, the time-delay errors generated by the DAC originate in the feedback path and, hence, do not affect the input-signal path. Therefore, for correspondence with the CT $\Delta\Sigma$ modulator, an $N$th-order error-mapping term $\hat{H}_N(z)$ or $\hat{H}_{pN}(z)$ in Table I or Table II must be implemented in an $N$th-order DT $\Delta\Sigma$ modulator architecture in such a way that the corresponding jitter-induced coefficient errors $\Delta k$ or factors $\delta k_p$ affect only the feedback-DAC path, and not

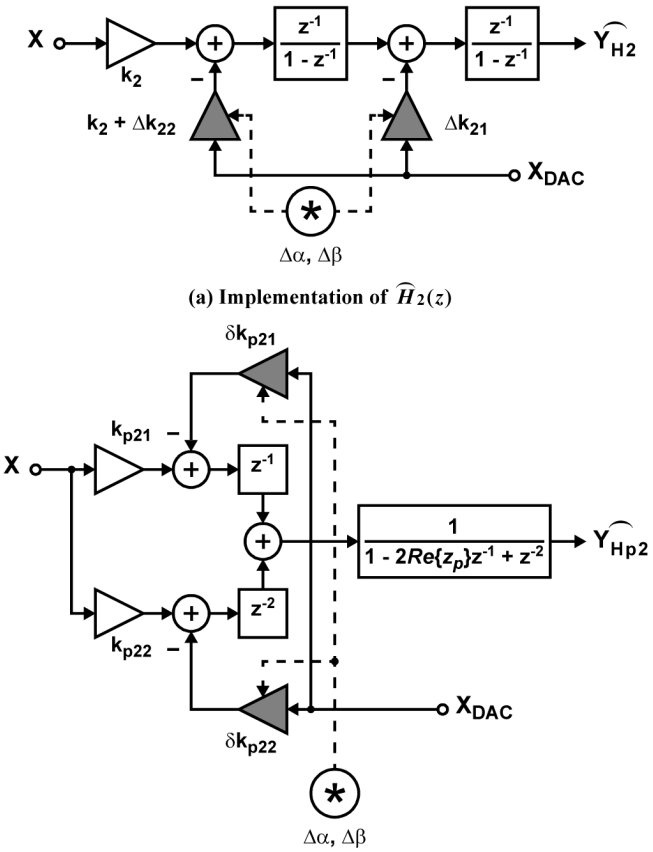


Fig. 3. Implementation of (a) error-mapping term $\hat{H}_2(z)$ in Table I and (b) error-mapping term $\hat{H}_{p2}(z)$ in Table II. The terminal names correspond to the DT $\Delta\Sigma$ modulator illustrated in Fig. 1(b).

the input-signal path. Fig. 3 illustrates such implementations for error-mapping terms $\hat{H}_2(z)$ and $\hat{H}_{p2}(z)$.

### C. Suppression of Jitter-Induced Errors by the $\Delta\Sigma$ Loop

Consider an $N$th-order term $H_N(z)$ with poles at $z = 1$ (dc). In the absence of clock jitter (i.e., when $\Delta\alpha = \Delta\beta = 0$), all jitter-induced coefficient errors $\Delta k_{Nm}$ $(m = 1, \ldots, N)$ in the corresponding error-mapping term $\hat{H}_N(z)$ in Table I reduce to zero. Therefore, in the implementation of $\hat{H}_N(z)$ and, equivalently, in the corresponding CT $\Delta\Sigma$ modulator, a jitter-induced coefficient error $\Delta k_{Nm}$ $(m = 1, \ldots, N)$ receives high-pass shaping of order $N - m$ from the $\Delta\Sigma$ loop. For example, in the implementation of $\hat{H}_2(z)$ in Fig. 3(a), error $\Delta k_{21}$ is first-order shaped, while error $\Delta k_{22}$ is not suppressed by the $\Delta\Sigma$ loop. Similarly, jitter-induced coefficient errors $\Delta k_{31}$ and $\Delta k_{32}$ in the error-mapping term $\hat{H}_3(z)$ receive second- and first-order high-pass shaping, respectively, while error $\Delta k_{33}$ is not suppressed by the $\Delta\Sigma$ loop.

Consider an $N$th-order term $H_{pN}(z)$ with poles at $z = z_p$. In the absence of clock jitter (i.e., when $\Delta\alpha = \Delta\beta = 0$), the jitter-induced coefficient factor $\delta k_{pN}$ of the corresponding error-mapping term $\hat{H}_{pN}(z)$ in Table II reduces to the nominal coefficient $k_{pN}$. Observe that, in Table II, the jitter-induced errors $\delta k_p$ are multiplicative (rather than additive, as for $\Delta k$ in Table I). Therefore, in the implementation of $\hat{H}_{pN}(z)$, the jitter-induced coefficient factors $\delta k_p$ are not shaped by the $\Delta\Sigma$ loop. For example, in the implementation of $\hat{H}_{p2}(z)$ in Fig. 3(b), the jitter-induced coefficient factors $\delta k_{p21}$ and $\delta k_{p22}$ are not suppressed by the $\Delta\Sigma$ loop.

The above observations become important when comparing the relative performance of various feedback-DAC pulsing schemes on lowpass versus bandpass $\Delta\Sigma$ modulators, as discussed in Section IV.

## III. Validation of DT Modeling Technique

To accurately simulate the effect of clock jitter on the RZ and NRZ feedback-DAC pulses of a CT $\Delta\Sigma$ modulator, a set of DAC behavioral blocks have been developed in SIMULINK, as described in Appendix II. These blocks are then utilized to validate the results generated by the proposed DT modeling technique.

Consider the CT $\Delta\Sigma$ modulator architectures listed in Table III. Fig. 4 provides block diagrams for standard configurations of the CT test architectures described in Table III, along with their equivalent DT realizations based on the proposed DT modeling technique. To evaluate the performance of the proposed DT modeling technique, the CT loop transfer functions of Architectures A and B were simulated in SIMULINK using:

1) a CT $\Delta\Sigma$ modulator, based on the developed feedback-DAC blocks (Appendix II);
2) an equivalent DT $\Delta\Sigma$ modulator, based on the proposed DT modeling technique (Section II).

This choice of test architectures (Table III) ensured that all error-mapping terms in Tables I and II were used at least once in the loop transfer functions. Two clock-jitter approximations were applied to each test architecture, as described below.

### A. Clock-Jitter Approximations

Clock jitter can be modeled as an additive timing error on the ideal clock edges, as described in (3) for delayed rectangular pulses. Under the *independent clock-jitter* approximation [3], the timing errors in (3) can be expressed as

$$\Delta\alpha(n) = \delta_\alpha(n) \text{ and } \Delta\beta(n) = \delta_\beta(n) \tag{10}$$

where $\delta_\alpha$ and $\delta_\beta$ are independent identically distributed (i.i.d.) zero-mean random variables, each following a Gaussian distribution with a standard deviation $\sigma_j$. This approximation results in a clock jitter with a white power spectrum.

Under the *accumulated* clock-jitter approximation (presented in [13] and applied in [3]) the timing errors in (3) are expressed as

$$\Delta\alpha(n) = \sum_{m=0}^{n} \delta_\alpha(m) \text{ and } \Delta\beta(n) = \sum_{m=0}^{n} \delta_\beta(m) \tag{11}$$

where $\delta_\alpha$ and $\delta_\beta$ are i.i.d. zero-mean random variables, each following a Gaussian distribution with a standard deviation $\sigma_{j,\text{eff}}$. The accumulated clock-jitter approximation results in a jitter power spectrum consisting of nonwhite skirts on either side of the clock signal tone, with each sideband power having a $1/f^2$ frequency dependence. This approximates the phase noise of a voltage-controlled oscillator (VCO) [14].

For timing errors $\Delta\alpha$ and $\Delta\beta$ to have the same standard deviation under both the accumulated and the independent jitter

TABLE III
TEST ARCHITECTURES FOR CT $\Delta\Sigma$ MODULATORS

| | Architecture | Loop transfer function | Placement of zeros in noise transfer function (NTF) |
|---|---|---|---|
| **A** | 3rd-Order Lowpass | $H_A(s) = \frac{r_3}{(sT_S)^3} + \frac{r_2}{(sT_S)^2} + \frac{r_1}{(sT_S)}$ | • 3 zeros at dc |
| **B** | 3rd-Order Lowpass | $H_B(s) = \frac{r_{21}(sT_S) + r_{22}}{(sT_S)^2 + s_p^2} + \frac{r_1}{(sT_S)}$ | • 1 zero at dc<br>• 1 pair of complex-conjugate zeros within the signal band $[0, f_{BW}]$ |
| **C** | 4th-Order Bandpass | $H_C(s) = \frac{r_{21a}(sT_S) + r_{22a}}{(sT_S)^2 + s_{pa}^2} + \frac{r_{21b}(sT_S) + r_{22b}}{(sT_S)^2 + s_{pb}^2}$ | • 1 pair of complex-conjugate zeros on either side of the center frequency $f_0$ |

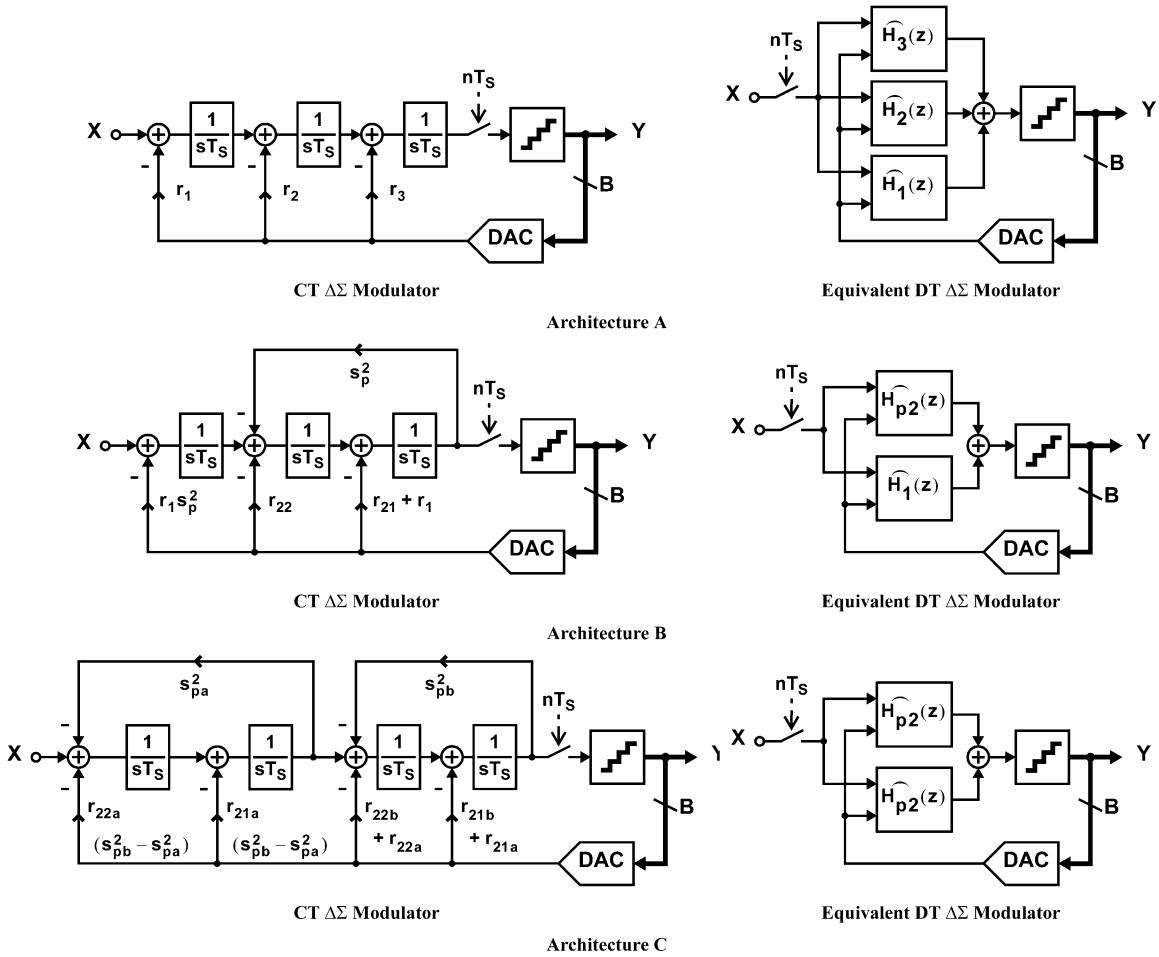


Fig. 4. Block diagrams for the CT $\Delta\Sigma$ modulator architectures listed in Table III, along with the equivalent DT realizations based on the proposed DT modeling technique. The DT $\Delta\Sigma$ modulators are composed of blocks similar to those in Fig. 3.

approximations, an *effective* clock jitter of $\sigma_{j,\text{eff}} = \sigma_j/\sqrt{N_{pts}}$ must be selected for the accumulated jitter, where $\sigma_j$ is the independent jitter and $N_{pts}$ is the number of simulation points.

### B. Accuracy of the DT Modeling Technique

The accuracy of the proposed DT modeling technique was validated based on the CT $\Delta\Sigma$ modulators with Architectures A and B in Table III, using both the independent and accumulated clock-jitter approximations. Architecture A was simulated for an oversampling ratio of $OSR = 32$ and a 5-b RZ DAC with $\alpha = 0.25$ and $\beta = 0.75$. Architecture B was simulated for an OSR$= 16$ and a 5-b NRZ DAC with $\alpha = 0.5$ and $\beta = 1.5$. Fig. 5 shows the SNR at the modulator output as a function of the normalized clock jitter $\sigma_j/T_S$ for the independent clock-jitter approximation [in (a)] and the normalized *effective* clock jitter $\sigma_{j,\text{eff}}/T_S = (\sigma_j/\sqrt{N_{pts}})/T_S$ for the accumulated clock-jitter approximation [in (b)].

The results of the SIMULINK simulations are compared for a CT $\Delta\Sigma$ modulator (based on the developed SIMULINK feedback-DAC blocks) and an equivalent DT $\Delta\Sigma$ modulator (based on the proposed DT modeling technique). In Fig. 5, the excellent matching (to within 1-dB) between the simulation results for the DT and CT $\Delta\Sigma$ modulators demonstrates the accuracy of the proposed DT modeling technique.

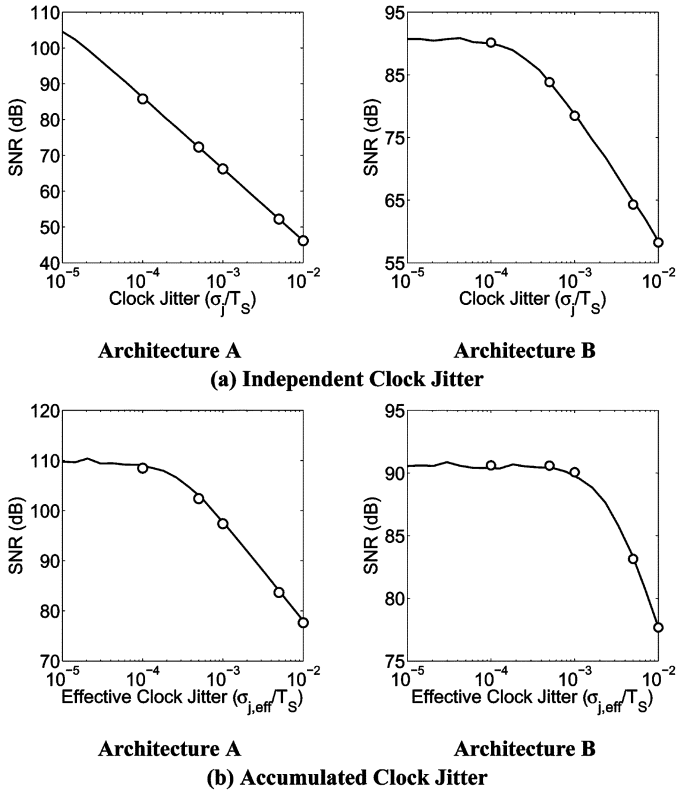


Fig. 5. SNR versus (a) normalized *independent* jitter $\sigma_j/T_S$ and (b) normalized effective *accumulated* jitter $\sigma_{j,\text{eff}}/T_S = (\sigma_j/\sqrt{N_{pts}})/T_S$. ○ = CT ΔΣ modulator, based on the developed SIMULINK blocks for feedback DACs. — = Equivalent DT ΔΣ modulator, based on the proposed DT modeling technique.

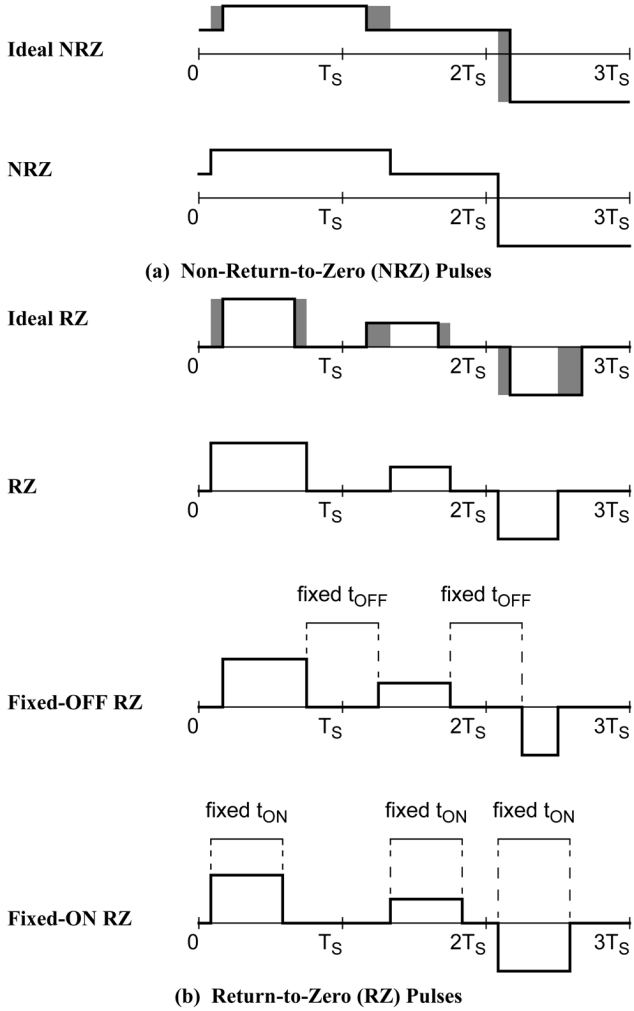


Fig. 6. Feedback-DAC rectangular pulses studied in the jitter analysis. The shaded areas on the ideal pulses represent the edge errors due to clock jitter. (a) Ideal NRZ pulse shape and the corresponding jittered NRZ pulse. (b) Ideal RZ pulse shape and the corresponding jittered RZ pulse, fixed-ON RZ pulse (i.e., jittered RZ pulse with a fixed on-time duration), and fixed-OFF RZ pulse (i.e., jittered RZ pulse with a fixed off-time duration).

## IV. Jitter Analysis

Here, the proposed DT modeling technique is applied to study the relative effectiveness of different rectangular feedback-DAC pulses (Fig. 6) in reducing the effect of clock jitter on the performance of CT ΔΣ modulators. The analysis examines lowpass and bandpass ΔΣ modulators (Table III), in both single-bit and multibit configurations.

Fig. 6 illustrates the different feedback-DAC pulses that will be studied in the jitter analysis:

1) NRZ pulse, where the $\alpha$ pulse edge of the *current* clock cycle corresponds to the $\beta$ pulse edge of the *previous* clock cycle, such that $\tilde{\alpha}(n) = \tilde{\beta}(n-1) - 1$;
2) RZ pulse, with uncorrelated errors $\Delta\alpha(n)$ and $\Delta\beta(n)$ on the $\alpha$ and $\beta$ edges;
3) RZ pulse with a fixed off-time (fixed-OFF RZ), where the $\alpha$ pulse edge of the *current* clock cycle is generated using the $\beta$ pulse edge of the *previous* clock cycle, in order to achieve $\Delta\alpha(n) = \Delta\beta(n-1)$ and, hence, a fixed off-time duration $t_{\text{off}}$ for the DAC pulses [15];
4) RZ pulse with a fixed on-time (fixed-ON RZ), where the $\beta$ pulse edge is generated using the $\alpha$ pulse edge, in order to achieve $\Delta\alpha(n) = \Delta\beta(n)$ and, hence, a fixed on-time duration $t_{\text{on}}$ for the DAC pulses.

Table III describes the loop transfer functions of the ΔΣ modulator architectures that will be studied in the jitter analysis, indicating the placement of the zeros in the NTF of each modulator. The exact transfer functions were designed using the Delta-Sigma Toolbox [16]. An oversampling ratio of OSR= 256 was assumed for all three architectures to ensure that the jitterinduced errors were dominant in the signal band, compared to the quantization errors. In multibit configurations, a 5-b quantizer and a 5-b DAC were used.

### A. Lowpass ΔΣ Modulator

Fig. 7(a) and (b) compare the performance of the rectangular feedback-DAC pulses illustrated in Fig. 6, when each is employed in lowpass CT ΔΣ modulators with Architectures A and B (Table III), in single-bit and multibit configurations. Observe that the plots are effectively identical for both Architecture A (with all NTF zeros at dc) and Architecture B (with a pair of resonating NTF zeros within the signal band). Accordingly, the following conclusions can be inferred about the clock-jitter sensitivity of a lowpass CT ΔΣ modulator.

1) *Feedback-DAC Pulsing Scheme*: A fixed-ON RZ pulse significantly outperforms all other rectangular pulses (Fig. 6) in reducing the clock-jitter sensitivity of a lowpass CT ΔΣ

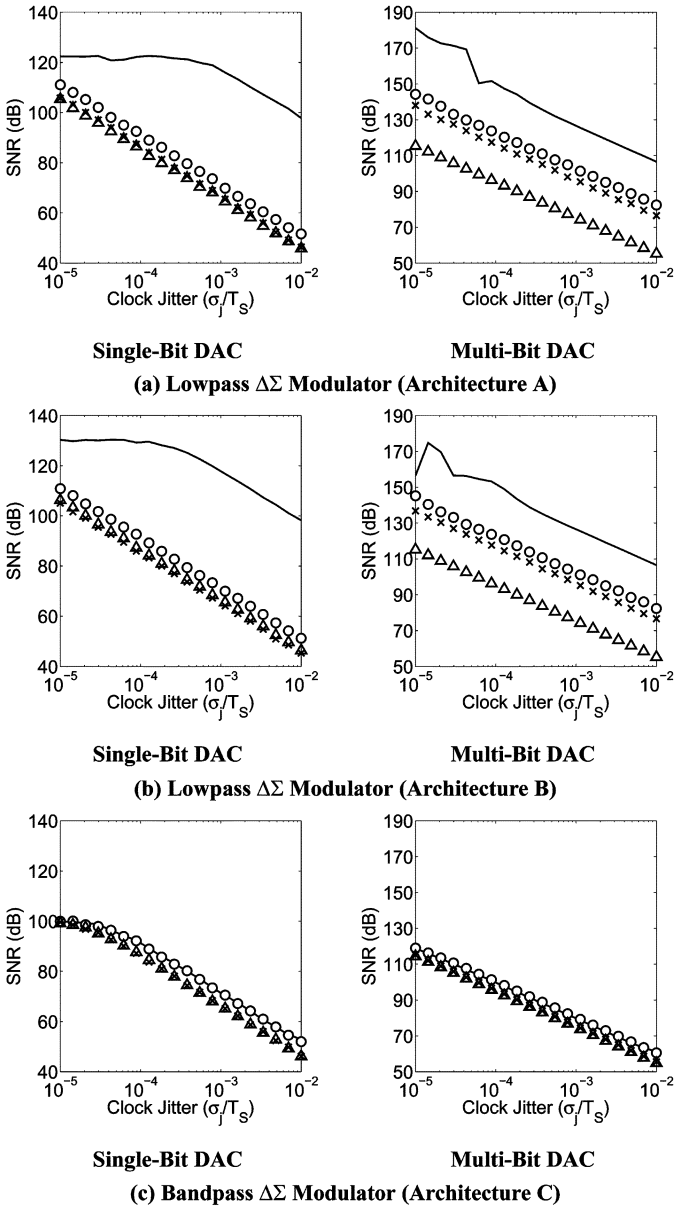


Fig. 7. Jitter performance for (a) a lowpass $\Delta\Sigma$ modulator with three NTF zeros at dc (Architecture A in Table III), (b) a lowpass $\Delta\Sigma$ modulator with one NTF zero at dc and an optimally-placed resonating pair (Architecture B), and (c) a bandpass $\Delta\Sigma$ modulator with NTF zeros spread optimally on either side of the center frequency (Architecture C). Here — = fixed-ON RZ; ◯ = NRZ; × = fixed-OFF RZ; and △ = RZ.

modulator [Figs. 7(a) and 9(b)]. This can be explained as follows:

Architecture A is a lowpass CT $\Delta\Sigma$ modulator with all its NTF zeros at dc ($z = 1$). Therefore, the loop transfer function of its equivalent DT $\Delta\Sigma$ modulator is composed of the three error-mapping terms in Table I. Hence, jitter-induced coefficient error $\Delta k_{31}$ is second-order high-pass shaped, errors $\Delta k_{21}$ and $\Delta k_{32}$ are first-order high-pass shaped, whereas errors $\Delta k_{11}$, $\Delta k_{22}$, and $\Delta k_{33}$ are not shaped by the $\Delta\Sigma$ loop (as described in Section II). A fixed-ON RZ pulse sets $\Delta\alpha = \Delta\beta$ and, hence, reduces the jitter-induced coefficient errors $\Delta k_{11}$, $\Delta k_{22}$, and $\Delta k_{33}$ (which are not suppressed by the $\Delta\Sigma$ loop) to zero. As a result, for Architecture A, a fixed-ON RZ pulse provides superior performance compared to all other rectangular pulses.

Architecture B is a lowpass CT $\Delta\Sigma$ modulator with one NTF zero at dc and a pair of resonating (complex-conjugate) NTF zeros in the signal band [17]. The loop transfer function of its equivalent DT $\Delta\Sigma$ modulator is therefore composed of error-mapping terms from both Tables I and II. However, the jitter-induced coefficient factors in Table II are neither suppressed by the $\Delta\Sigma$ loop (as described in Section II) nor reduced to their nominal value by using a fixed-ON RZ pulse with $\Delta\alpha = \Delta\beta$. Yet, Architecture B still provides performance equivalent to that of Architecture A, whose loop transfer function is composed of error terms from Table I only (as described above). To understand why this is the case, observe that the jitter-induced coefficient factor in Table II reduces to

$$\delta k_{p2} = k_{p2} z_p^{-\Delta\alpha} = k_{p2} e^{-j2\pi(f_p/f_S)\Delta\alpha} \tag{12}$$

when setting $\Delta\alpha = \Delta\beta$ using a fixed-ON RZ pulse. Here, $f_s$ is the sampling frequency and $f_p$ is the frequency of pole $z_p$ in the loop-transfer function. Under the condition that $f_s \gg f_p$, the coefficient factor $\delta k_{p2}$ in (12) further reduces to its nominal value $k_{p2}$, independent of the jitter-induced time-delay error $\Delta\alpha$. In a lowpass $\Delta\Sigma$ modulator, $f_p$ is placed within the signal band $[0, f_{\mathrm{BW}}]$. Define the oversampling ratio of the $\Delta\Sigma$ modulator as OSR $= f_s/(2f_{\mathrm{BW}})$. Then, in a lowpass $\Delta\Sigma$ modulator, the condition $f_s \gg f_p$ is equivalent to $OSR \gg 1$, which is readily achievable. As a result, in a lowpass $\Delta\Sigma$ modulator, the fixed-ON RZ pulse provides a performance that is superior to all other rectangular feedback-DAC pulses, irrespective of whether or not the modulator NTF has one or more pairs of resonating zeros within the signal band.

2) *Multibit DAC*: Increasing the number of quantization bits (DAC levels) significantly improves the performance of both the NRZ and the fixed-OFF RZ pulsing schemes [Fig. 7(a) and (b)] in reducing the clock-jitter sensitivity of a lowpass CT $\Delta\Sigma$ modulator. However, it has no noticeable effect on the performance of a standard RZ pulse. Hence, with multibit DACs, both NRZ and fixed-OFF RZ pulses provide a significant advantage over a standard RZ pulse. This can be explained as follows:

Increasing the number of quantization bits decreases the sample-to-sample change in the output signal of the lowpass $\Delta\Sigma$ modulator and, hence, in the step size of the associated rectangular feedback-DAC pulses. Consequently, charge transfer errors (due to clock jitter) at the output of the feedback DAC are reduced during each output transition. For an NRZ pulse, this significantly improves the performance. However, for RZ pulses (except for the fixed-OFF RZ pulse), this does not noticeably improve the performance because of the large number of DAC output transitions (as compared to an NRZ pulse) and, hence, the large total charge-transfer error. A fixed-OFF RZ pulse effectively compensates for errors introduced in the previous clock cycle during the current clock cycle and,

therefore, is sensitive to only one pulse edge. As a result, a fixed-OFF RZ pulse provides similar performance to an NRZ pulse, although approximately 6-dB lower. However, the primary advantage of a fixed-OFF RZ pulse (which is true for all RZ pulses) versus an NRZ pulse is that it reduces the memory effects in the feedback DAC and, hence, minimizes intersymbol interference (ISI) errors, which can degrade the performance of an NRZ DAC [8].

### B. Bandpass ΔΣ Modulators

Fig. 7(c) compares the performance of the rectangular feedback-DAC pulses illustrated in Fig. 6, when each is employed in a bandpass CT ΔΣ modulator with Architecture C (Table III), in single-bit and multibit configurations. The performance observed for the bandpass ΔΣ modulator differs considerably from that observed above for the lowpass ΔΣ modulators. The following conclusions can be inferred from Fig. 7(c) regarding the clock-jitter sensitivity of a bandpass CT ΔΣ modulator.

1) *Feedback-DAC Pulsing Scheme*: In a bandpass ΔΣ modulator, the fixed-ON RZ pulse no longer provides any advantage over the other rectangular feedback-DAC pulses [Fig. 7(c)], contrary to the case of a lowpass ΔΣ modulator [Fig. 7(a) and (b)]. This can be explained as follows. Architecture C is a bandpass CT ΔΣ modulator with pairs of resonating (complex-conjugate) NTF zeros spread optimally within its signal band. Therefore, the loop-transfer function of its equivalent DT ΔΣ modulator is composed of error-mapping terms from Table II only. For a bandpass ΔΣ modulator, the frequency $f_p$ of pole $z_p$ in the loop transfer function is within the signal band $[f_0 \pm f_{\rm BW}/2]$, where $f_0$ is the bandpass center frequency. Therefore, the condition $f_s \gg f_p$ corresponds to $f_s \gg f_0/(1 - 1/4{\rm OSR})$, where ${\rm OSR} = f_s/(2f_{\rm BW})$ is the oversampling ratio. However, for ease of implementing the digital mixers after the bandpass ΔΣ modulator [12], the sampling frequency is typically selected as $f_s = 4f_0$. Therefore, the condition $f_s \gg f_p$ (which is true for a lowpass ΔΣ modulator) is not readily achievable in a bandpass ΔΣ modulator. Consequently, in a bandpass ΔΣ modulator, the jitter-induced coefficient factor $\delta k_{p2}$ in (12) does not reduce to its nominal value $k_{p2}$, when setting $\Delta\alpha = \Delta\beta$ using a fixed-ON RZ pulse (this is contrary to the case of a lowpass ΔΣ modulator). As a result, in a bandpass ΔΣ modulator, all rectangular feedback-DAC pulses provide an approximately equivalent performance [Fig. 7(c)].

2) *Multibit DAC*: Increasing the number of quantization bits (DAC levels) does not improve the performance of the NRZ and the fixed-OFF RZ pulses in reducing the clock-jitter sensitivity of a bandpass ΔΣ modulator [Fig. 7(c)]. This is contrary to the case of a lowpass ΔΣ modulator [Fig. 7(a) and (b)]. This can be explained as follows.
In a lowpass ΔΣ modulator, the input signal is limited to low frequencies relative to the sampling frequency $f_s$ (assuming an $OSR \gg 1$). Therefore, a signal at the center of the signal band is sampled $OSR$ times over its period. As a result, with multibit quantization, the sample-to-sample variations in the output signal of the lowpass ΔΣ modulator are small. However, in a bandpass ΔΣ modulator, the input signal is typically sampled at $f_s = 4f_0$ for ease of implementing the digital mixers after the bandpass ΔΣ modulator [12]. This means that a signal at the center of the signal band is only sampled 4 times over its period. Consequently, the sample-to-sample signal variations at the modulator output and hence, the average step size of the rectangular feedback-DAC pulses tend to be considerably greater in a bandpass ΔΣ modulator, as compared to an equivalent lowpass ΔΣ modulator. Therefore, the decrease in the average step size of the feedback-DAC pulses when using a multibit quantizer is not significant for a bandpass ΔΣ modulator. As a result, increasing the number of quantization bits does not noticeably improve the performance of the NRZ and fixed-OFF RZ pulses in a bandpass ΔΣ modulator. Hence, in terms of clock-jitter sensitivity, a multibit bandpass ΔΣ modulator provides no advantage over an equivalent single-bit implementation.

## V. Conclusion

A discrete-time modeling technique was proposed to rapidly, yet accurately, simulate the effect of clock jitter on continuous-time ΔΣ modulators. The technique was validated (for both independent and accumulated clock-jitter errors) using behavioral blocks, which were developed in SIMULINK to accurately simulate RZ or NRZ DACs with clock jitter. The effect of clock jitter was then analyzed for both lowpass and bandpass continuous-time ΔΣ modulators using four different rectangular feedback-DAC pulses: 1) NRZ; 2) RZ; 3) RZ with a fixed on-time duration (fixed-ON RZ); and 4) RZ with a fixed off-time duration (fixed-OFF RZ). For a lowpass ΔΣ modulator, in terms of reducing the modulator sensitivity to clock jitter, it was shown that: 1) a fixed-ON RZ pulse has a superior performance compared to all other rectangular pulses and 2) the performance of the NRZ and fixed-OFF RZ pulses improves significantly when using a multibit DAC rather than a single-bit DAC (i.e., when increasing the number of quantization bits and DAC levels), whereas the performance of the standard RZ pulse is not noticeably affected. For a bandpass ΔΣ modulator, in terms of reducing the modulator sensitivity to clock jitter, it was shown that: 1) all feedback-DAC rectangular pulses have an approximately equivalent performance and 2) there is no noticeable improvement in the performance of the feedback-DAC pulses when using a multibit DAC.

## Appendix I

Section II presented the implementation of the second-order error-mapping term $\hat{H}_2(z)$ in Fig. 3(a), through a simplified derivation that seemingly applied the Laplace and $Z$ transforms to a time-varying impulse response. This appendix presents a more rigorous derivation of the implementation in Fig. 3(a), outlining all assumptions and intermediate steps, to demonstrate the validity of the results obtained in Section II.

As in Section II, this derivation starts with the second-order term of a DT loop transfer function

$$H_2(z) = \frac{k_2}{(z-1)^2}. \tag{13}$$

Equation (13) is then transformed into the $s$-domain using a $z \rightarrow s$ impulse-invariant transform with *nominal* pulse-edge timing parameters $\alpha$ and $\beta$

$$H_2(s) = \frac{r_1(sT_S) + r_2}{(sT_S)^2} \cdot \mathrm{DAC}(s) \tag{14}$$

where

$$\begin{aligned} r_1 =& (1/2)k_2((\alpha+\beta-2)/(\beta-\alpha)) \\ r_2 =& k_2(1/(\beta-\alpha)) \end{aligned}$$

and $\mathrm{DAC}(s)$ is the transfer function of the feedback DAC. Observe that, unlike (7), $DAC(s)$ has been included explicitly in (14). For a rectangular feedback pulse:

$$\mathrm{DAC}(s) = \frac{1}{s}(e^{-s\alpha T_S} - e^{-s\beta T_S}) \tag{15}$$

where $\alpha$ and $\beta$ are normalized to the sampling period $T_S$.

To demonstrate how jitter-induced errors are translated into the $z$ domain, $H_2(s)$ in (14) is first transformed into the time domain using an inverse Laplace transform

$$\begin{aligned} h_2(t) = &\left[(t-\alpha T_S)\frac{r_1}{T_S} + (t-\alpha T_S)^2\frac{r_2}{2T_S^2}\right]u(t-\alpha T_S) \\ &- \left[(t-\beta T_S)\frac{r_1}{T_S} + (t-\beta T_S)^2\frac{r_2}{2T_S^2}\right]u(t-\beta T_S) \end{aligned} \tag{16}$$

where $u(t)$ is the unit-step function.

The next step in the derivation differs, depending on whether the DAC has: 1) an RZ feedback pulse, with the $\alpha$ and $\beta$ edges occurring in the same clock cycle (i.e., $0 \le \alpha \le 1$ and $0 \le \beta \le 1$) or 2) an NRZ feedback pulse, with the $\beta$ edge occurring in the clock cycle after the $\alpha$ edge (i.e., $0 \le \alpha \le 1$ and $1 \le \beta \le 2$). Each case is derived separately below.

*RZ Feedback Pulse:* For an RZ feedback pulse, it is assumed that $0 \le \alpha \le 1$ and $0 \le \beta \le 1$. Therefore, when $h_2(t)$ is sampled at intervals of $T_S$, both $u(t-\alpha T_S)$ and $u(t-\beta T_S)$ in (16) reduce to $u(n-1)$. The sampled impulse response is then equal to

$$\begin{aligned} h_2(n) = &\left[(n-\alpha)r_1 + (n-\alpha)^2\frac{r_2}{2}\right]u(n-1) \\ &- \left[(n-\beta)r_1 + (n-\beta)^2\frac{r_2}{2}\right]u(n-1). \end{aligned} \tag{17}$$

Replacing the *nominal* pulse-edge timing parameters $\alpha$ and $\beta$ in (17) with their *clock-jittered* equivalents $\widehat{\alpha}(m)$ and $\widehat{\beta}(m)$ (defined in (3)), the resulting time-varying impulse response can be expressed as

$$\widehat{h}_2(n,m) = h_2(d) + h_{2\alpha}(d)\Delta\alpha(m) + h_{2\beta}(d)\Delta\beta(m) \tag{18}$$

where

$$\begin{aligned} d =& n-m \\ h_{2\alpha}(d) =& -[r_1 + (d-1)r_2 + (1-\alpha)r_2]u(d-1) \\ h_{2\beta}(d) =& [r_1 + (d-1)r_2 + (1-\beta)r_2]u(d-1) \end{aligned}$$

and $h_2(d)$ is given in (17). Here, $d$ is the delay between time $m$ when the input sample is applied, and time $n$ when the output sample is observed. Note that the second-order error terms $\Delta\alpha(m)^2$ and $\Delta\beta(m)^2$ have been removed from (18), as $|\Delta\alpha(m)| < 1$ and $|\Delta\beta(m)| < 1$ and, hence, the first-order error terms $\Delta\alpha(m)$ and $\Delta\beta(m)$ dominate.

Since the individual impulse responses $h_2(n)$, $h_{2\alpha}(n)$ and $h_{2\beta}(n)$ in (17) and (18) are time invariant, their $Z$ transforms can be directly computed as

$$H_2(z) = \frac{k_2}{(z-1)^2} \tag{19}$$

$$H_{2\alpha}(z) = -\frac{k_2}{2}\frac{1}{z-1} - \frac{k_2}{\beta-\alpha}\frac{1}{(z-1)^2} \tag{20}$$

$$H_{2\beta}(z) = -\frac{k_2}{2}\frac{1}{z-1} + \frac{k_2}{\beta-\alpha}\frac{1}{(z-1)^2}. \tag{21}$$

In (18), jitter-induced errors $\Delta\alpha(m)$ and $\Delta\beta(m)$ depend only on time $m$, when the input is applied. This models the behavior of a CT $\Delta\Sigma$ modulator, where the input of the loop filter during clock cycle $m$ [i.e., the DAC feedback signal $x_{DAC}(m)$ in Fig. 1(a)] is affected only by the jitter-induced timing errors $\Delta\alpha(m)$ and $\Delta\beta(m)$ introduced during clock cycle $m$. Since $\Delta\alpha(m)$ and $\Delta\beta(m)$ depend only on time $m$ when the input is applied, they can be easily shifted from the impulse response $\widehat{h_2}(n,m)$ to the input. Thus, the response of $\widehat{h_2}(n,m)$ to $x_{DAC}(m)$ can be expressed, using a standard input–output relationship, as

$$\widehat{y_{H2}}(n) = -\sum_{m=0}^{n} \widehat{h_2}(n,m)x_{\mathrm{DAC}}(m) \tag{22}$$

where $x_{\mathrm{DAC}}(m)$ and $\widehat{y_{H2}}(n)$ represent, respectively, the input and output of the loop filter with impulse response $\widehat{h_2}(n,m)$, assuming no signal is applied at the modulator input. The output in (22) can then be split into three components as

$$\widehat{y_{H2}}(n) = y_{H2}(n) + \widehat{y_{H2\alpha}}(n) + \widehat{y_{H2\beta}}(n) \tag{23}$$

where

$$y_{H2}(n) = -\sum_{m=0}^{n} h_2(n-m)x_{\mathrm{DAC}}(m) \tag{24}$$

$$\widehat{y_{H2\alpha}}(n) = -\sum_{m=0}^{n} h_{2\alpha}(n-m)\Delta\alpha(m)x_{\mathrm{DAC}}(m) \tag{25}$$

$$\widehat{y_{H2\beta}}(n) = -\sum_{m=0}^{n} h_{2\beta}(n-m)\Delta\beta(m)x_{\mathrm{DAC}}(m). \tag{26}$$

Observe that, based on (24)–(26), $x_{\mathrm{DAC}}(m)$, $\Delta\alpha(m)x_{\mathrm{DAC}}(m)$ and $\Delta\beta(m)x_{\mathrm{DAC}}(m)$ can now be viewed as the inputs to loop-filter components $H_2(z)$, $H_{2\alpha}(z)$ and $H_{2\beta}(z)$, respectively. Hence, error sequences $\Delta\alpha(m)$ and $\Delta\beta(m)$ only act as scaling factors on the loop-filter input signal $x_{\mathrm{DAC}}(m)$ and, therefore, can be treated as gain errors in the coefficients of an equivalent DT $\Delta\Sigma$ modulator. Accordingly, using (19)–(21), the total loop-filter output $\widehat{y_{H2}}(n)$ can be generated in the DT domain using Fig. 8. This implementation matches the one

presented in Fig. 3(a), thereby confirming the validity of the results derived in Section II.

*NRZ Feedback Pulse:* For an NRZ feedback pulse, it is assumed that $0 \leq \alpha \leq 1$, $\beta = 1 + \alpha$, and, hence, $1 \leq \beta \leq 2$. Therefore, when $h_2(t)$ is sampled at intervals of $T_S$, $u(t-\alpha T_S)$ in (16) reduces to $u(n-1)$, as in the RZ case. However, since $1 \leq \beta \leq 2$, $u(t-\beta T_S)$ now reduces to $u(n-2)$. Thus, for the NRZ feedback pulse, the sampled impulse response in (16) reduces to

$$h_{2,\mathrm{NRZ}}(n) = \left[(n-\alpha)r_1 + (n-\alpha)^2\frac{r_2}{2}\right]u(n-1) - \left[(n-\beta)r_1 + (n-\beta)^2\frac{r_2}{2}\right]u(n-2). \quad (27)$$

Replacing the *nominal* pulse-edge timing parameters $\alpha$ and $\beta$ in (27) with their *clock-jittered* equivalents $\widehat{\alpha}(m)$ and $\widehat{\beta}(m)$ [defined in (3)], the resulting time-varying impulse response can be expressed as

$$\widehat{h_{2,\mathrm{NRZ}}}(n,m) = h_{2,\mathrm{NRZ}}(d) + h_{2\alpha,\mathrm{NRZ}}(d)\Delta\alpha(m) + h_{2\beta,\mathrm{NRZ}}(d)\Delta\beta(m) \quad (28)$$

where

$$\begin{aligned} d &= n-m \\ h_{2\alpha,\mathrm{NRZ}}(d) &= -[r_1 + (d-1)r_2 + (1-\alpha)r_2]u(d-1) \\ h_{2\beta,\mathrm{NRZ}}(d) &= [r_1 + (d-2)r_2 + (2-\beta)r_2]u(d-2) \end{aligned}$$

and $h_{2,\mathrm{NRZ}}(d)$ is given in (27). Comparing (28) to the case of an RZ feedback pulse in (18), note that:

- the $Z$ transform of $h_{2,\mathrm{NRZ}}(d)$ reduces to $H_2(z)$ in (19), after compensating for excess loop delay [8];
- the $Z$ transform of $h_{2\alpha,\mathrm{NRZ}}(d)$ is equal to $H_{2\alpha}(z)$ in (20), as $h_{2\alpha,\mathrm{NRZ}}(d)$ in (28) is equal to $h_{2\alpha}(d)$ in (18);
- the $Z$ transform of $h_{2\beta,\mathrm{NRZ}}(d)$ is:

$$H_{2\beta,\mathrm{NRZ}}(z) = -\frac{k_2}{2}\left[1 - \frac{2}{\beta-\alpha}\right]\frac{z^{-1}}{z-1} + \frac{k_2}{\beta-\alpha}\frac{z^{-1}}{(z-1)^2} \quad (29)$$

Since $\beta = 1 + \alpha$ for an NRZ feedback pulse, (29) can be simplified to

$$H_{2\beta,\mathrm{NRZ}}(z) = \frac{k_2}{2}\frac{z^{-1}}{z-1} + \frac{k_2}{\beta-\alpha}\frac{z^{-1}}{(z-1)^2}. \quad (30)$$

The added delay in $H_{2\beta,\mathrm{NRZ}}(z)$, as compared with $H_{2\beta}(z)$ in (21), reflects the fact that the input to $H_{2\beta,\mathrm{NRZ}}(z)$ (i.e., $\Delta\beta(m)x_{\mathrm{DAC}}(m)$) is generated in the previous clock cycle. Furthermore, the difference in sign between the first-order terms of $H_{2\beta,\mathrm{NRZ}}(z)$ and $H_{2\beta}(z)$ has no effect on the results of the DT models.

The remainder of the derivation for the implementation of the second-order mapping term in Fig. 3(a) for the case of an NRZ feedback pulse matches the above derivation for the case of an RZ feedback pulse. Accordingly, since the loop-filter responses ($H_{2,\mathrm{NRZ}}(z)$, $H_{2\alpha,\mathrm{NRZ}}(z)$, and $H_{2\beta,\mathrm{NRZ}}(z)$) in the NRZ case match the corresponding responses in the RZ case, the total loop-filter output $\widehat{y_{H2,\mathrm{NRZ}}}(n)$ can also be generated in the DT domain using Fig. 8.

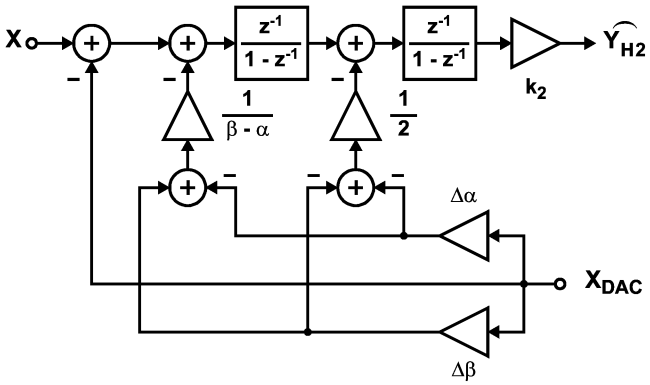


Fig. 8. DT implementation of the second-order mapping term, with output $\widehat{y_{H2}}(n)$ in (23). The terminal names correspond to the DT $\Delta\Sigma$ modulator illustrated in Fig. 1(b).

In summary, the derivation of the error mapping terms presented in Section II produces correct results, since the time-varying terms $\Delta\alpha(m)$ and $\Delta\beta(m)$ can be shifted to the input of loop filter components $H_{2,\mathrm{NRZ}}(z)$, $H_{2\alpha,\mathrm{NRZ}}(z)$, and $H_{2\beta,\mathrm{NRZ}}(z)$, as in (24)–(26). Therefore, the $\Delta\alpha(m)$ and $\Delta\beta(m)$ terms are not processed by the Laplace transform in (14) or by the $Z$ transform in (19)–(21). Thus, a CT $\Delta\Sigma$ modulator affected by clock jitter (i.e., a time-varying system) is converted into a time-invariant system (in the form of a DT $\Delta\Sigma$ modulator) where the input to the loop filter (the output of the feedback DAC) is scaled by $\Delta\alpha(m)$ or $\Delta\beta(m)$. A comparable approach is described in [11] for general time-varying systems.

## Appendix II

To validate the proposed DT modeling technique, SIMULINK blocks are developed for the behavioral simulation of DACs that generate jittered RZ and NRZ pulses in the feedback path of CT $\Delta\Sigma$ modulators. The goal is to implement a simple system that realistically and, therefore, accurately simulates the effect of clock jitter in a CT $\Delta\Sigma$ modulator, while allowing for full control over the timing of the generated pulse edges in its feedback DAC.

This appendix first presents a SIMULINK block that generates a rectangular clock signal with jittered edges. It then describes how this clock generator can be utilized for the behavioral simulation of RZ and NRZ DACs that generate jittered rectangular pulses in CT $\Delta\Sigma$ modulators.

*Generation of a Jittered Clock in SIMULINK:* The developed SIMULINK block for jittered-clock generation is shown in Fig. 9. Its inputs are the ideal clock-edge timing ($\alpha$ and $\beta$) and the time-delay errors due to clock jitter ($\Delta\alpha$ and $\Delta\beta$)[1]. Its output is a delayed rectangular clock signal with jittered edges, as per (3).

The jittered-clock generator is implemented entirely in discrete time, as the continuous-time delay blocks in SIMULINK do not provide sufficient accuracy. It is divided into two sampling domains (Fig. 9): 1) a *nominal-resolution domain*, operating at the sampling period $T_S$ and 2) a *high-resolution domain*, operating at a period of $T_S/N_R$. Here, the integer $N_R$ divides

[1]Recall that all time references $\alpha$, $\beta$, $\widehat{\alpha}$, $\widehat{\beta}$, $\Delta\alpha$, and $\Delta\beta$ are normalized with respect to the sampling clock period $T_S$.

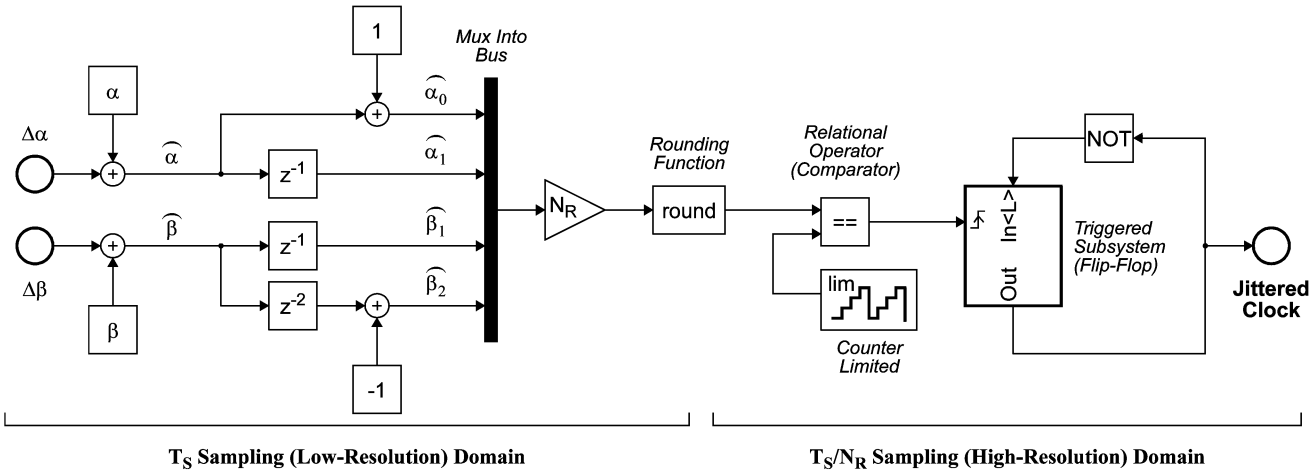


Fig. 9. Block diagram of the jittered-clock generator developed in SIMULINK.

the sampling period into smaller time segments, thereby setting the maximum resolution for time-delay variations (i.e., the maximum pulse-edge resolution). Observe that increasing the resolution $N_R$ results in a proportional increase in simulation time.

The blocks operating in the nominal-resolution ($T_S$ sampling) domain are responsible for generating the timing of the $\alpha$ and $\beta$ edges (Fig. 9). First, the nominal pulse-edge timing values ($\alpha$ and $\beta$) are added to the time-delay errors ($\Delta\alpha$ and $\Delta\beta$) in order to compute the actual pulse-edge timing values ($\hat{\alpha}$ and $\hat{\beta}$), as per (3). The $\hat{\alpha}$ and $\hat{\beta}$ values are computed during the clock cycle *prior to* the nominal clock cycle of the corresponding clock pulse. Then, offset and/or delayed versions of $\hat{\alpha}$ and $\hat{\beta}$ are multiplexed into a bus. These timing versions are subsequently used in the high-resolution domain of the clock generator to set the timing of the $\alpha$ and $\beta$ clock edges, as described below. The version used (i.e., $\hat{\alpha}_0$ or $\hat{\alpha}_1$ and $\hat{\beta}_1$ or $\hat{\beta}_2$) depends on the values of $\hat{\alpha}$ and $\hat{\beta}$ *prior* to the nominal clock cycle, as summarized in Table IV. Note that $\hat{\alpha}$ is offset by 1 if $-1 \le \hat{\alpha} < 0$ and $\hat{\beta}$ is offset by $-1$ if $1 \le \hat{\beta} < 2$, such that the timing values used to generate the corresponding $\alpha$ and $\beta$ clock edges (i.e., $\hat{\alpha}_0$ and $\hat{\beta}_2$) are always between 0 and 1 during the corresponding clock cycle.

The blocks operating in the high-resolution ($T_S/N_R$ sampling) domain translate the $\hat{\alpha}$ and $\hat{\beta}$ values computed in the nominal-resolution domain into edge timing for the jittered clock signal at the generator output (Fig. 9). This is realized by first converting the $\hat{\alpha}_0$, $\hat{\alpha}_1$, $\hat{\beta}_1$, and $\hat{\beta}_2$ values into integers between 0 and $N_R - 1$, through scaling by the pulse-edge resolution $N_R$ and rounding. These integers are then compared with the output of a global counter, which has limits 0 and $N_R - 1$. The integers selected by the comparator depend on the $\hat{\alpha}$ and $\hat{\beta}$ values *prior* to the nominal clock cycle, as summarized in Table IV. The result of the comparison is a series of impulses, which are used as the clocking signal for an output flip-flop. The output of the flip-flop switches (from $0 \rightarrow 1$ or $1 \rightarrow 0$) upon arrival of either an $\hat{\alpha}$ or a $\hat{\beta}$ impulse. This simplifies the generation of the output signal and eliminates timing conflicts due to an unintentional overlap of $\hat{\alpha}$ and $\hat{\beta}$. Proper timing is guaranteed by ensuring that the first $\alpha$ edge occurs prior to the first $\beta$ edge.

TABLE IV
SELECTION OF THE MULTIPLEXED $\hat{\alpha}$ AND $\hat{\beta}$ SIGNALS BY THE COMPARATOR IN FIG. 9

| Timing range of jittered pulse edge | Clock cycle when pulse edge occurs | Value selected by comparator to generate pulse edge |
|---|---|---|
| $-1 \le \widehat{\alpha}(n) < 0$ | $n$ | $\widehat{\alpha_0}$ |
| $0 \le \widehat{\alpha}(n) < 1$ | $n+1$ | $\widehat{\alpha_1}$ |
| $0 \le \widehat{\beta}(n) < 1$ | $n+1$ | $\widehat{\beta_1}$ |
| $1 \le \widehat{\beta}(n) < 2$ | $n+2$ | $\widehat{\beta_2}$ |

**Note:** Here, $n$ is the clock-cycle index. The $\widehat{\alpha}$ and $\widehat{\beta}$ values are computed during the clock cycle *prior to* the nominal clock cycle of the corresponding clock pulse. It is assumed that the clock jitter does not force the $\alpha$ edge into the next clock cycle or the $\beta$ edge into the previous clock cycle.

*RZ DAC:* An RZ DAC block can be realized in SIMULINK by applying the output of the developed clock generator (Fig. 9) as both the clocking signal and the active-low reset of a standard flip-flop. This approach is equally viable for modeling single-bit and multibit DACs, as it only applies a time delay to the DAC input signal.

*NRZ DAC:* An NRZ DAC block can be realized in SIMULINK by applying the output of the developed clock generator (Fig. 9) as the clocking signal of a standard flip-flop. The timing of the $\beta$ clock edge is not critical in the case of an NRZ pulse (Fig. 2), provided it is correctly initialized to ensure that $\hat{\beta} > \hat{\alpha}$.

## REFERENCES

[1] L. J. Breems, R. Rutten, R. H. M. van Veldhoven, and G. van der Weide, "A 56 mW continuous-time quadrature cascaded $\Sigma\Delta$ modulator with 77 dB DR in a near zero-IF 20 MHz band," *IEEE J Solid-State Circuits*, vol. 42, no. 12, pp. 2696–2705, Dec. 2007.

[2] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani, "A 20-mW 640-MHz CMOS continuous-time $\Sigma\Delta$ ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2641–2649, Dec. 2006.

[3] J. A. Cherry and W. M. Snelgrove, "Clock jitter and quantizer metastability in continuous-time delta-sigma modulators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 46, no. 6, pp. 661–676, Jun. 1999.
[4] H. Tao, L. Toth, and J. M. Khoury, "Analysis of timing jitter in bandpass sigma-delta modulators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 8, pp. 991–1001, Aug. 1999.
[5] M. Ortmanns and F. G. Manoli, "A continuous-time $\Sigma\Delta$ modulator with reduced sensitivity to clock jitter through SCR feedback," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 5, pp. 875–884, May 2005.
[6] K. R. Pavan, "Fundamental limitations of continuous-time delta-sigma modulators due to clock jitter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 10, pp. 2184–2194, Oct. 2007.
[7] F. Gardner, "A transformation for digital simulation of analog filters," *IEEE Trans. Commun.*, vol. COM-34, no. 7, pp. 676–680, Jul. 1986.
[8] J. A. Cherry and W. M. Snelgrove, "Excess loop delay in continuous-time delta-sigma modulators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 4, pp. 376–389, Apr. 1999.
[9] L. Hernandez, A. Wiesbauer, S. Paton, and A. D. Giandomenico, "Modelling and optimization of low pass continuous-time sigma-delta modulators for clock jitter noise reduction," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2004, pp. 1072–1075.
[10] O. Oliaei and H. Aboushady, "Jitter effects in continuous-time $\Sigma\Delta$ modulators with delayed return-to-zero feedback," in *Proc. IEEE Int. Conf. Electronics Circuits Syst.*, Sep. 1998, pp. 351–354.
[11] J. Roychowdhury, "Reduced-order modeling of time-varying systems," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 10, Oct. 1999.
[12] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Hoboken, NJ: IEEE Press/Wiley, 2005.
[13] A. Berkovitz and I. Rusnak, "FFT processing of randomly sampled harmonic signals," *IEEE Trans. Signal Process.*, vol. 40, no. 11, pp. 2816–2819, Nov. 1992.
[14] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillator," *IEEE J. Solid-State Circuits*, vol. 33, no. 1, pp. 179–194, Feb. 1998.
[15] S. Paton, A. D. Giandomenico, and L. Hernandez, "A 70-mW 300-MHz CMOS continuous-time $\Sigma\Delta$ ADC with 15-MHz bandwidth and 11 bits of resolution," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1056–1063, Jul. 2004.
[16] R. Schreier, The Delta-Sigma Toolbox v7.1 (Delsig) 2004 [Online]. Available: http://www.mathworks.com/matlabcentral/fileexchange/
[17] A. A. Hamoui and K. W. Martin, "High-order multibit modulators and pseudo data-weighted-averaging in low-oversampling $\Sigma\Delta$ ADCs for broadband applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 1, pp. 72–85, Jan. 2004.

**Philip M. Chopp** received the B.A.Sc. degree in computer engineering from the University of Waterloo, Waterloo, ON, Canada in 2005. He is currently working towards the Ph.D. degree at McGill University, Montreal, QC, Canada.

His research examines delta-sigma modulator architectures for analog-to-digital conversion of high-frequency signals.

Mr. Chopp was the recipient of a Canada Graduate Scholarship from the Natural Sciences and Engineering Research Council of Canada (NSERC) for his doctoral research.

**Anas A. Hamoui** received the B.Eng. (Honors) degree from Kuwait University, Kuwait, in 1996, the M.Eng. degree from McGill University, Montreal, QC, Canada, in 1998, and the Ph.D. degree from the University of Toronto, Toronto, ON, Canada, in 2004, all in electrical engineering.

From 1996 to 1998, he was a Research Assistant with the Microelectronics and Computer Systems Laboratory, McGill University, working in the area of timing and power analysis of submicron CMOS digital circuits. From 1998 to 2004, he was a Research Assistant and a Part-Time Instructor with the Electronics Group, University of Toronto, working in the area of analog and mixed-signal integrated circuits for high-speed data communications. Since 2004, he has been an Assistant Professor with the Department of Electrical and Computer Engineering, McGill University. His research emphasis is on analog-to-digital and digital-to-analog data converters. His contributions to the teaching of microelectronic circuits comprise writing the SPICE sections (including device models, circuit macromodels, and design examples) at the end of each chapter in the widely utilized textbook *Microelectronic Circuits* by A. S. Sedra and K. C. Smith.

Dr. Hamoui is an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS. He was the recipient of a Post-Graduate Scholarship from the Natural Sciences and Engineering Research Council of Canada (NSERC) and a Henderson Research Fellowship from the University of Toronto for his doctoral research. He was also a recipient of the 2001 Outstanding Student Designer Award from Analog Devices Inc. He is the co-chair of the Montreal Chapter of the Solid-State Circuit Society, the recipient of the 2007 Outstanding-Chapter Award. He was awarded the "Professor of the Year" Award by the Electrical, Computer and Software Engineering Student Society at McGill University for two consecutive years for his teaching of microelectronic circuits to undergraduate students.