

Analysis of Complete Power-Distribution Network and Co-Design Optimization

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Abstract

This paper describes the modelling analysis for a power-distribution network and demonstrates co-design and co-simulation in using the detailed prototype model, which includes a chip, package, and printed circuit board. A circuit simulator and a 2D solver using the finite element method are used to study the frequency and transient responses for the core switching noise. In the model, we assume a chip model (current profile and on-chip capacitance) and define the circuit parameters with an equivalent circuit to meet the target impedance. Then the physical design of the package and printed circuit board were done to check all of the required circuit parameters. According to the modelling and evaluation, the package design with a low equivalent series inductance capacitor in the bottom layer and a thin core structure is more advantageous than a capacitor in the top layer.

Keywords: Power-Distribution Network, Power Integrity, Target Impedance, Co-Design and Co-Simulation

1. Introduction

The design of the power distribution network (PDN) in high-end microprocessors is becoming critical as clock frequencies and power consumption continue to increase rapidly. As CMOS technologies are scaled, the power supply voltage is lowered, but as clock rates rise and more functions are integrated on-chip, the power consumed is greatly increased. These facts, coupled with higher operating frequencies and sharper clock edges, make the design of a PDN ever more challenging. In addition, as the core supply voltages are lowered to around 1V, only very small amounts of ripple in the power supply voltages can be tolerated.

The target impedance is defined as the ratio of noise voltage tolerance. For example, for a supply voltage of 1 V with a 5% maximum ripple tolerance requirement and a maximum current of 100 A, the target impedance will be 1 m-ohm ($1 \text{ V} \times 5\% / (100 \text{ A} \times 0.5)$). The PDN should have an impedance below the target impedance over a frequency range of DC to hundreds of MHz.[1]

In general, impedance peaks appear in the frequency range from a few MHz to tens of MHz. This is the mid-frequency noise, due to the circuit resonance from the on-chip capacitance and the effective inductance of the PDN including the package (PKG) parasitic inductance.[2, 3] A

good PDN design must keep this impedance peak below the target impedance.

However, in many cases, no detailed chip model is provided by the chip maker to clarify the required target impedance for the PKG or PCB design. It is very difficult to quantify the noise and target impedance through direct calculation from Ohm's law because of the complexity of the models. In this paper, we focus on a modeling methodology for target impedance that uses the current profile and on-chip capacitance.

2. Co-design and co-simulation

Figures 1 and 2 show the flows of co-design and co-simulation. Since the modelling analysis is done by individuals using conventional techniques, shortening the development time for faster delivery is difficult. When the development cycle of a product becomes very short, it is necessary to use a co-simulation platform so that the chip, PKG, and PCB, and the power integrity (PI), signal integrity (SI), and electromagnetic interference (EMI) can all be refined simultaneously.[4, 5]

3. PDN Equivalent circuit and modeling analysis

Figure 3 shows a PDN equivalent circuit and cross-

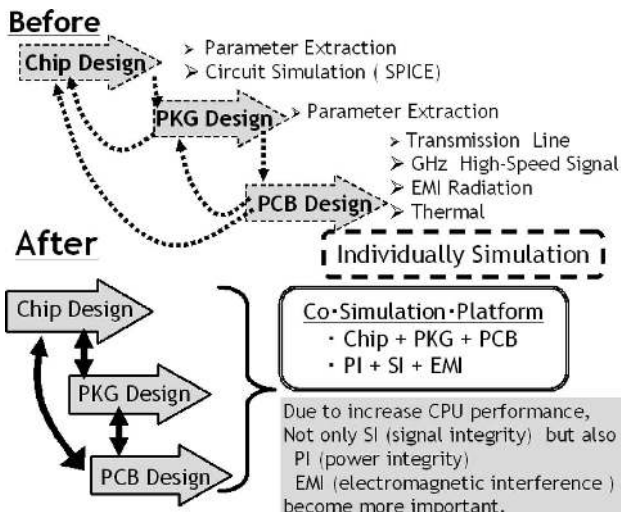


Fig. 1 Chip + PKG + PCB co-design flow.

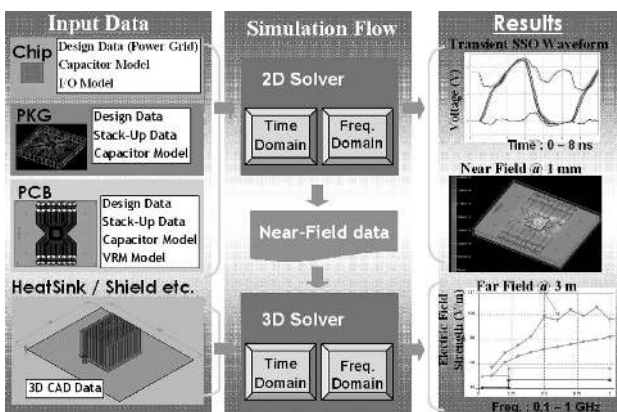


Fig. 2 Chip + PKG + PCB co-simulation flow.

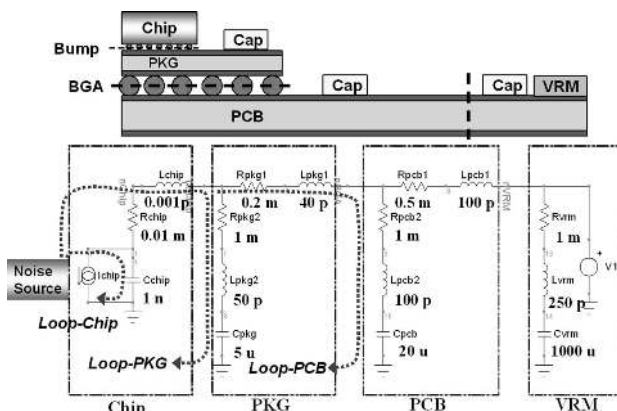


Fig. 3 Electrical equivalent circuit and cross-section of PDN.

section, which consists of a chip, PKG, PCB, and voltage regulator module (VRM). The voltage noise of the PDN can be defined as Z (the impedance of the PDN) $\times \Delta I$ (the change in the current). To reduce the power noise of the passive components, Z must be reduced.[6] There are loops between the power and ground caused by traces, the

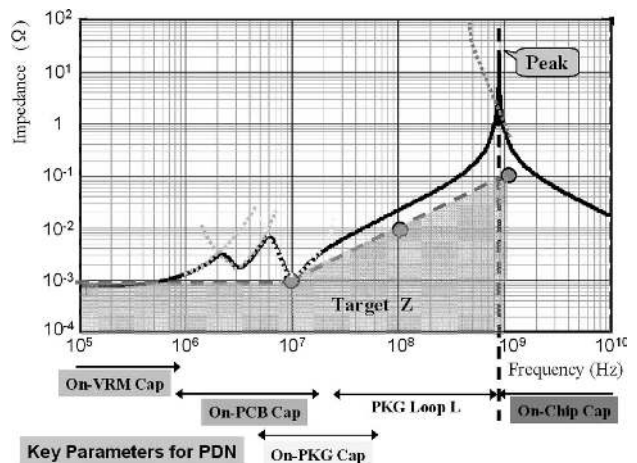


Fig. 4 Impedance profile of PDN.

power plane, chip solder bumps, the ball grid array (BGA) balls, and the decoupling capacitor leads. The key for effectively decoupling the capacitors is minimizing the inductance and resistance elements. In Figure 3, these include R_{pkg1} , R_{pkg2} , L_{pkg1} , L_{pkg2} , R_{pcb1} , R_{pcb2} , L_{pcb1} , and L_{pcb2} . To minimize the impedance profile of a chip, a flip chip PKG is preferred.

Figure 4 shows the impedance profile of the PDN in a circuit simulator with the parameters shown in Figure 3. At low kHz frequencies, the low equivalent series resistance (ESR) of the bulk capacitor in the VRM is used to smooth the output power supply voltage. At middle MHz frequencies, the low equivalent series inductance (ESL) of that capacitor reduces the power and ground bounce. At high GHz frequencies, the on-chip capacitors are used. The on-PCB capacitors are mainly used to remove or shift the plane resonances that are related to EMI. Therefore appropriate capacitors must be selected for the PDN to satisfy the target impedance.

The impedance peak of the mid-frequency resonance is observed around 1 GHz, as shown in Figure 4, which comes from the inductance element (L) on the PKG and the capacitance element (C) in the chip. In general, the chip-PKG LC anti-resonance will be highly sensitive, as explained in the earlier discussion of target impedances.

In contrast, power supply noise is a time-domain event, and therefore transient analysis in the time domain is also important. In general, simplified triangular or trapezoidal waveforms are used to model the switching currents.[7] We assumed three kinds of $\Delta I/\Delta t$ as shown in Figure 5, which are the noise sources (1) 1 A/0.5 ns @ 1 GHz, (2) 10 A/5 ns @ 100 MHz, and (3) 100 A/50 ns @ 10 MHz. We also assumed 10% of the operational power voltage of one

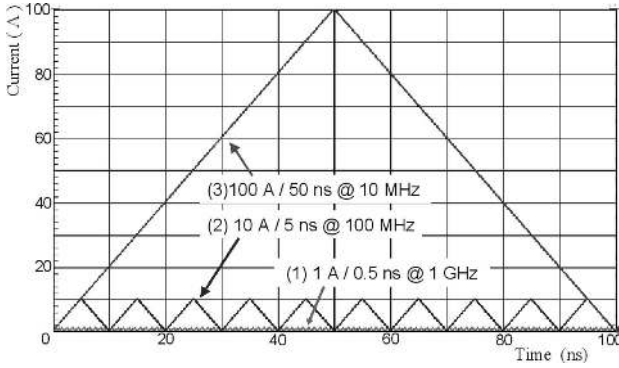


Fig. 5 Current profiles for noise source.

volt (100 mV) based on this circuit simulation. The results in transient noise waveforms are shown in Figure 6, with the worst-case power noise of 403 mV at the noise source (1), which is the closest frequency to the chip-PKG LC anti-resonance.

Figure 7 shows two enhanced impedance profiles from changing the chip's and the PKG's parameters, respectively. To keep the power noise below 100 mV, the chip-PKG LC anti-resonance frequency must be shifted. To improve the chip, the on-chip capacitance (Cchip in Figure 3) is increased from 1 nF to 2.5 nF. For the PKG, the inductance element (Lpkg2 in Figure 3), which also includes the capacitor's ESL, is decreased from 50 pF to 13 pF. Table 1 also summarizes the enhanced parameters for the noise sources (2) and (3).

4. Modelling practice and evaluation for prototype design

To implement the parameters from the circuit simulation in Section 3, we inspected the physical design parameters and modeling method. Instead of a quad flat package (QFP), we used a chip-size package (CSP) and built up a layered structure with micro-via. If a QFP was used, it would be very difficult to meet the target impedance, due to the large inductance of the bonding wire/lead frame and the small number of power pins.

Figure 8 shows a comparison of the two prototype designs. The PCB is a flame retardant -4 (FR-4) board with through-hole via. Both the PKG and PCB use a six-layer structure. The size of the chip and PKG are 5.5 by 5.5 mm and 24 by 24 mm. The sizes of the two PCBs are 125 by 100 mm for Design-A and 62.5 by 50 mm for Design-B.

Figure 9 shows a cross-section of the two designs. The location of the on-PKG capacitors is different. They are on the top layer for Design-A and under the chip in the bottom layer for Design-B. Table 2 shows the capacitance

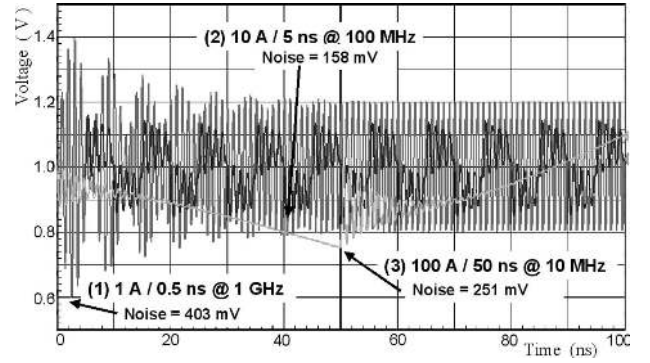


Fig. 6 Simulated transient noise waveform by circuit simulator.

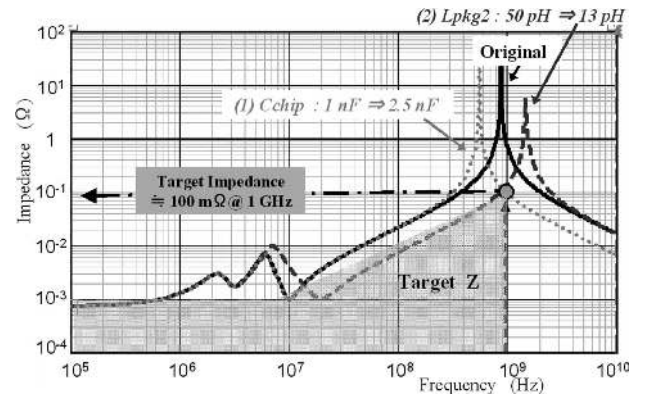


Fig. 7 Enhanced impedance profile for noise source (1) 1 A / 0.5 ns @ 1 GHz.

Table 1 Circuit parameters to satisfy 100 mV of noise voltage.

Circuit parameter in figure 2		Cchip	Rpkg2	Lpkg2	Cpkg
Default value		1 nF	1 mΩ	50 pF	5 uF
Noise Source	$\Delta I/\Delta t$	Frequency			
(1)	1 A/0.5 ns	1 GHz	$\Rightarrow 2.5$ nF	-	-
(2)	10 A/5 ns	100 MHz	-	$\Rightarrow 13$ pF	-
(3)	100 A/50 ns	10 MHz	-	$\Rightarrow 0.2$ mΩ	$\Rightarrow 40$ uF

parameters as mounted on the PDN. The PCB thickness is the same in both cases. A PKG was designed for both designs. The Design-A PKG is 1.46 mm thick with a thick core compared to the 0.5 mm thick PKG with a thin core of Design-B. Both designs have low ESL capacitors on the PKG. However, the simulation results show that the impedance profile of Design-B is much better than Design-A due to the different capacitor locations, the design rules (as shown in Figure 10), and the number of vias (as shown in Table 3). Table 4 shows the parameters that are the sum of the inductances, which include the PKG's parasitic

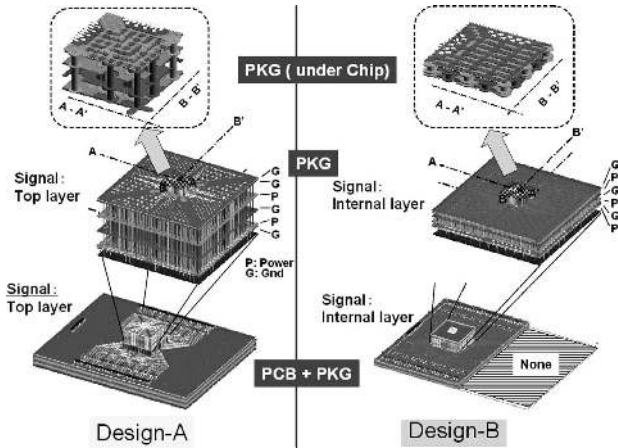


Fig. 8 Prototype design for modeling.

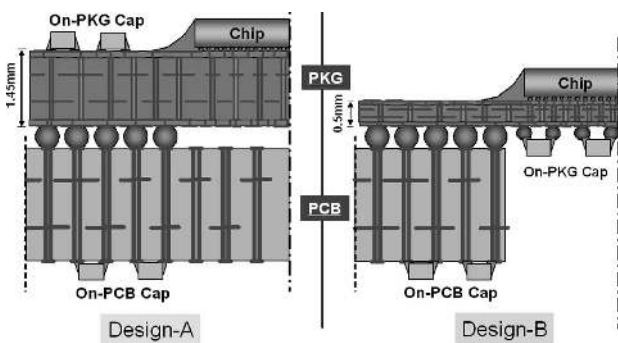


Fig. 9 Cross-section for modeling.

Table 2 Capacitance parameters.

Location	Layer	C (F)	ESL (H)	ESR (Ω)	Qty	Design-A	Design-B
Chip	-	1 n	-	-	1		○
PKG	Top	2.2 u	50 p	5 m	9	○	-
	Bottom					-	○
PCB	Bottom	0.1 u	430 p	2.6 m	36		○
	Bottom	470 u	1000 p	5 m	4		○

○: with Capacitor

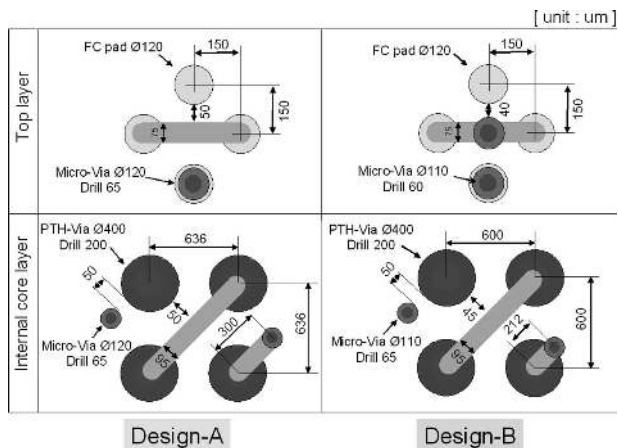


Fig. 10 PKG design rule for prototype.

Table 3 The numbers of bumps, BGAs, and Vias.

Model	Bump	BGA	Via @ PKG	Via @ PCB
Design-A	VDD = 272	VDD = 92	VDD = 92	VDD = 202
	Gnd = 201	Gnd = 156	Gnd = 165	Gnd = 289
Design-B	VDD = 220	VDD = 220	VDD = 241	VDD = 357
	Gnd = 253	Gnd = 220	Gnd = 220	Gnd = 384

Table 4 Extracted circuit parameters for prototype designs based on the 2D solver.

Circuit parameters in figure 2	Rpkg2	Lpkg2	Cpkg
PKG's Parameters to meet target Z @ noise source (1)	1 m Ω	13 pH	5 uF
Design-A	1.2 m Ω (0.6 m Ω @ Cap) (0.6 m Ω @ PKG)	38.9 pH (5.6 pH @ Cap) (33.1 pH @ PKG)	19.8 uF
Design-B	0.6 m Ω (0.6 m Ω @ Cap) (0.02 m Ω @ PKG)	6.7 pH (5.6 pH @ Cap) (1.1 pH @ PKG)	19.8 uF

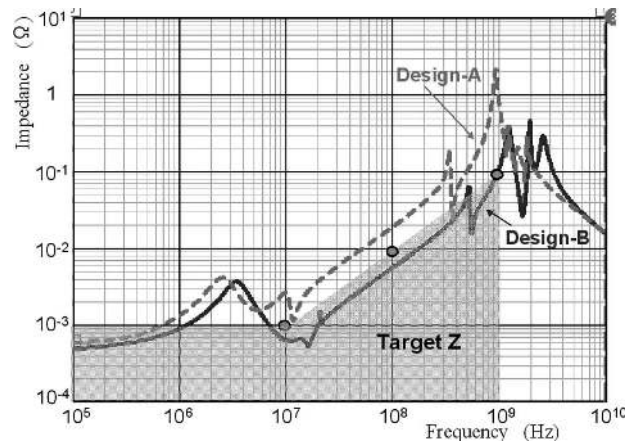


Fig. 11 Simulated impedance profile for prototype designs based on the 2D solver.

capacitance and the on-PKG capacitor.

To achieve the target impedance with the excitation noise source (1) 1 A/0.5 ns @ 1 GHz from Section 3, the impedance must be less than 13 pH. The inductance of Design-A is 38.9 pH, which is about three times the permissible value, but the inductance of Design-B is 6.7 pH which is about half of the limit. Therefore, this shows the superiority of the source profile of Design-B. We completed the model for the PKG and PCB from the design data and calculated the impedance with the solver. Figure 11 compares the impedances. Design-B satisfies the target impedance for all of the excitation sources.

We also studied the impedance peaks observed around 300 MHz for Design-A and 500 MHz for Design-B. These

are due to the resonance of the PCB and depend on the sizes of the power and ground planes. These peak values don't appear in the simulation results of Figure 4. Therefore, we need to be careful with the resonance profile of the PCB. Table 5 shows the simulation results and target impedance for each excitation noise source.

Even though Design-B meets the target for impedance in all cases, its noise voltage is 132 mV over the permissible voltage with the excitation noise source (3) 100 A/50 ns @ 10 MHz. This is caused by the anti-resonance between the inductance of the capacitors on PCB. Therefore, it is necessary to use transient analysis to check if the noise voltage is below the allowed power noise voltage.

Therefore, if all of the capacitors in the bottom layer of the PCB are increased from 0.1 uF to 22 uF, the impedance peak at low frequency will be reduced as shown in Figure12 (Design-B1). The results of the transient analysis show the worst noise voltage will be decreased from 132

Table 5 Target impedance and simulation results for prototype design.

Noise source	(1)	(2)	(3)
Frequency	@ 1 GHz	@ 100 MHz	@ 10 MHz
Target Z	100 mΩ	10 mΩ	1 mΩ
Design-A	1 Ω	18 mΩ	2.5 mΩ
Design-B	95 mΩ	5 mΩ	0.6 mΩ
$\Delta I/\Delta t$	1 A/0.5 ns	10 A/5 ns	100 A/50 ns
Allowed noise voltage	100 mV		
Design-A	269 mV	165 mV	217 mV
Design-B	64 mV	42 mV	132 mV

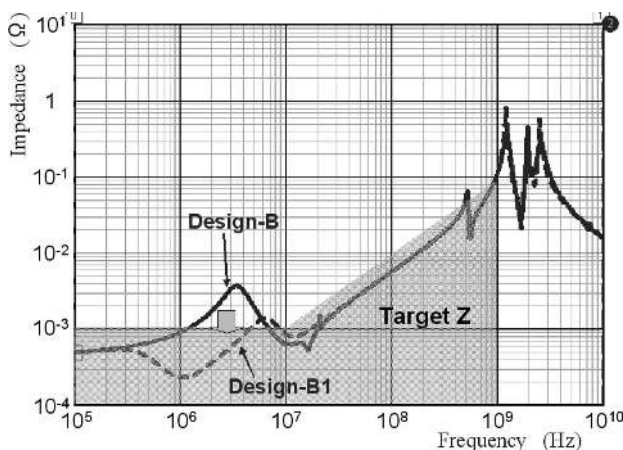


Fig. 12 Simulated impedance profile for prototype designs improving at low frequency based on the 2D solver.

mV to 75 mV, which meets the noise criteria.

Figure 13 shows the transient analysis when all of the current sources are simultaneously active. We assume there is power on/off for noise source (3), I/O switching for noise source (2) and core logic switching for noise source (1). The noise voltage in Design-B1 is 146 mV, which does not meet the noise criteria because of the core logic switching. Therefore, the impedance profile of Design-B1 still needs to be improved at high frequencies. Figure 14 shows the impedance profile when the on-chip capacitance changes from 1 nF (Design-B1) to 10 nF (Design-B2), while the peak resonant frequency is lowered. Finally the noise voltage in Design-B2 is less than 10% of the supply voltage. However, there is still some concern in the 300 to 700 MHz frequency range. Packaging technologies that use capaci-

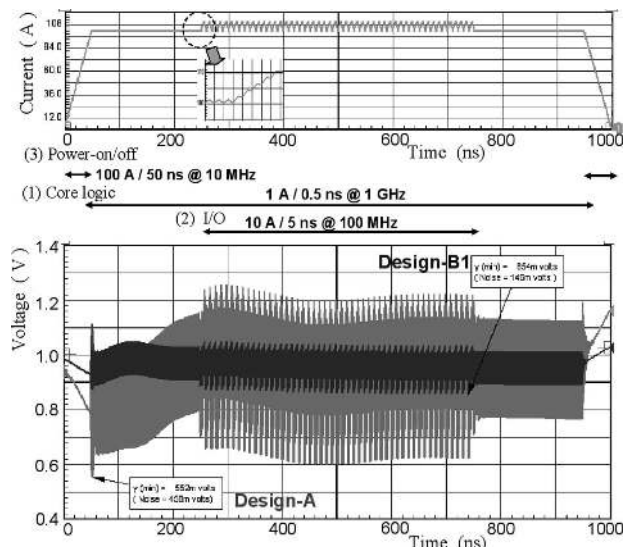


Fig. 13 Simulated transient noise waveform by circuit simulator.

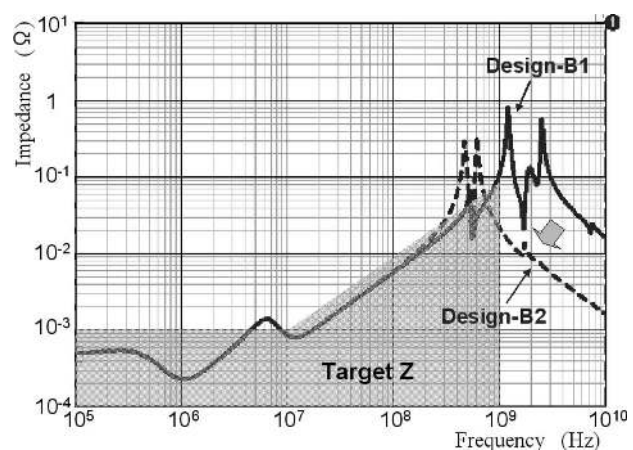


Fig. 14 Simulated impedance profile for prototype designs improving at high frequency based on the 2D solver.

tors embedded in the packages[8, 9] or coreless substrate packages[10] could improve the robustness against power noise.

5. Summary

In this paper, we assumed a chip model that includes the current profile, the on chip capacitance, and the allowed power noise voltage of the PDN, and showed how to specify the target impedance profiles for PDN-equivalent circuits. For the impedance target, the PKG loop inductance tends to become a critical parameter. Also, we designed two prototypes that include a PKG and PCB for a PDN. According to the modeling and evaluation for both frequency and time domain analysis, the PKG design with a small ESL capacitor in the bottom layer with a thin core structure is superior to using a capacitor in the top layer.

If the target impedance is to be controlled more rigidly, then the PDN model must include detailed design information for the chip. However, during a real-life development phase, it is very difficult to get modeling data that includes such confidential information. This is one of the problems that co-design and co-simulation helps to address.

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