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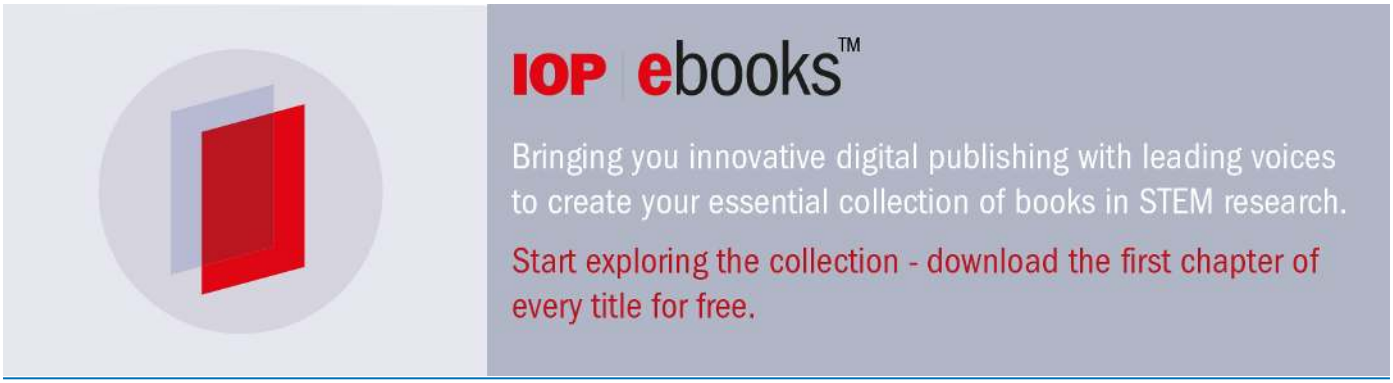

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Analysis of current mirror circuits designed with line tunnel FET devices at different temperatures

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Abstract

The goal of this work is to study the performance of current mirror circuits designed with line tunnel field effect transistor (TFET) devices and compare the suitability of this technology with alternatives such as point TFETs and FinFETs. Experimental results have been obtained at room and high temperatures and the analyses focused on parameters such as the magnitude of the on-state current and the sensitivity of the current transfer ratio to channel dimensions mismatch and to the temperature. Line TFETs exhibited higher on-state current than point TFETs, in spite of a higher susceptibility to the channel length. When band-to-band tunneling prevails for both input and output transistors, the current transfer ratio with line TFETs presented a nearly linear dependence on the temperature due to bandgap narrowing. This way, a general equation of the current transfer ratio for circuits designed with the three highlighted technologies is proposed. Globally, it was observed that, unless a very low sensitivity to channel length mismatch is required, line TFET devices are a very suitable alternative for current mirror circuits, since this technology provides much higher on-state currents than point TFETs, and at the same time it is much less sensitive to temperature variations than FinFET transistors.

Keywords: TFET, FinFET, temperature impact, current mirror, analog circuits

(Some figures may appear in colour only in the online journal)

Introduction

As the most recent technological nodes reach the nanoscale domain, some undesirable phenomena, such as short channel effects and leakage current become major issues [1, 2]. Since supply voltage and power dissipation have not been scaled down accordingly [3], new device concepts have been studied for low power applications, such as the tunnel field effect transistors (TFETs) [4–6].

TFETs are based on a gate-controlled p–i–n diode structure, with drift-diffusion transport being replaced by band-to-band tunneling (BTBT), which enables subthreshold swing (SS) values lower than 60 mV/decade at room temperature [7, 8]. Lower parasitic capacitance and improved saturation behavior have also been reported as advantages of this technology [9, 10]. Experimental measurements of point tunneling transistors, however, revealed that the undesirable impact of trap-assisted tunneling (TAT) in the OFF-state often prevented the devices from reaching sub-60 mV/decade SS [11, 12].

In order to tackle not only this SS degradation but also the low values obtained for ON-state currents, line tunnel FET structures have been widely discussed in the literature [13–15]. This new class of devices presents a source/gate

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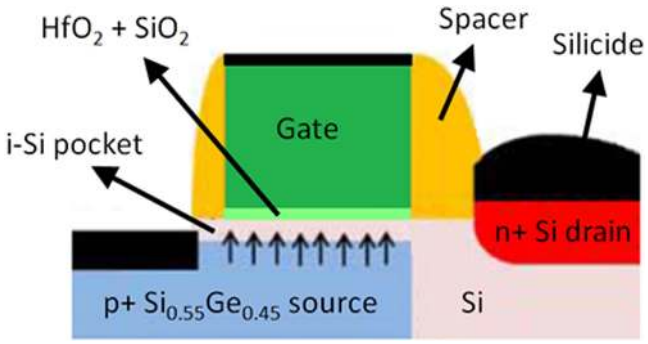

Figure 1. Line tunnel FET structure.

overlap, in a way that the direction of tunneling becomes aligned with the gate electric field [16, 17]. As a consequence of this design, line TFETs enhanced drive current varies proportionally to the gate length, while the point tunnel FETs poor one is basically unaffected by this parameter [18, 19].

Considering the mentioned advantages of TFETs individual behavior, recent studies haves shown how basic circuits may be improved as well [20–22]. Digital configurations such as inverters and multiplexers have been analyzed, with a vast majority of studies based on simulations [23, 24], but also a few with experimental data [25, 26]. Meanwhile, some analog designs have been proposed with simulation approaches [27, 28].

Among many interesting digital and analog applications, this is the first paper to evaluate the performance of line tunnel FET technology in analog circuits with experimental results. The impact of the device dimensions and the temperature on a widely used circuit block, namely a current mirror, has been analyzed in this study. Initial results of current mirrors designed with point tunneling devices and FinFETs have been published in [29]. This work compares the results obtained for three different technologies and extends the conclusions on the suitability of each of them in current mirror circuits.

Device characteristics

The measurements have been performed with devices fabricated on 300 mm silicon-on-insulator wafers at imec/Belgium. The transistors have been designed with Si/SiGe heterojunction, since the performance is known to be enhanced due to the lower bandgap at source [30]. These line-nTFETs present a thin intrinsic silicon pocket layer on top of a p-type $Si_{0.55}Ge_{0.45}$ source extending under the gate. An undoped Si channel separates the source and drain regions.

Regarding the gate stack, there is 1 nm of interfacial SiO_2 followed by layers of HfO_2 (1.8 nm) and TiN (2 nm). Subsequently p-doped amorphous silicon is deposited. This study evaluates transistors with a channel width of 60 nm, 70 nm and 130 nm, and a channel length of 130 nm and 1000 nm, respectively.

A schematic structure of a line tunnel FET is shown in figure 1. More details can be found in [30].

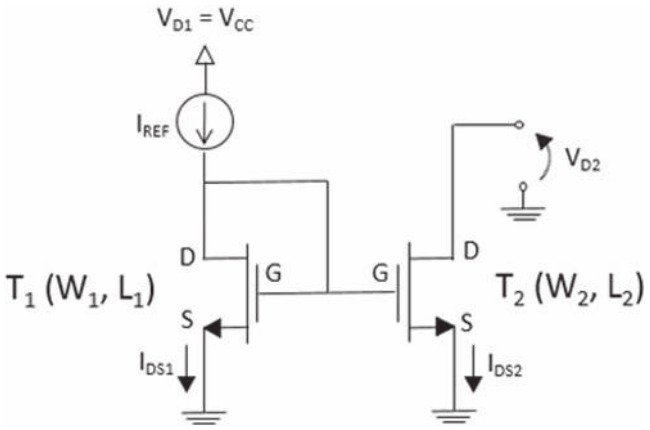

Figure 2. Current mirror circuit.

The working principle of this structure relies on the potential well in the conduction band of the pocket as a result of an increasing gate bias. This way, tunneling starts as soon as the lowest sub-band in the conduction band of the pocket aligns with the valence band of the source. The electrons are then collected by the positively biased drain, with the current magnitude increasing proportionally with both the channel length and width.

Results and analysis

The studied circuit is schematically represented in figure 2. The input transistor drain is connected to a current source, resulting in a gate-source voltage ($V_{GS1} = V_{GS2}$) ranging from 1.2 to 1.8 V. While for the input device $V_{DS1} = V_{GS1}$, the output transistor drain voltage ranges from 0 to 1.5 V. The output and input drain current ratio (I_{DS2}/I_{DS1}) has been investigated as a function of device dimensions, bias condition and temperature.

Analysis of the current mirror circuit at room temperature

Measurements have been performed with 4 different line TFETs, with channel width ranging from 60 to 105 nm and a channel length either 130 or 1000 nm. Figures 3 and 4 illustrate the transfer curves, exhibiting the drain current as a function of gate voltage for V_{DS} of 0.6 V and 1.5 V and the drain current as a function of drain voltage for V_{GS} of 1.2 V and 1.8 V, respectively.

As explained in previously, the drain current is expected to be proportional to the channel area, similar to the results shown in figures 3 and 4. This behavior differs from point tunneling devices, in which the local tunneling is perpendicular to the gate electric field, making them basically not affected by the channel length [5, 18, 19]. This channel length impact on line TFETs differs also from the FinFET dependency, since the prevailing drift/diffusion mechanism makes the current decrease for longer channels. It is worth mentioning that the listed values correspond to the mask dimensions. Besides, the drain voltage does not affect the drain current for higher values of the gate voltage.

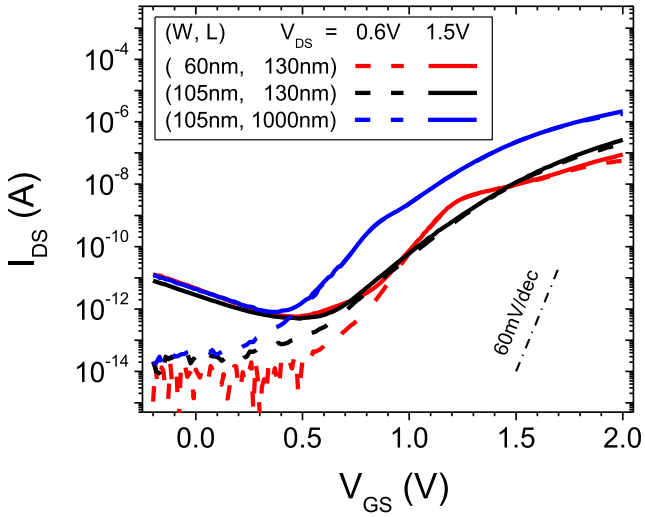

Figure 3. Drain current as a function of V_{GS} for line TFETs with different values of channel length and width.

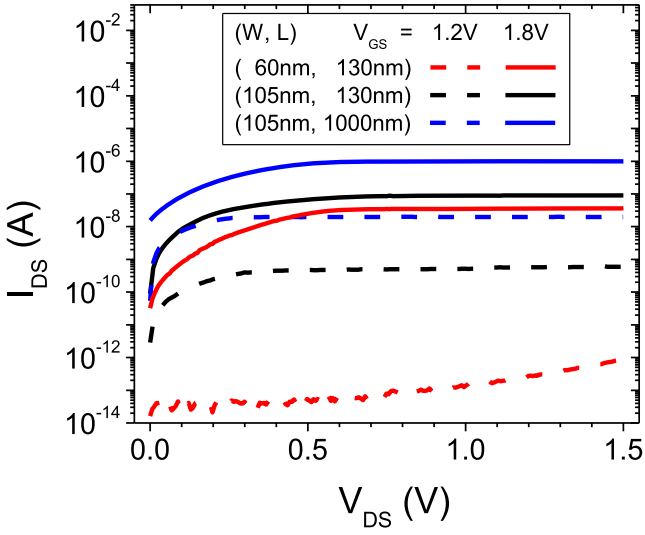

Figure 4. Drain current as a function of V_{DS} for line TFETs with different values of channel length and width.

Therefore, considering the working principle for each of the three structures, the on-state current can be expressed by the generic equation (1), as a function of the effective values of channel width (W_{ef}) and length (L_{ef}). The introduced parameter m is -1 for a line TFET, 0 for a point TFET and $+1$ for a FinFET. These expressions neglect the early effect, drain induced barrier thinning and other short channel effects. The different values of m will give rise to length dependence for the current mirrors designed with each technology.

$$I_{DS} \propto \frac{W_{ef}}{L_{ef}^{m}}, \tag{1}$$

where:

$$m_{\text{Line TFET}} = -1;\ m_{\text{Point TFET}} = 0;\ m_{\text{FinFET}} = 1.$$

Based on this equation and on the results presented in [29], it is possible to reaffirm a major advantage for line tunnel FET devices, namely the increased on-state current when

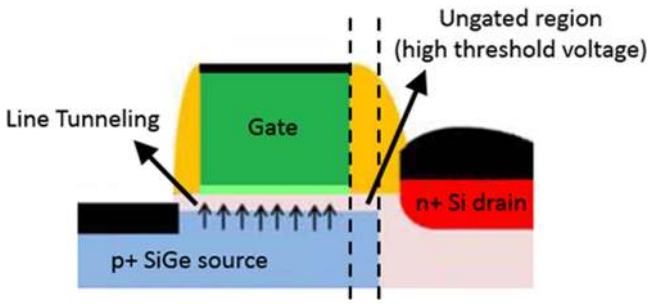

Figure 5. Basic structure of a line tunnel FET structure with an ungated channel region [30].

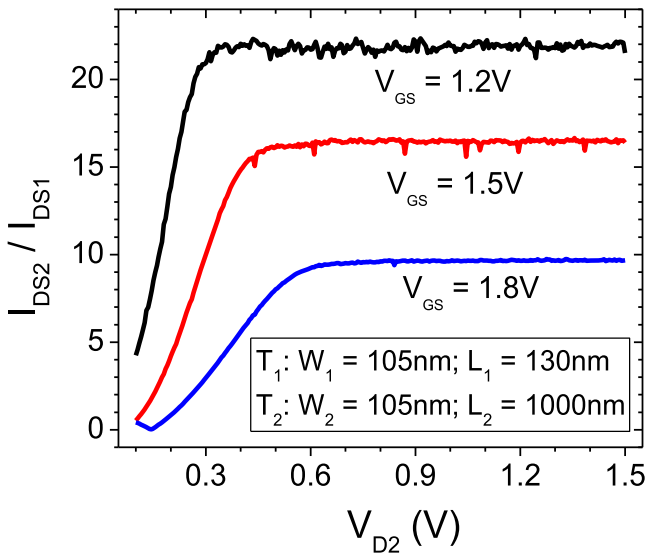

Figure 6. Current transfer ratio as a function of V_{D2} for different values of gate voltage.

compared to point TFETs with similar dimensions, in contrast to its mentioned disadvantage related to the channel length dependence.

Another interesting behavior is observed in the shape of the curves for the transistor with $W = 60$ nm and $L = 130$ nm in figure 3. This is possibly due to an effective structure represented in figure 5. As detailed in [30], an abrupt variation in the drain current slope may be critically affected by the gate-source alignment. If the source edge extends beyond the gate edge, the weakly gated source region presents a high threshold voltage, leading to a decrease in the on-state current. It is important to compare the slope of the drain current for devices intended to be used in current mirror circuits, since this will explain the dependence of the current transfer ratio (I_{DS2}/I_{DS1}) on the bias condition.

Figure 6 shows the obtained results of current transfer ratio (I_{DS2}/I_{DS1}) when the output drain voltage ranges from 0 to 1.5 V. Different I_{REF} values have been used, so that the gate voltage ranged from 1.2 to 1.8 V.

As expected from the results showed in figures 3 and 4, an increase in the reference current (and the consequent increase in V_{GS}) results in lower values of the I_{DS2}/I_{DS1} plateau. Meanwhile, higher values of gate voltage require

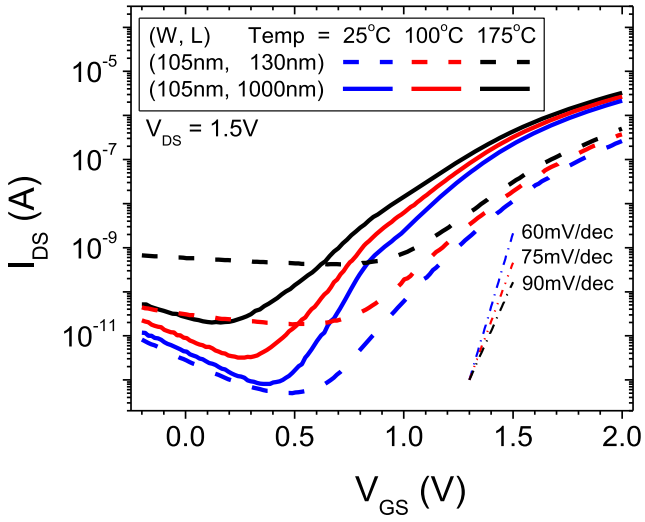

Figure 7. Drain current as a function of V_{GS} for line TFETs with different temperatures and dimensions.

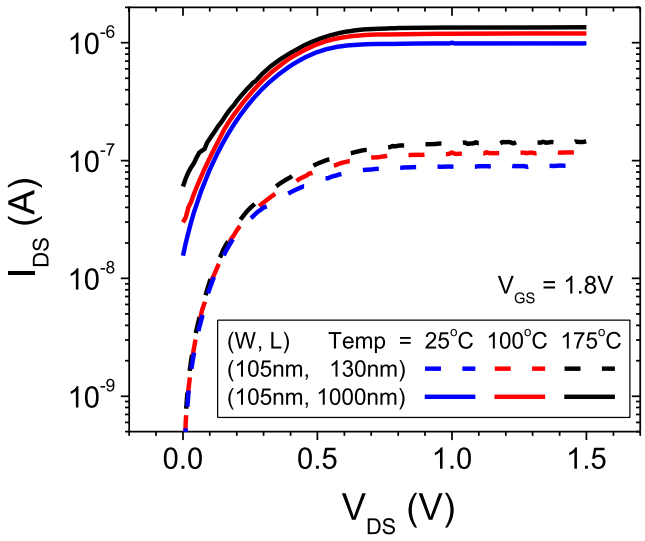

Figure 8. Drain current as a function of V_{DS} for line TFETs with different temperatures and dimensions.

higher V_{D2} values to saturate the output transistor, causing the narrowing of the operation region.

Analysis of the current mirror circuit for temperatures ranging from 300 to 450 K

The susceptibility of the transfer curves to the temperature is shown in figures 7 and 8. The obtained data refer to the same devices used in the current mirror circuit illustrated in figure 6, for three different temperatures.

Based on the temperature impact obtained for the studied devices, the next step consists of extracting the activation energy for each of them to investigate the dominant transport mechanism for different bias conditions. The activation energy values for V_{GS} ranging from 0.6 to 1.8 V are shown in figure 9.

BTBT is considered to dominate when $E_A < 0.1$ V, while TAT prevails otherwise [31]. Therefore, in order for all

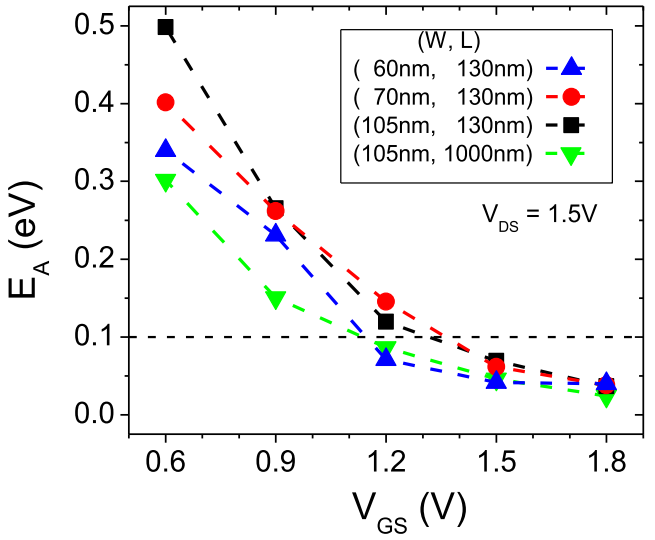

Figure 9. Activation energy as a function of V_{GS} for line TFETs with different values of channel length and width.

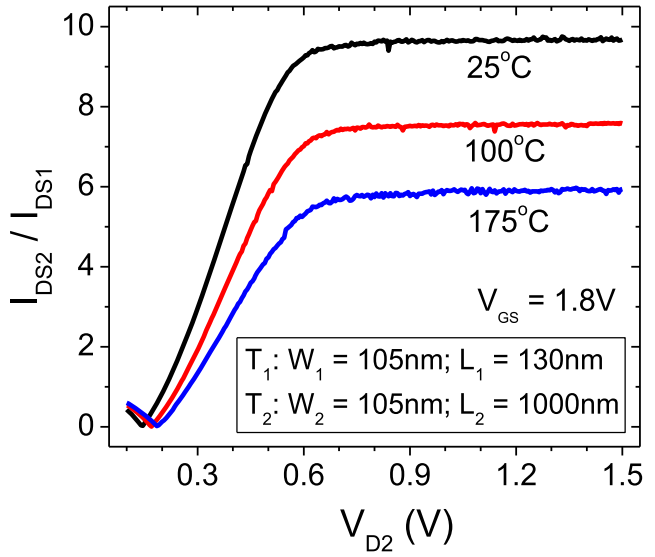

Figure 10. Current transfer ratio as a function of V_{D2} for different temperatures.

the studied devices to be clearly dominated by BTBT, the bias condition of $V_{GS} = 1.8$ V has been chosen for the next steps of the analyses.

Figure 10 exhibits the results for the same pair of devices used in the current mirror circuit reported in figure 6. When the temperature increases, the current transfer ratio plateau decreases, since the activation energy of the input transistor is slightly bigger than the one for the output device. The operation range in terms of V_{D2} is not affected by the temperature.

Finally, figures 11 and 12 show the results of the I_{DS2}/I_{DS1} plateau obtained for current mirror circuits designed with devices with different dimensions and operating under different temperatures.

For all the studied circuits, there was a closely linear negative trend of current transfer ratio with the temperature. The negative trend may be explained based on the difference in

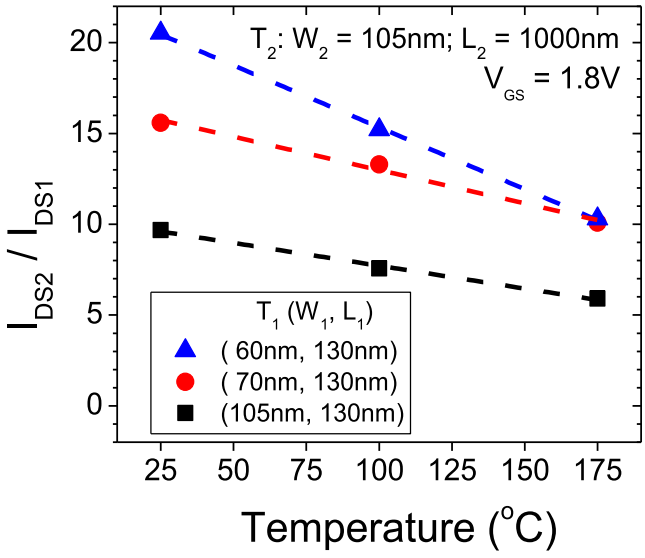

Figure 11. Current transfer ratio as a function of temperature for different input transistor dimensions.

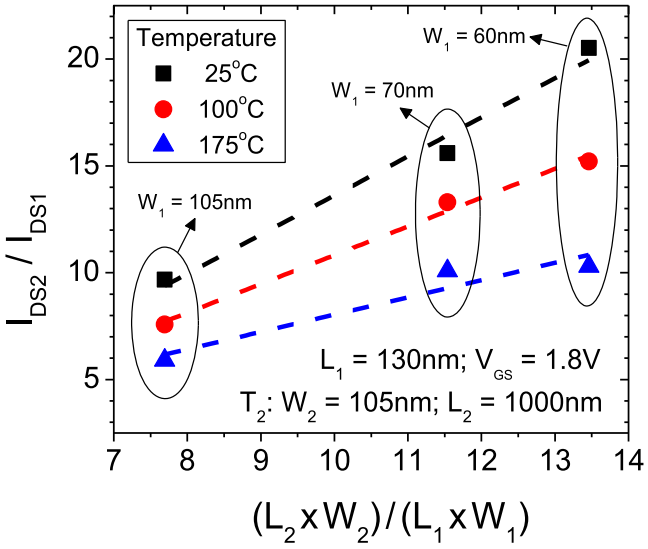

Figure 12. Current transfer ratio as a function of output and input channel area ratio for different temperatures.

the activation energy, as shown in figure 9. For $V_{GS} = 1.8$ V, the device with channel length of 1000 nm and channel width of 105 nm is exactly the one with the lowest value of E_A. Considering that this is the output transistor for the three studied circuits (T_2), when the temperature increases, the input current presents a stronger rise than the output one, leading to a decrease in I_{DS2}/I_{DS1} ratio. The slope in such an analysis increases with larger differences in the activation energy.

Meanwhile, the approximately linear behavior comes from the prevailing transport mechanism. Since BTBT dominates both input and output devices, the variations are basically explained due to the band gap (E_g) narrowing for higher temperatures. Equation (2) gives the BTBT susceptibility to E_g [32], which is graphically shown in figure 13 as a function of temperature. The linear temperature dependence is rather

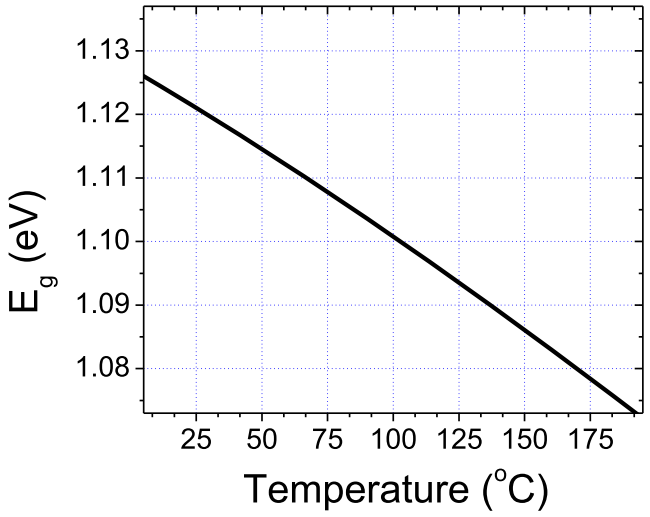

Figure 13. Silicon band gap as a function of the temperature.

limited in the studied temperature range.

$$I_{BTBT} \propto e^{(-k.E_g{}^{3/2})}. \quad (2)$$

Regarding the channel area impact, figure 12 reassure the previously explained dependence of line tunnel FET devices to its dimensions, with a closely linear positive trend of I_{DS2}/I_{DS1} ratio with the respective channel area ratio. Some deviations from the expected curves are caused by differences between the effective and the mask dimensions and by non-ideal structures as shown in figure 5.

Therefore, it is possible to compare the results obtained for current mirrors designed with line tunnel FET with the ones for point TFETs and FinFETs, previously studied in [29]. The current transfer ratio can be expressed by equation (3), where m is -1 for line TFET, 0 for point TFET and $+1$ for FinFET. The fitting parameter p is related to the activation energy of T_1 and T_2, being one if $E_{A1} = E_{A2}$.

$$\frac{I_{DS2}}{I_{DS1}} = p\,(E_{A1}, E_{A2})\,.\,\frac{W_{ef2}/L_{ef2}^{m}}{W_{ef1}/L_{ef1}^{m}}, \quad (3)$$

where:

$$m_{\text{Line TFET}} = -1;\ m_{\text{Point TFET}} = 0;\ m_{\text{FinFET}} = 1.$$

Comparing the suitability of these three technologies to design current mirror circuits, table 1 sums up the advantages presented by each of them in terms of susceptibility to channel length mismatch, susceptibility to temperature variations and magnitude of the on-state current.

As a conclusion, it can be stated that in spite of the susceptibility to channel length mismatch, line TFET technology could overcome relevant issues observed in circuits designed with FinFETs and point TFETs, as mentioned in the Introduction section. After all, it was possible to obtain a combination of high on-state current, typical for FinFET transistors, and low dependence on the temperature, a very important characteristic of tunneling devices.

Table 1. Features presented by current mirrors designed with FinFET, point TFET and line TFET devices.

	FinFET	Point TFET	Line TFET
Low susceptibility to channel length mismatch		✓	
Low susceptibility to the temperature		✓	✓
High on-state current	✓		✓

Conclusions

This work studied the performance of current mirrors designed with line TFET devices. The analyses evaluated the results for different temperatures and dimensions, leading to an overall conclusion on the suitability of line TFETs, point TFETs and FinFETs for the design of such a circuit.

The first part highlighted the experimental data obtained at room temperature. Based on the line TFET working principle, the input and output characteristic curves have been explained. A general equation of drain current as a function of effective dimensions has been presented and used to predict the impact of device mismatching on the current mirror circuit. Regarding the bias condition, increasing the input transistor drain voltage required a higher output bias to reach the current transfer ratio plateau, narrowing the operation region.

In the second part, the temperature impact has been scrutinized. In order to compare the dominant transport mechanisms for each transistor, the activation energy has been plotted for a varying gate voltage and the condition of $V_{GS} = 1.8$ V has been chosen, in a way that BTBT could prevail for all the devices. Even with the same transport mechanism, the slight difference in the activation energy value resulted in a higher susceptibility of the circuits to the temperature. Higher temperatures caused a nearly linear decrease in the current transfer ratio, with a slope depending on the input and output E_A difference. The experimental results for circuits with different dimensions leads to a general equation for the current transfer ratio as a function of the effective input and output channel length and width.

Taking all the results into consideration, it is possible to compare the advantages and disadvantages of current mirrors designed with different technologies. If this circuit is expected to be used in an application with a high sensitivity to channel length mismatch, point TFET devices would be the best option, with the disadvantage of presenting a low on-state current. On the other hand, other applications should consider line TFETs as the most suitable alternative, since they combine a low susceptibility to the temperature provided by BTBT with a high on-state current found in conventional technologies. In other words, this work showed how line TFET technology is a quite promising technology for a very relevant analog circuit.

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