Digital Object Identifier (DOI): 10.1109/TPEL.2017.2704293

IEEE Transaction on Power Electronics (Volume: 33, Issue: 4, April 2018)

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Suggested Citation

Y. Ko, H. Jedtberg, G. Buticchi and M. Liserre, "Analysis of DC-Link Current Influence on Temperature Variation of Capacitor in a Wind Turbine Application," in *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 3441-3451, April 2018.

Analysis of DC-Link Current Influence on Temperature Variation of Capacitor in a Wind Turbine Application

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***Abstract*—Back-to-back converters for wind turbine systems feature capacitors in the dc-link to maintain a stable voltage and to decouple a generator from the electric grid. The electrolytic capacitors are typically chosen for their advantages; a higher energy density and a higher capacitance at lower costs. Long-term field experiences and recorded failure data revealed that the capacitors are one of the most frequent failure reasons for the wind turbine system. The current profile of the capacitors is highly responsible for this degradation, since it determines the dissipated power of the capacitor. This paper analyzes the actual current profile in the dc-link capacitor of a back-to-back converter for wind turbine application. A power converter is also designed to generate sinusoidal current at arbitrary frequency and arbitrary dc bias voltage for testing purposes. The experimental results confirm that the proposed power converter enables us to derive the correlation between the current frequency and the temperature variation of capacitor.**

***Index Terms*—Back-to-back converter, electrolytic capacitor, reliability, wind turbine, ripple current stress.**

I. Introduction

HIGH reliability has become the most important requirement for wind turbine installation, in order to reduce maintenance costs and ensure a high system availability. The failures are mostly located in the power converter part and the capacitors are responsible for 60% of the failures [1]–[3]. Therefore, condition monitoring methods have been proposed to evaluate the capacitor health status by estimating the internal parameters [4]–[7]. Furthermore, the useful lifetime estimation methods have been proposed in [8]–[11] for a scheduled maintenance, which are based on the lifetime model derived by the Physics of Failure approach [12], [13].

On the other hand, core temperature is the most influencing factor for the capacitors lifetime [14]–[17], and it depends on the ambient as well as the power losses inside the capacitor, which are depending mainly on the current profile. Therefore, many research works investigated the current spectrum [18]–[21] and the current reduction by synchronization of carrier signals in a back-to-back converter [22], [23]. However, a clear correlation between the current harmonics and the lifetime (or core temperature variation) in such research works is still missing.

After analyzing the capacitor current spectra under different operating conditions, this paper proposes a power converter to perform capacitor testing. The idea is to individuate via simulations the capacitor current spectrum and to reproduce them with the realized test setup. To define the frequency range, the dc-link capacitor current in the two-level back-to-back converter is identified, with consideration of different power and power factors in Section II. Then, in Section III, the impact on the lifetime is discussed taking the typical model of electrolytic capacitor to highlight the motivation. Before demonstrating the temperature variation in Section V, the power converter is proposed to inject sinusoidal current at various frequencies, which are obtained based on a real operation, to the capacitor under test (CUT) in Section IV. The challenge in its design is to achieve a low total harmonic distortion (THD) to derive further clear correlation. Moreover, it is as well required to control the bias voltage on the CUT; the parallel control strategy is proposed and verified by the experimental results. Finally, this paper is concluded in Section VI.

II. Analysis of DC-Link Capacitor Current in Back-to-Back Converter

In this section, the dc-link capacitor current is identified in accordance with operating points to provide the information of the current spectrum. The capacitor current ($i_{\mathrm{link},c}$) can be calculated by the subtraction between the machine-side current ($i_{\mathrm{link},m}$) and the grid-side current ($i_{\mathrm{link},g}$) as (1), considering the two-level back-to-back converter shown in Fig. 1

$$i_{\mathrm{link},c}(t) = i_{\mathrm{link},m}(t) - i_{\mathrm{link},g}(t) \tag{1}$$

where the subscript c denotes the capacitor-side, the subscript m is the machine-side, and the subscript g is the grid-side. Then, referring [18], the capacitor current can be mathematically expressed as (2), shown at the bottom of the next page. The

Manuscript received October 17, 2016; revised March 30, 2017; accepted May 6, 2017. Date of publication May 15, 2017; date of current version January 3, 2018. This work was supported in part by the European Union/Interreg V-A—Germany-Denmark under PE:Region Project and in part by the Gesellschaft für Klimaschutz Schleswig-Holstein GmbH within the framework of the "LIFE-WIND" project. This paper was presented in part at the *IEEE Applied Power Electronics Conference and Exposition*, Long Beach, CA, USA, March 20–24, 2016. Recommended for publication by Associate Editor P. Bauer. *(Corresponding author: Youngjong Ko.)*

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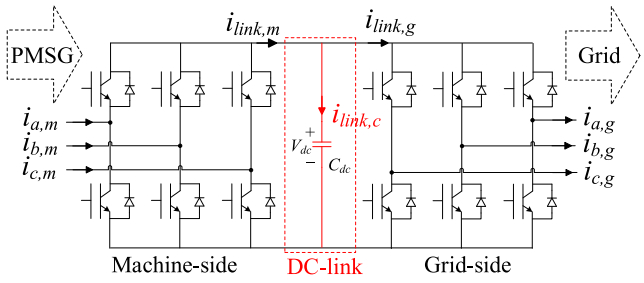


Fig. 1. Two-level back-to-back converter used as a case study.

derivation of machine- and grid-side equations is also presented in Appendix B.

In the following analysis, the three currents ($i_{\text{link},m}$, $i_{\text{link},g}$, $i_{\text{link},c}$) of 2 MW wind turbine, whose specification is shown in Table A-1 (see Appendix A), is simulated under four operating points in Table II (see Appendix A). It is assumed that the carriers of machine- and grid-side are synchronized to cancel the first harmonics of switching frequency as well as the power factor of the machine-side is set to 0.98 since no magnetizing current needs to be provided to permanent magnet synchronous generator (PMSG) [24], [25].

On the other hand, the power factor of the grid-side could be controlled within a defined boundary by the German grid code [26], [27]. Following the definition of variant 1, the boundary of the power factor angle in the grid-side, which is presented in (3), is considered

$$-48.99^\circ \leq \varphi_{0,g} \leq 67.38^\circ. \tag{3}$$

The current waveforms of the machine-, grid-, and capacitor-side under the operating point 2 (see Table A-2 in Appendix A) are simulated in Fig. 2, along with their harmonic spectrum. Focusing on the harmonic spectrum, while the machine- and grid-side current contain both low-order harmonics and high-order harmonics as shown in Fig. 2(a) and (b), it can be observed that the harmonics of the capacitor-side current are dominantly distributed at high-order harmonics, as shown in Fig. 2(c).

In Fig. 3, the harmonics variation of the capacitor current is shown in accordance with the operating point (generated power) and the power factor of the grid-side. The harmonics amplitude accordingly increases by the increased power as shown in Fig. 3(a). Fig. 3(b) shows the influence of the power factor on the capacitor-side current spectrum, and the side-band harmonics are increased with the lower power factor.

As a conclusion, the high-order harmonics of around $a \cdot f_s$ mainly affects the lifetime of dc-link capacitors, where the f_s is the switching frequency and the a is the integer.

III. Lifetime Considerations for Electrolytic Capacitors

A. Electrolytic Capacitor Model

A simplified model of an electrolytic capacitor is depicted in Fig. 4, where C is the terminal capacitance, C_D and R_D account for the losses caused by the dielectric, R_0 is the combined constant resistance of terminals, tabs, and foils, respectively, and R_t is the resistance of the electrolyte [28]. It should be

$$\begin{aligned}
i_{\text{link},c}(t) = & \sum_{\eta=1}^{3} I_m \cdot \cos\left(\omega_m t + \varphi_{\eta,m} - \varphi_{0,m}\right) \\
& \left[\frac{1}{2} + \frac{2}{\pi} \cdot \sum_{n=1}^{\infty} \frac{1}{n\left(\frac{\omega_m}{\omega_{sw}}\right)} \cdot J_n\left(n\left(\frac{\omega_m}{\omega_{sw}}\right)\frac{\pi}{2} m_{a,m}\right) \cdot \sin\left(n\frac{\pi}{2}\right) \cdot \cos\left(n\left(\omega_m t + \varphi_{\eta,m}\right)\right)\right. \\
& + \frac{2}{\pi} \cdot \sum_{m=1}^{\infty} \frac{1}{m} \cdot J_0\left(m\frac{\pi}{2} m_{a,m}\right) \cdot \sin\left(m\frac{\pi}{2}\right) \cdot \cos\left(m\left(\omega_{sw} t + \varphi_{\text{pwm},m}\right)\right) \\
& \left. + \frac{2}{\pi} \cdot \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{q} \cdot J_n\left(q\frac{\pi}{2} m_{a,m}\right) \cdot \sin\left((m+n)\frac{\pi}{2}\right) \cdot \cos\left(m\left(\omega_{sw} t + \varphi_{\text{pwm},m}\right) + n\left(\omega_m t + \varphi_{\eta,m}\right)\right)\right] \\
& - \sum_{\eta=1}^{3} I_g \cdot \cos\left(\omega_g t + \varphi_{\eta,g} - \varphi_{0,g}\right) \\
& \left[\frac{1}{2} + \frac{2}{\pi} \cdot \sum_{n=1}^{\infty} \frac{1}{n\left(\frac{\omega_g}{\omega_{sw}}\right)} \cdot J_n\left(n\left(\frac{\omega_g}{\omega_{sw}}\right)\frac{\pi}{2} m_{a,g}\right) \cdot \sin\left(n\frac{\pi}{2}\right) \cdot \cos\left(n\left(\omega_g t + \varphi_{\eta,g}\right)\right)\right. \\
& + \frac{2}{\pi} \cdot \sum_{m=1}^{\infty} \frac{1}{m} \cdot J_0\left(m\frac{\pi}{2} m_{a,g}\right) \cdot \sin\left(m\frac{\pi}{2}\right) \cdot \cos\left(m\left(\omega_{sw} t + \varphi_{\text{pwm},g}\right)\right) \\
& \left. + \frac{2}{\pi} \cdot \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{q} \cdot J_n\left(q\frac{\pi}{2} m_{a,g}\right) \cdot \sin\left((m+n)\frac{\pi}{2}\right) \cdot \cos\left(m\left(\omega_{sw} t + \varphi_{\text{pwm},g}\right) + n\left(\omega_g t + \varphi_{\eta,g}\right)\right)\right]
\end{aligned} \tag{2}$$

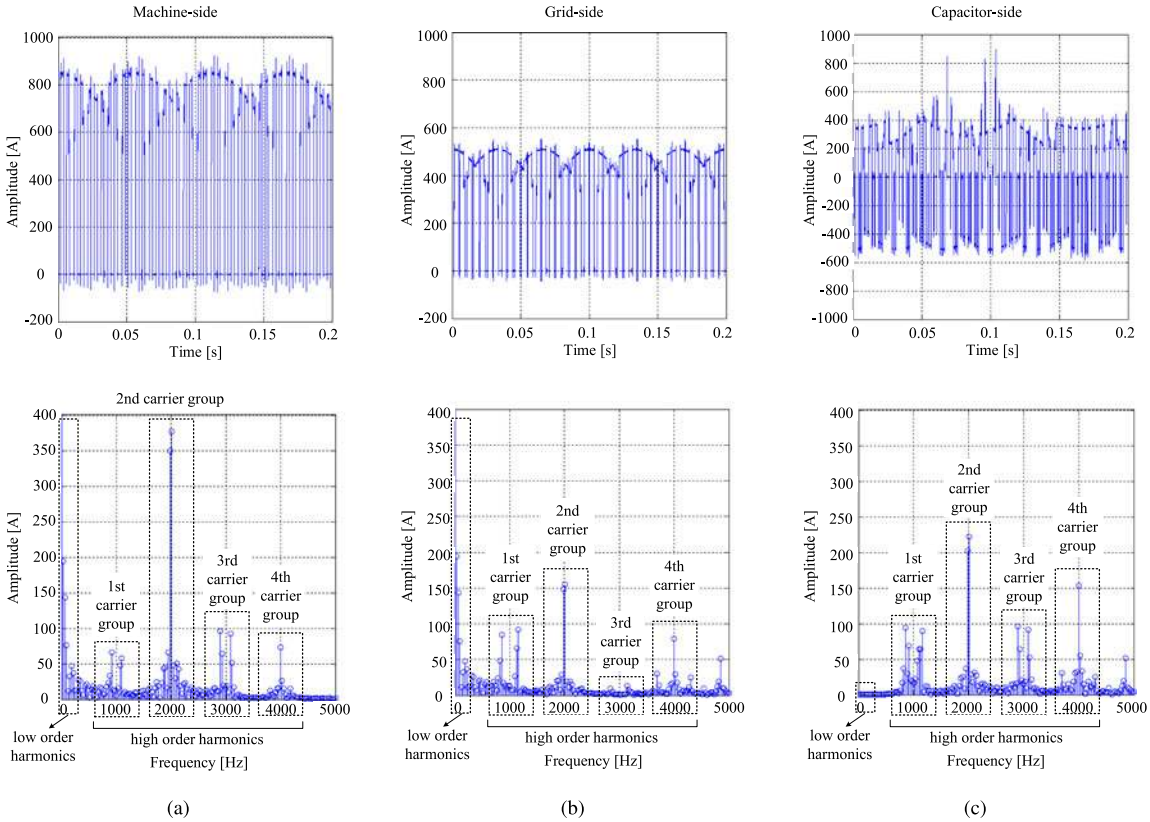


Fig. 2. Simulated current waveform and its harmonic spectrum in (a) machine-side, (b) grid-side, and (c) capacitor under operating point no. 2 of Table II in Appendix A.

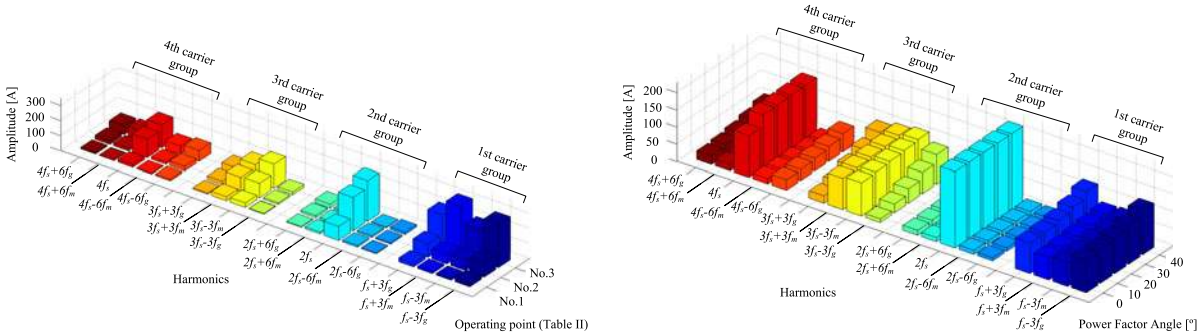


Fig. 3. Harmonics distribution of dc-link capacitor current depending on (a) generated power and (b) power factor angle of grid-side.

noted that the capacitor model is also containing an inductive part in series. For the following analysis, this inductance will be neglected, following the assumption that the capacitor is operated well below its resonance frequency. The equivalent series resistance (ESR) represents the real part of the capacitor's impedance. Therefore, it can be expressed as

$$R_{\text{ESR}} = R_0 + R_f + R_t \tag{4}$$

where R_f represents the frequency-dependent resistance of the dielectric layer, which is composed by C_D and R_D, and R_t is the temperature-dependent part due to the characteristics of the employed electrolyte [17], [28]. Since with increasing temperature the viscosity of the electrolyte changes, its conductivity increases, which in turn leads to a reduction in ESR due to R_t. This effect can be modeled by applying (5), where $R_{t,b}$ is R_t at base temperature T_b, T_s is the hotspot temperature of the capacitor, and SF denotes a capacitor-dependent temperature sensitivity factor [28]

$$R_t = R_{t,b}(T_b) \cdot e^{\frac{T_b - T_s}{SF}}. \tag{5}$$

In Fig. 5, the ESR is plotted against frequency for different temperatures in accordance to [28]. As discussed before, it can

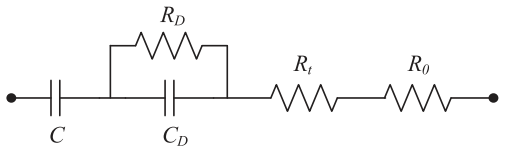


Fig. 4. Equivalent model of electrolytic capacitor.

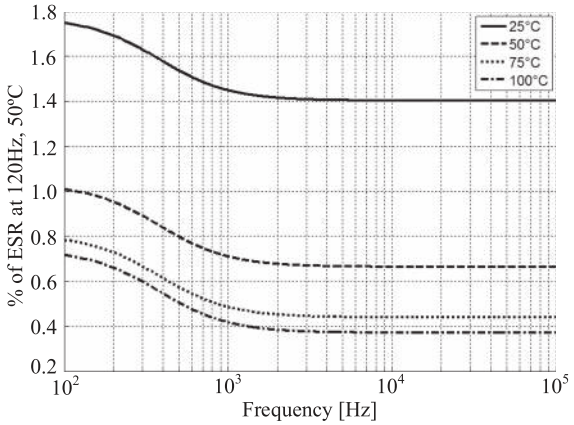


Fig. 5. Variation of ESR with respect to ripple current frequency and temperature [28].

be seen that the ESR decreases as temperature increases. Moreover, it can be noted that increasing frequencies also lead to a decrease in ESR due to R_f.

B. Impact of Capacitor Current on Lifetime

As stated before, the capacitor's current modifies the capacitor's temperature, affecting the lifetime. The hotspot temperature of the capacitor can be estimated by applying (6), where T_a denotes the ambient temperature, ΔT is the additional heating caused by the power dissipation P_d, and the thermal resistance from hotspot to ambient of the capacitor R_{th}

$$T_s = T_a + \Delta T = T_a + P_d \cdot R_{\text{th}}. \tag{6}$$

Since the ESR exhibits a frequency-dependent behavior, for the correct calculation of P_d the knowledge of the RMS capacitor current at the corresponding frequencies is needed [19], [22]. Therefore, the spectral analysis of the previous paragraph can be adopted for the calculation of the different harmonic components. By knowing the capacitor current harmonics, P_d can be calculated by

$$P_d = \sum_{i=1}^{n} I_{R,i}^2 \cdot R_{\text{ESR},i} \tag{7}$$

where $I_{R,i}$ and $R_{\text{ESR},i}$ denote the RMS ripple current and the ESR at frequency harmonic i, respectively, with $i = 1, 2, \ldots, n$

$$L = L_0 \cdot 2^{\frac{T_{\max} - T_a}{10\,\text{K}}} \cdot 2^{1 - \left(\frac{I_a}{I_0}\right)^2 \cdot \frac{\Delta T_0}{A}} \cdot \left(\frac{V_a}{V_0}\right)^{-m}. \tag{8}$$

The lifetime model of an electrolytic capacitor is shown in (8), where L_0 denotes the lifetime at nominal values as given in the manufacturer's datasheets, $T_{\max}$ is the maximum permissible temperature, I_a is the applied capacitor current, I_0 is the rated capacitor current, ΔT_0 is the temperature increase when I_0 is applied, A is the temperature coefficient, V_a is the applied voltage, V_0 is the nominal voltage, and m accounts for the manufacturer-dependent voltage factor as discussed in [29]. The model consists of three parts, where each part is considered as one of the three major stressors. The impact of the ambient temperature follows the Arrhenius rule, which constitutes a doubling in lifetime for each 10 K temperature decrease. Moreover, the applied voltage is taken into account in this model, since an increasing voltage level causes degradation due to electrolyte evaporation effects, which in turn affects the lifetime of the capacitor. As mentioned above, the ripple current is influencing the capacitor's lifetime by acting on the temperature rise ΔT, which is also taken into account in (8). The factor A accounts for the higher impact of ΔT on the lifetime, since it is evaluated experimentally by some manufacturers that the lifetime is bisected by an increase of, e.g., 7–10 K in ΔT [12].

Degradation of the capacitor is not included in (8). Since the heat rise due to the capacitor current causes electrolyte evaporation, it leads to the degradation of the capacitor's parameters, being the ESR and the capacitance C, respectively. As discussed in [30], the ESR will increase with time, whereas C might decrease.

As can be seen from the analysis in Section II, the overall capacitor current is independent from the capacitor parameters. Nevertheless, since the capacitor parameters change over time due to degradation, the lifetime of the capacitor will be affected. An increase in ESR will lead to an increase of the hotspot temperature, which in turn may lead to a faster degradation due to increased electrolyte evaporation. In the case of a dc-link capacitor tank with several branches in parallel sharing the overall current, degradation will still lead to an increasing ESR of the respective capacitor, but since the impedance of the respective branch will increase accordingly, the current sharing within the capacitor tank will change. The current will not be shared equally anymore, but branches with less aged capacitors, and therefore, lower impedance values will carry more current than branches with more aged capacitors. Thereby, the aging of the more stressed capacitors will be increased due to the higher power dissipation and the subsequent increased temperature stress, leading to a reduction in lifetime of the overall capacitor tank. Thus, in order to better understand and predict the lifetime of capacitors employed in dc-link applications, it is necessary to quantify the impacts of mission profile oriented stresses on capacitor hotspot temperature.

IV. Power Converter for Capacitor Test [29]

A. Topology Selection

The power converter in this section aims at injecting the electrical stress to a CUT in order to stress the CUT with sinusoidal currents having different frequencies obtained in Section II.

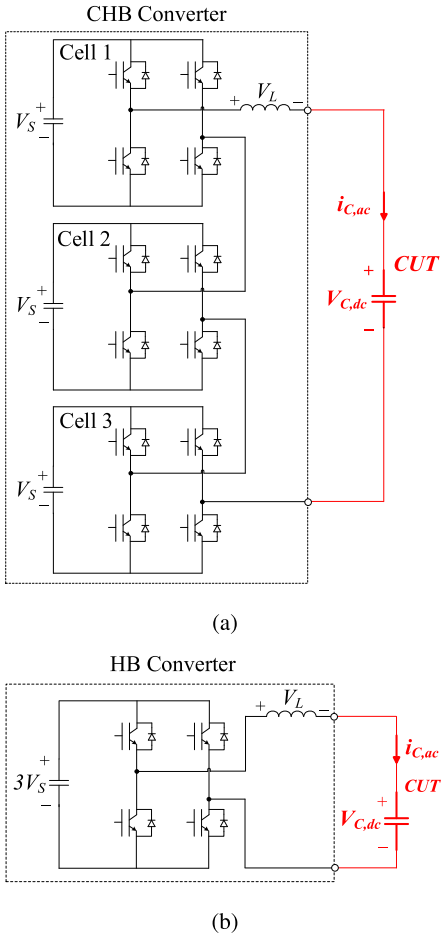


Fig. 6. Possible converters for capacitor test; (a) CHB and (b) HB.

Two possible converters, which are the cascaded H-bridge (CHB) and the H-bridge (HB) shown in Fig. 6, are discussed in terms of structure complexity, THD, filter size, and source voltage. The major challenge is to achieve the given test requirements of the high-frequency sinusoidal currents with a low THD and the high dc bias voltage on the CUT. It is worth noting that the low THD is beneficial to the further clear correlation between the frequency and the temperature variation.

The CHB converter in Fig. 6(a) is composed of three H-bridge cells connected in series, allowing the multilevel output voltage with the six times higher equivalent switching frequency by the phase shifted modulation, and the three times lower source voltage for each cell [31], as shown in Fig. 7(a). These features make the filter inductance to be reduced (by the multilevel voltage and the high equivalent switching frequency) and the commercially available switching devices to be acceptable to generate the high dc bias voltage on the CUT (by the lower source voltage of each cell). On the other hand, the HB converter in Fig. 6(b) is considered for the system complexity point of view, since this can be realized with $1/3$ less number of switching devices and voltage sources in comparison with the CHB converter; nevertheless, the advantages of the CHB converter cannot be matched by the HB converter, as shown in Fig. 7(b).

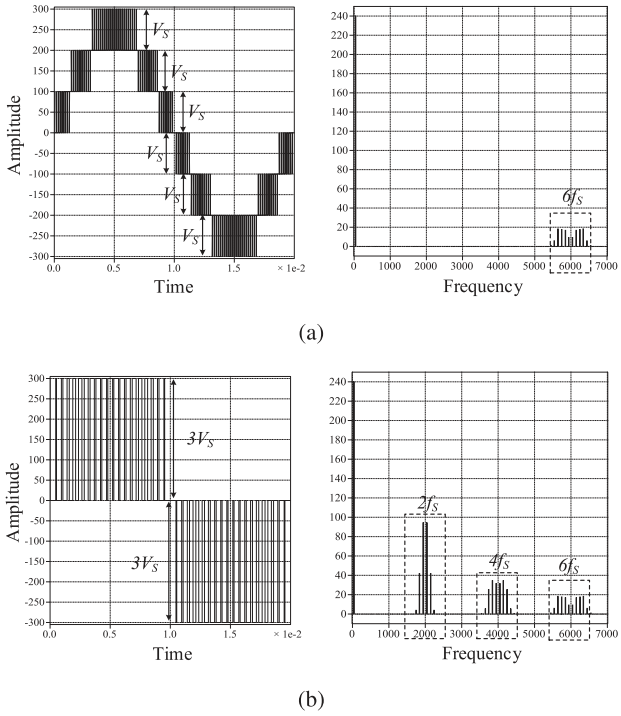


Fig. 7. Output voltage and its harmonic spectrum of (a) CHB and (b) HB.

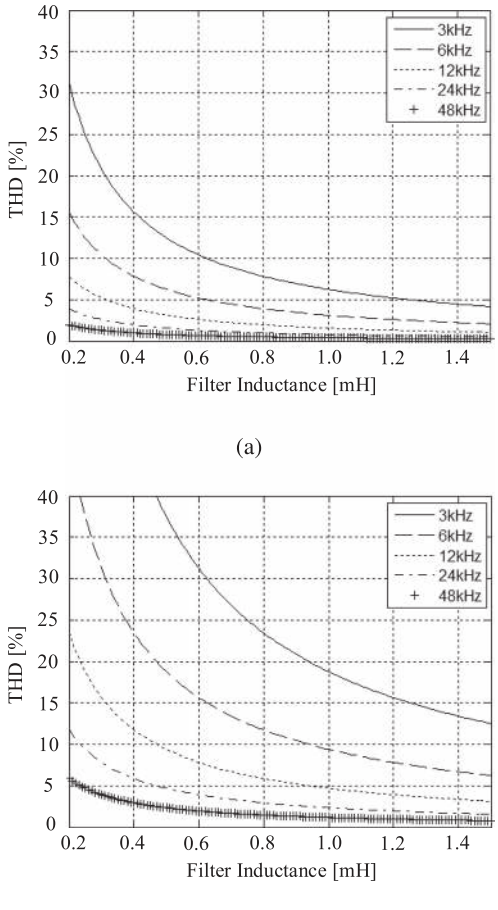
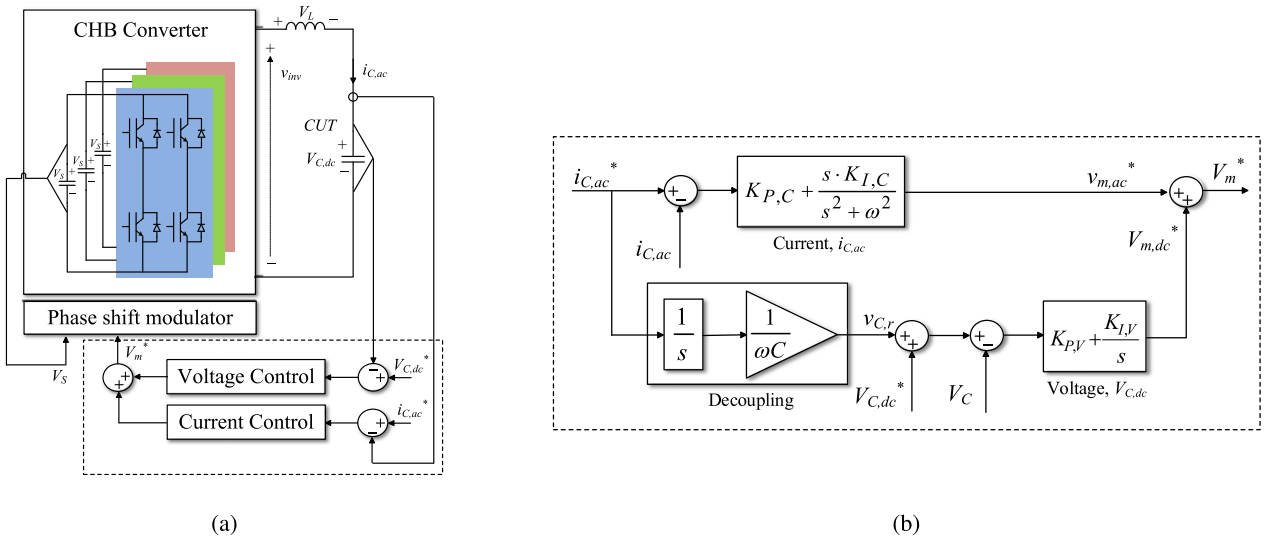


Fig. 8. THD as a function of filter inductance under different switching frequencies in case of (a) CHB and (b) HB.



(a) (b)

Fig. 9. (a) Concept of parallel control strategy and (b) its control block diagram.

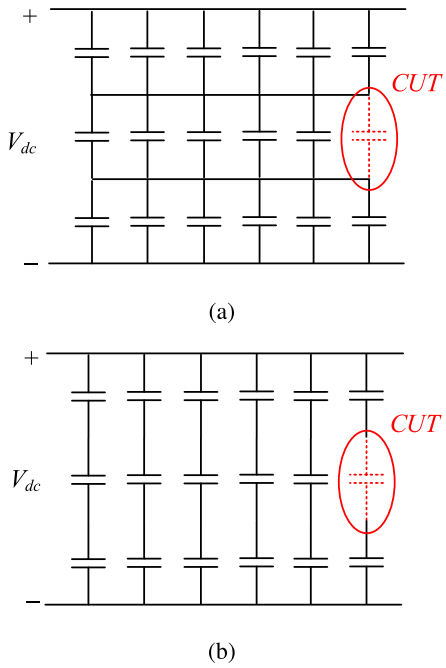


Fig. 10. Typical schemes of capacitor bank in a back-to-back converter; (a) internally paralleled and (b) not internally paralleled.

In the following, the THD performance of each converter is evaluated by a mathematically derived equation, which is a function of the filter inductance and the switching frequency. The dc bias voltage of the CUT can be defined as

$$V_{C,\mathrm{dc}} = 6 \cdot V_S \cdot (D - 0.5) \tag{9}$$

where V_S is the source voltage and D represents the duty ratio whose range is from zero to one. The voltage drop across the filter inductor is determined by a relation between V_S and $V_{C,\mathrm{dc}}$ as

$$V_L = 3 \cdot V_S - V_{C,\mathrm{dc}}. \tag{10}$$

Then, the switching ripple current is given as

$$\Delta I_L = \frac{V_L \cdot D}{L \cdot f_S} \quad (\mathrm{CHB})$$
$$\Delta I_L = \frac{3 \cdot V_L \cdot D}{L \cdot f_S} \quad (\mathrm{HB}) \tag{11}$$

where L is the filter inductance and f_S denotes the device switching frequency.

By substituting (9) and (10) into (11), the switching ripple current can be defined as a function of L, f_S, and D, assuming that V_S is constant

$$\Delta I_L(L,\, f_S,\, D) = \frac{V_S \cdot (1 - D) \cdot D}{L \cdot f_S} \quad (\mathrm{CHB})$$
$$\Delta I_L(L,\, f_S,\, D) = \frac{3 \cdot V_S \cdot (1 - D) \cdot D}{L \cdot f_S} \quad (\mathrm{HB}). \tag{12}$$

Consequently, the THD can be determined by (12) and amplitude of the capacitor current as

$$\mathrm{THD} = \frac{\Delta I_L(L,\, f_S,\, D)}{|i_{C,\mathrm{ac}}|}. \tag{13}$$

The THD of each converter is shown in Fig. 8 as a function of the filter inductance with different switching frequencies, where D is fixed to 0.5 for simplicity. In order to achieve the same THD performance with the HB, either a bigger filter inductance or a higher switching frequency needs to be chosen. However, the bigger filter inductance leads a lower effective dc bias voltage on the CUT due to a higher voltage drop across the filter, which implies a higher source voltage to be required. Even though the filter inductance can be reduced by employing the higher switching frequency, this is limited by the commercially available switching devices. The relation between the total source voltage and the voltage drop on the filter inductor is presented in (14), and this should be satisfied in order to provide the $i_{C,\mathrm{ac}}$ in combination with the $V_{C,\mathrm{dc}}$

$$V_S \geq V_{C,\mathrm{dc}} + 2 \cdot \pi \cdot f_{I_C} \cdot L \cdot i_{C,\mathrm{ac}} \tag{14}$$

where f_{Ic} denotes the fundamental frequency of $i_{C,\mathrm{ac}}$.

Consequently, the CHB converter is reasonable solution for this purpose, since the better THD performance can be achieved with the lower filter inductance and the slower switching frequency, then, in turn, this leads the lower source voltage and the lower block voltage of the switching devices.

B. Parallel Control Strategy

As stated before, the sinusoidal current ($i_{C,\mathrm{ac}}$) and the dc bias voltage ($V_{C,\mathrm{dc}}$) on the CUT should be simultaneously controlled and this can be done by the proposed parallel control strategy shown in Fig. 9(a). As shown in Fig. 9(b), the current and the voltage control are accomplished by means of the proportional resonance (PR) and the proportional integral (PI) loop, respectively, and the final reference (V_m^*) is obtained by the summation of their output as

$$\begin{aligned} V_m^* &= V_{m,\mathrm{dc}}^* + v_{m,\mathrm{ac}}^* \\ &= V_{m,\mathrm{dc}}^* + V_{m,\mathrm{ac}}^* \cdot \cos(\omega t + \varphi) \end{aligned} \tag{15}$$

where $V_{m,\mathrm{dc}}^*$ is the output of the voltage control loop, $v_{m,\mathrm{ac}}^*$ is the output of the current control loop, ω is the angular frequency, and Φ denotes the initial phase. The proposed control strategy also features to decouple the two paralleled control loops in order to prevent a conflicting target, since the current ($i_{C,\mathrm{ac}}$) through the CUT causes a ripple voltage on the dc bias voltage ($V_{C,\mathrm{dc}}$) as

$$V_C = V_{C,\mathrm{dc}} + v_{C,r} \tag{16}$$

where $v_{C,r}$ is the ripple component that is coupled with the current. Hence, this component should be eliminated and can be expressed by the capacitance of the CUT and the current reference as

$$v_{C,r} = \frac{1}{s} \cdot \frac{1}{\omega C} \cdot i_{C,\mathrm{ac}}^*. \tag{17}$$

By adding the above-mentioned equation to the reference of the dc bias voltage ($V_{C,\mathrm{dc}}^*$) and, then, substituting it by the measured voltage (V_C), only dc component can be fed to the voltage controller.

To conclude the section, it is worth noting that the proposed control block in Fig. 9(b) provides single sinusoidal currents in order to analyze the effect of each single frequency based on the decomposition of considered current profile. However, the real current profile could be synthesized with additional PR current controllers to combine the impacts of several harmonic components. Moreover, the feedback controller could be mathematically designed with consideration of the system nonlinearity for precise and stable performance in [32]. Finally, the presented analysis can be adopted to other applications that feature dc-link capacitors, like the uninterrupted power supplies [33].

V. Experimental Results

The typical configuration of a dc-link capacitor bank in a back-to-back converter is shown in Fig. 10 [34]. In this experiment, a single capacitor in the capacitor bank is targeted for the purpose of this paper.

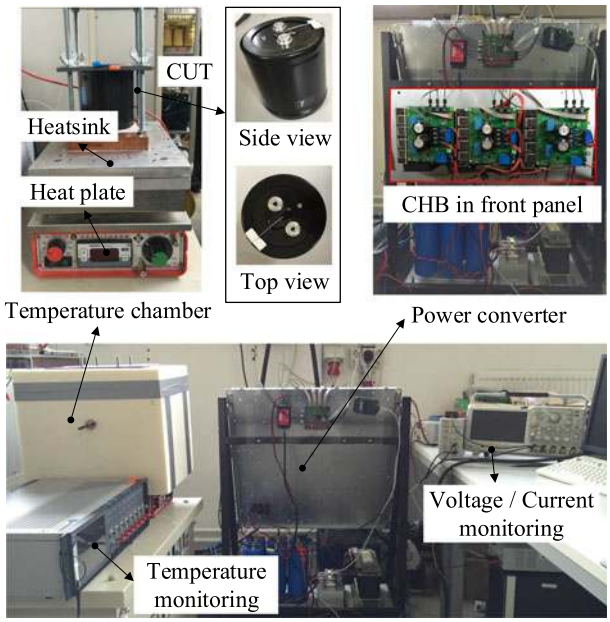


Fig. 11. Configuration of entire experimental setup; seven-level CHB converter, monitoring systems, temperature chamber, and CUT integrated with fiber optic sensor.

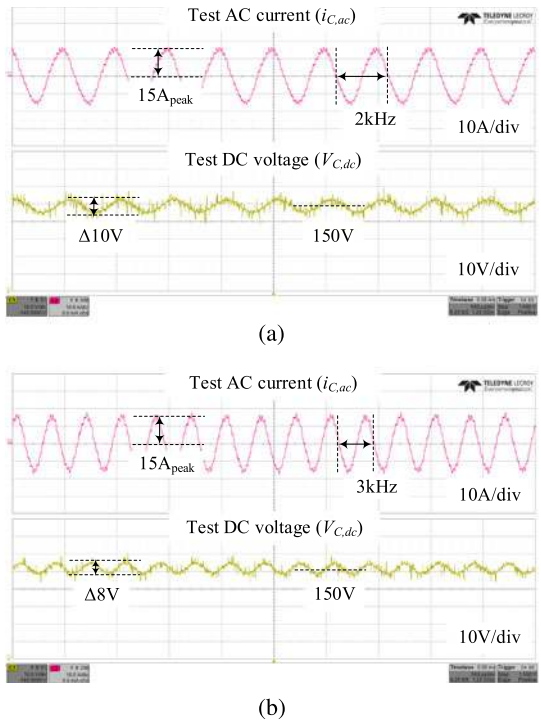


Fig. 12. High-frequency sinusoidal current of (a) 2 kHz and (b) 3 kHz at dc bias voltage of 150 V [29].

As shown in Fig. 11, the developed setup is composed of the seven-level CHB converter controlled by a microprocessor "MPC5643L," the monitoring system for current and voltage on the CUT, and the temperature chamber to keep the ambient temperature at a same level during a test. Moreover, a temperature sensor is integrated into the CUT in order to measure directly the core temperature variation, which brings more precise re-

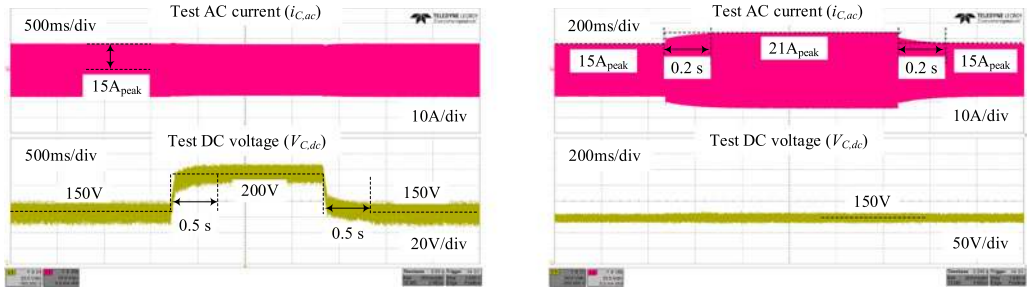


Fig. 13. Dynamic characteristic of (a) dc bias voltage control and (b) sinusoidal current control [29].

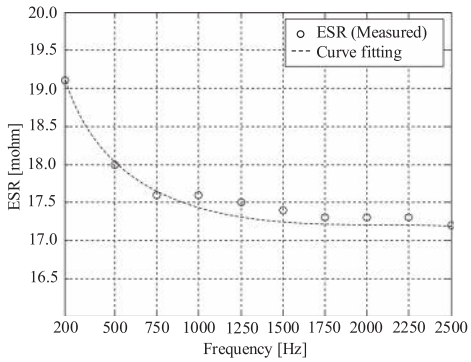


Fig. 14. ESR measurement of CUT.

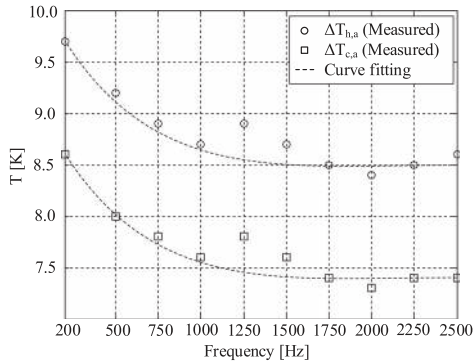


Fig. 15. Measurement of differences between core and ambient temperatures ($\Delta T_{h,a}$) and case and ambient temperatures ($\Delta T_{c,a}$) at constant amplitude sinusoidal currents at different fundamental frequencies.

sults than estimating methods through a case temperature and a thermal impedance [4], [5]. The core temperature of the CUT is measured by fiber optic sensors "OTG-A" and recorded by the signal conditioner "ProSens."

As stated in the previous section, the challenge of this work is to generate the high-frequency sinusoidal current in few kHz and to regulate the dc bias voltage simultaneously. The proposed control strategy is verified in Fig. 12(a) and (b) with controlled currents of 2 kHz and 3 kHz at the bias voltage of 150 V, respectively.

The paralleled control strategy allows basically the two parameters (the sinusoidal current and the dc bias voltage) to be controlled and the decoupling feed-forward term serves the ability of the completely separated control. This is confirmed through showing the dynamic characteristic in Fig. 13. Fig. 13(a) shows the case of the voltage control from 150 V to 200 V with the fixed current at 15 A_{peak}. The opposite case that the current is regulated from 15 A_{peak} to 21 A_{peak} while the voltage is fixed at 150 V is shown in Fig. 13(b). As it can be seen in both the cases, the change of one parameter does not affect the control performance of another parameter.

In Fig. 14, the ESR of the CUT (aluminum electrolytic capacitor 4500 μF, 500 V) measured at different frequencies is depicted and this is done with an *LCR* meter. As it can be seen, the ESR shows the frequency-dependent behavior as described in Section III. In order to verify the capabilities of the test setup at room temperature, constant amplitude ripple currents (14.3 A_{rms}) are applied to the CUT at different fundamental frequencies and the resulting hotspot temperatures are measured. The temperature differences between hotspot and ambient $\Delta T_{h,a}$ and case and ambient $\Delta T_{c,a}$, respectively, are shown in Fig. 15. In this context, case temperature refers to the temperature measured at the side of the capacitor can. Since the amplitude of the applied ripple current is fixed, it is expected that the curve of the hotspot temperature shows a proportional behavior to the measured curve of the ESR as shown in Fig. 14. As can be seen from Fig. 15, the progression of the measured temperature curves of both, $\Delta T_{h,a}$ and $\Delta T_{c,a}$, respectively, matches well the expectations. The measurements can be repeated for capacitors at different aging stages. Since the ESR of the capacitor will increase with increasing degradation, a higher hotspot temperature is to be expected in the experiments.

VI. Conclusion

This paper proposed a capacitor test setup to control sinusoidal currents at variable frequency and different dc bias voltages to reproduce the operating condition of the dc-link of a wind turbine system. This leads to the better understanding of relation between current harmonics and the capacitor hotspot temperature. To consider a real operating condition, the dc-link current in a back-to-back converter was decomposed as case study, and it was pointed out that the current harmonics are mainly distributed around the switching frequency harmonics. It was confirmed that this test requirement of high-frequency current in combination with dc voltage offset can be performed by the proposed converter and the control strategy. Finally, the capability of the test setup to provide sinusoidal test currents

for a broad range of frequencies was demonstrated by means of temperature measurements of case to ambient and hotspot to ambient in a test capacitor. Therefore, with the proposed setup it is possible to quantify impacts of wind turbine dc-link capacitor operating conditions on the capacitor lifetime.

APPENDIX

A. SYSTEM SPECIFICATION AND SIMULATION CONDITION

TABLE A-1
SPECIFICATION OF WIND TURBINE SYSTEM

Machine-side (PMSG)	Rated power	2 MW
	Rated voltage	690 V
	Rated frequency (f_m)	50 Hz
	Number of poles	4
	Switching frequency	1 kHz
DC-Link	Capacitance (C_{dc})	10 mF
	Voltage (V_{dc})	1100 V
Grid-side	Line-to-line voltage	690 V
	Frequency (f_g)	50 Hz
	Switching frequency (f_s)	1 kHz

TABLE A-2
CONSIDERED OPERATING POINTS TO IDENTIFY THEIR IMPACT ON CURRENT SPECTRUM

No.	Power (kW)	Machine-side (PMSG)		Grid-side	
1	128	Rotating speed (r/min)	600 (20 Hz)	Current per phase (A_{rms})	106
		Current per phase (A_{rms})	266		
2	432	Rotating speed (r/min)	900 (30 Hz)	Current per phase (A_{rms})	360
		Current per phase (A_{rms})	600		
3	1024	Rotating speed (r/min)	1200 (40 Hz)	Current per phase (A_{rms})	853
		Current per phase (A_{rms})	1066		
4	2000	Rotating speed (r/min)	1500 (50 Hz)	Current per phase (A_{rms})	1666
		Current per phase (A_{rms})	1666		

B. CALCULATION OF DC-LINK CURRENT IN BACK-TO-BACK CONVERTER

The time varying switched dc-link machine- and grid-side currents are expressed as a summation of each phase currents multiplied by their corresponding switching function as

$$\begin{aligned} i_{\mathrm{link},m}(t) &= \sum_{\eta=1}^{3} I_m \cos\left(\omega_m t + \varphi_{\eta,m} - \varphi_{0,m}\right) \\ &\quad \cdot S_{\eta,m}\left(t, \omega_m, \omega_{sw}, \varphi_{\eta,m}, \varphi_{\mathrm{pwm},m}\right) \\ i_{\mathrm{link},g}(t) &= \sum_{\eta=1}^{3} I_g \cos\left(\omega_g t + \varphi_{\eta,g} - \varphi_{0,g}\right) \\ &\quad \cdot S_{\eta,g}\left(t, \omega_g, \omega_{sw}, \varphi_{\eta,g}, \varphi_{\mathrm{pwm},g}\right). \end{aligned} \tag{A-1}$$

TABLE A-3
DEFINITION OF USED SYMBOLS

Symbol	Description
ω_{sw}	Switching frequency
$J_n(X)$	First kind Bessel function order *n*
I_m	Magnitude of the machine-side current
ω_m	Fundamental angular frequency of machine-side
$\varphi_{\eta,m}$	Phase of three-phase voltages (*a*, *b*, and *c* of machine-side)
$\varphi_{0,m}$	Phase between ac voltage and current of machine-side
$\varphi_{\mathrm{pwm},m}$	Phase of machine-side PWM carrier signal
$m_{m,a}$	Modulation index of machine-side
I_g	Magnitude of the grid-side current
ω_g	Fundamental angular frequency of grid-side
$\varphi_{\eta,g}$	Phase of three-phase voltages (*a*, *b*, and *c* of grid-side)
$\varphi_{0,g}$	Phase between ac voltage and current of grid-side
$\varphi_{\mathrm{pwm},g}$	Phase of grid-side PWM carrier signal
$m_{a,g}$	Modulation index of grid-side
η	1, 2, and 3 for phases *a*, *b*, and *c*

The switching function of each phase can be formed by the phase voltage function as

$$\begin{aligned} &S_{\eta,m}\left(t, \omega_m, \omega_{sw}, \varphi_{\eta,m}, \varphi_{\mathrm{pwm},m}\right) \\ &\quad = \frac{v_{\eta,m}\left(t, \omega_m, \omega_{sw}, \varphi_{\eta,m}, \varphi_{\mathrm{pwm},m}\right)}{V_{\mathrm{dc}}} \\ &S_{\eta,g}\left(t, \omega_g, \omega_{sw}, \varphi_{\eta,g}, \varphi_{\mathrm{pwm},g}\right) \\ &\quad = \frac{v_{\eta,g}(t, \omega_g, \omega_{sw}, \varphi_{\eta,g}, \varphi_{\mathrm{pwm},g})}{V_{\mathrm{dc}}}. \end{aligned} \tag{A-2}$$

The $v_{\eta,m}$ and $v_{\eta,g}$ are expressed as a function of the time, the fundamental frequency, the switching frequency, the phase of three-phase voltages, and the phase of the PWM carrier signal by

$$\begin{aligned} \frac{v_{\eta,m}\left(t, \omega_m, \omega_{sw}, \varphi_{\eta,m}, \varphi_{\mathrm{pwm},m}\right)}{V_{\mathrm{dc}}} &= \frac{1}{2} + \frac{2}{\pi}\sum_{n=1}^{\infty} \frac{1}{n\left(\frac{\omega_m}{\omega_{sw}}\right)} \\ &\times J_n\left(n\left(\frac{\omega_m}{\omega_{sw}}\right)\frac{\pi}{2} m_{a,m}\right) \sin\left(n\frac{\pi}{2}\right) \cos\left(n\left(\omega_m t + \varphi_{\eta,m}\right)\right) \\ &+ \frac{2}{\pi}\sum_{m=1}^{\infty}\frac{1}{m} J_0\left(m\frac{\pi}{2} m_{a,m}\right) \sin\left(m\frac{\pi}{2}\right) \cos\left(m\left(\omega_{sw} t + \varphi_{\mathrm{pwm},m}\right)\right) \\ &+ \frac{2}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{q} J_n\left(q\frac{\pi}{2} m_{a,m}\right) \sin\left((m+n)\frac{\pi}{2}\right) \\ &\times \cos\left(m\left(\omega_{sw} t + \varphi_{\mathrm{pwm},m}\right) + n\left(\omega_m t + \varphi_{\eta,m}\right)\right) \\ \frac{v_{\eta,g}(t, \omega_g, \omega_{sw}, \varphi_{\eta,g}, \varphi_{\mathrm{pwm},g})}{V_{\mathrm{dc}}} &= \frac{1}{2} + \frac{2}{\pi}\sum_{n=1}^{\infty} \frac{1}{n\left(\frac{\omega_g}{\omega_{sw}}\right)} \\ &\times J_n\left(n\left(\frac{\omega_g}{\omega_{sw}}\right)\frac{\pi}{2} m_{a,g}\right) \sin\left(n\frac{\pi}{2}\right) \cos\left(n\left(\omega_g t + \varphi_{\eta,g}\right)\right) \end{aligned}$$

$$+\frac{2}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}J_0\left(m\frac{\pi}{2}m_{a,g}\right)\sin\left(m\frac{\pi}{2}\right)\cos\left(m\left(\omega_{sw}t+\varphi_{\mathrm{pwm},g}\right)\right)$$

$$+\frac{2}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{q}J_n\left(q\frac{\pi}{2}m_{a,g}\right)\sin\left((m+n)\frac{\pi}{2}\right)$$

$$\cos\left(m\left(\omega_{sw}t+\varphi_{\mathrm{pwm},g}\right)+n\left(\omega_g t+\varphi_{\eta,g}\right)\right) \quad \text{(A-3)}$$

where $q = m + n(\omega_m/\omega_{sw})$. Finally, by substituting (A-2) and (A-3) into (A-1), the $i_{\mathrm{link},m}$ and $i_{\mathrm{link},g}$ are obtained.

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