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Research Article

Analysis of Leakage Reduction Techniques in Independent-Gate DG FinFET SRAM Cell

Vandna Sikarwar, Saurabh Khandelwal, and Shyam Akashe

ITM University, Gwalior, India

Correspondence should be addressed to Vandna Sikarwar; vandnas477@gmail.com

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Scaling of devices in bulk CMOS technology leads to short-channel effects and increase in leakage. Static random access memory (SRAM) is expected to occupy 90% of the area of SoC. Since leakage becomes the major factor in SRAM cell, it is implemented using FinFET. Further, double-gate FinFET devices became a better choice for deep submicron technologies. With this consideration in our research work, 6T SRAM cell is implemented using independent-gate DG FinFET in which both the opposite sides of gates are controlled independently which provides better scalability to the SRAM cell. The device is implemented using different leakage reduction techniques such as gated-V_{dd} technique and multithreshold voltage technique to reduce leakage. Therefore, power consumption in the SRAM cell is reduced and provides better performance. Independent-gate FinFET SRAM cell using various leakage reduction techniques has been simulated using Cadence virtuoso tool in 45 nm technology.

1. Introduction

CMOS scaling has led to improvement in performance of digital circuits however faces significant challenges due to process technology limits. Short-channel effects, subthreshold leakage, gate dielectric leakage, and device-to-device variations are the leading challenges in additional leakage current. Scaling to nanometer regime produces a major short-channel effect which arises from several geometrical effects in which the channel length becomes equal to the depletion layer. Drain-induced barrier lowering (DIBL) is the major effect produced by SCE, in which high electric fields from the drain can lower that barrier that is supposedly only controlled by the gate. As technology scales down, while dealing with short-channel effects (SCEs), not only very ultrathin t_{ox} to keep the current drive is required but also very low V_{th} is required to maintain the device speed and V_{th} variations under control [1] as this effect can degrade the devices subthreshold slope and cause changes in the threshold voltage (V_{th}). Leakage current produced due to SCE is mainly categorized into two types. They are gate leakage and subthreshold leakage. The subthreshold current generally occurs when the gate-to-source voltage V_{gs} of transistors is less than the threshold voltage V_{th}. When the current flows from the gate through the oxide layer to substrate, this current is called gate leakage current. As we go down below 65 nm technology, there seems to be no viable options of continuing forth with the conventional MOSFET. Therefore, multigate FETs such as planar double-gate FETs and FinFETs have been proposed for low-power digital CMOS technologies to reduce SCE. FinFET is a double-gate device in which the second gate is connected opposite to the first gate. FinFET can be designed as tied-gate and independent-gate FinFET. In the tied-gate type, both the opposite gates are tied together giving short-channel effect immunity, and in the independent gate, one gate is used to switch on/off, and threshold voltage of the FinFET is adjusted by the other gate giving better V_{th} control [2]. Use of independent-gate FinFET reduces leakage and hence reduces power consumption to improve performance.

Since memory structures engage over a large fraction of chip area of a microprocessor. Because of large size of on-chip memories, reduction of leakage current even in single cell of cache, a large fraction of the total power can be diminished in the microprocessor. SRAMs are built using minimum size transistors to minimize area, making it highly vulnerable to process variations [3]. Significant degradation in SRAM

cell data stability is acquired by lowering supply voltage and threshold voltages [4]. Therefore the development of SRAM cell to enhance the data stability and to reduce leakage with the use of FinFET technology is highly desirable [5]. FinFET is suitable for future nanoscale memory circuits design due to its reduced short-channel effects (SCEs) and leakage current [6].

Many circuit and architectural level techniques have been introduced to reduce leakage. In this paper, some circuit level techniques are introduced instead of architectural level techniques, because architectural level techniques degrade the performance with the reduction of power. There are different types of leakage reduction techniques. One is the multithreshold leakage reduction technique [7] which uses high threshold PMOS and NMOS acting as a switch to disconnect power supply during standby mode thereby reducing leakage. This technique provides increased operating speed by low-threshold MOSFET and reduced leakage by high-threshold voltage. This technique has the disadvantage of increased overall circuit area and introduces extra parasitic capacitance and delay during MOSFET fabrication. Another technique is gated-V_{dd} [8] in which an NMOS transistor with gated voltage supply is connected to the SRAM cell. This technique maintains the lower supply and threshold voltages although reducing leakage and leakage power dissipation. Stacking effect is produced by additional transistor in combination with the SRAM cell transistors when the gated-V_{dd} transistor is turned off. These techniques have also been used to reduce leakage in independent-gate mode of FinFET-based 6T SRAM cell.

2. Conventional 6T SRAM Cell

Conventional 6T SRAM cell consists of two cross-coupled inverters known as latch and two access NMOS transistors acting as pass transistors. These cross-coupled inverters forming the latch act as a storing element; that is, each bit is stored in the latch and access transistors are enabled using word line (WL). The drain terminals of access transistors are connected to latch inputs, and source terminals are connected to bit line (BL) and bit line bar (BLB). When the word line is low, access transistors are disabled. At this time, read or write operations cannot be performed and hold state is acquired. At this state, latch can hold bit as long as the voltages remain at V_{dd} and gnd. When the word line becomes high, access transistors are enabled, and at this stage read and write operations can be performed. The basic 6T SRAM cell is shown in Figure 1.

There are three modes of operation of SRAM cell: hold or data retention mode, read mode, and write mode [9].

2.1. Hold Operation. In this mode, SRAM cell is capable of retaining the data as long as it is powered. If the word line is disabled (WL = 0), the access transistors (NM3 and NM4) become off and bit line and bit line bar are disconnected from the latch. The two cross-coupled inverters continue to reinforce each other as long as they are connected to the supply voltage (V_{dd}). The current flow in this state is called leakage current.

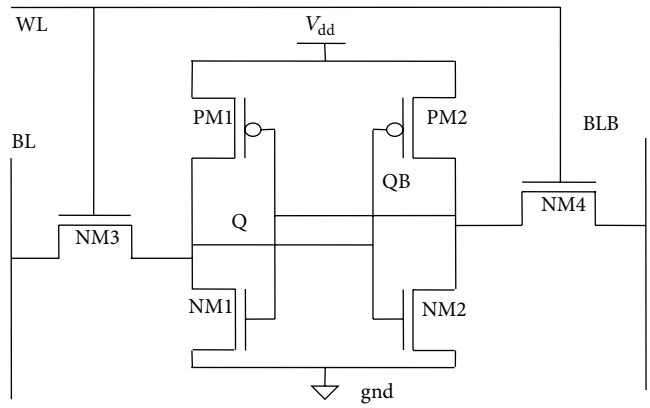


Figure 1: Schematic of conventional 6T SRAM cell.

2.2. Write Operation. In this mode, SRAM cell can be written with different bit value replacing its originally stored bit. To perform write operation, the access transistors (NM3 and NM4) are enabled using word line (WL = 1). The required data to be written is given to bit line (BL), and its complement is applied on bit line bar (BLB). That means if we want to write "1" to SRAM cell, we must provide "1" to bit line (BL) and "0" to bit line bar (BLB). When state of latch is changed the word line is deactivated (WL = "0"), and thus the required data is written to the cell.

2.3. Read Operation. In this mode, SRAM cell is capable of communicating its stored data. To read the data from the SRAM cell, the word line is kept at high (WL = "1") which activates the access transistors (NM3 and NM4). Now to perform read operation, both the bit lines are precharged to "1." Now one of the bit lines would remain precharged and the other would be discharged to ground, depending on the state of the latch. Thus if bit line (BL) remains charged, the bit line bar (BLB) must be discharged or vice versa. At this stage both the bit lines are applied to the input of sense amplifier which finally gives the information of the stored bit by amplifying the data to a significant level.

3. FinFET-Based SRAM Cell

The double-gate FinFET SRAM cell structure is a better choice due to the self-alignment of opposite sides of gates and the fabrication compatibility with the existing standard CMOS fabrication technology. The supply voltage (V_{dd}), threshold voltage (V_{th}), and Fin height can be used for reducing leakage in SRAM cell by increasing Fin height which allows reduction in V_{dd} but reduction in V_{dd} leaves strong impact on the stability of the SRAM cell under the parametric variations. Memories having short access time and low-power dissipation are generally required so that FinFET-based SRAM cells become popular due to the low-power dissipation. In addition, FinFET cell offers greater

noise margins. FinFET provides effective control of the short-channel effects without vigorously scaling down the gate-oxide thickness and increasing the channel doping density. The double-gate FinFET SRAM cell works in four different modes: shorted- or tied-gate (SG) mode, independent gate (IG) mode, low power (LP) mode and IG/LP mode. In the independent-gate mode, both the gates are controlled independently for low-power consumption.

3.1. Tied-Gate DG FinFET SRAM Cell. Tied-gate DG FinFET SRAM consists of WL to enable access to FinFET NMOS transistors. Two DG FinFET inverters are connected back to back as the bulk CMOS SRAM. FinFET reduces the SCE and hence leakage. But the delay increases in the 6T SRAM by using DG FinFET to some extent during the read and write cycle. All the transistors are sized minimum in this paper. For enhanced noise immunity and stability, minimum-sized SRAM is highly desirable, but the enhancement in stability through SRAM sizing comes at a cost of significantly higher leakage power consumption and cell area.

3.2. Independent-Gate DG FinFET SRAM Cell. Opposite sides of gates are restrained independent of each other in the independent-gate DG FinFET. In this device, multithreshold voltages are provided by independent-gate biasing which can be exploited to reduce number of transistors. Independent-gate DG SRAM cell is designed which reduces leakage current and increases data stability hence performance of the cell. Fins have been provided with minimum width. In cross-coupled inverters, both the opposite side gates in pull-up transistors are controlled independently to provide multithreshold voltages, and opposite gates in pull-down transistors are tied to each other. Direct-data-access mechanism causes interference in read cycle which can be minimized within the latch without increasing the transistor size. Therefore independent-gate FinFET gives better stability in SRAM cell.

While the word line (WL) is kept at low, the access transistors cut off to make the SRAM in standby mode. The stored bit is sustained by the latch of the SRAM cell. For a read operation, WL becomes high after the bit lines (BL and BLB) are precharged to V_{dd} and V_{ss}. Node Q stores "0"; BL is discharged through NM3 and NM1. Alternatively, when node QB stores "0," BLB is discharged through NM4 and NM2. The access transistors NM3 and NM4 act as high-V_{th} devices with weaker current-conducting capability as compared to tied-gate FinFET SRAM so that the current produced by access transistors is reduced. During a write operation, the WL is high. The access transistors NM3 and NM4 act as weak high-threshold-voltage devices. To write "0" at node Q, BL is discharged and BLB is charged so that transistor NM3 conducts and "0" is passed to IG-FinFET SRAM cell through NM3. Alternatively, to write "0" at node QB, BL is charged and BLB is discharged so that transistor NM4 conducts and "0" is passed to IG FinFET SRAM cell through NM4 as shown in Figure 2.

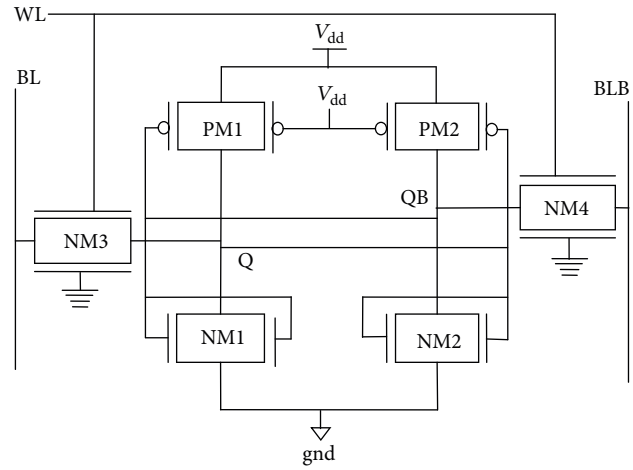


Figure 2: Schematic design of SRAM cell using independent-gate FinFET.

4. Leakage Current Components

Leakage current becomes a great issue in deep submicron CMOS technology consisting of three major components. They are junction-tunneling leakage, subthreshold leakage, and gate leakage. In CMOS technology junction leakage does not leave much affect on total leakage, whereas subthreshold leakage and gate leakage leave a greater impact in total leakage. Subthreshold leakage, gate leakage, and junction-tunneling leakage have been described below.

4.1. Subthreshold Leakage. Generally, subthreshold leakage is the drain source current of the transistor when the gate-source voltage becomes less than the threshold voltage ($V_{gs} < V_{th}$) [10]. In the weak inversion (or subthreshold) regime, the drain current depends exponentially on the gate-source voltage given by

$$I_d \propto \exp\left(\frac{V_{gs}}{nV_T}\right), \tag{1}$$

where

$$V_T = \frac{kT}{q}. \tag{2}$$

Here, V_T is the temperature voltage, k the Boltzmann constant, T the absolute temperature, and q the electron charge.

4.2. Gate Leakage. Since oxide scaling increases the field across the oxide. The high electric field coupled with the low oxide thickness results in gate-tunneling leakage current from the gate to the channel and source/drain overlap region or from the source/drain overlap region to the gate. Gate leakage mainly consists of three components: gate-to-source/-drain overlap current, gate-to-channel current, and gate-to-substrate current. Gate-to-source/-drain overlap current overcomes when the transistor is in off state and gate-to-channel leakage current takes place when the transistor is

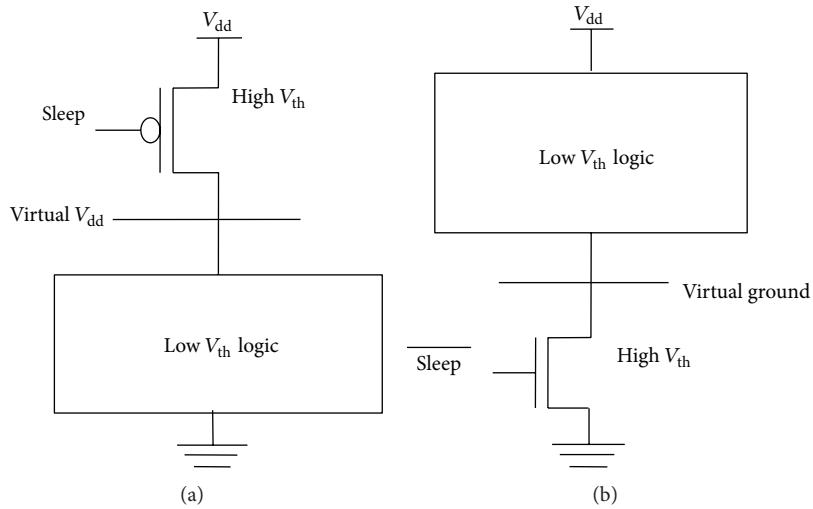


Figure 3: Multithreshold voltage technique using (a) PMOS HVT and (b) NMOS HVT.

in on state, whereas gate-to-substrate leakage is less than the gate-to-channel and gate-to-source/-drain overlap current. Since gate-to-source/-drain overlap region is less than the gate-to-channel, gate leakage current in off state is less than gate leakage current in on state.

4.3. Junction-Tunneling Leakage. Generally, junction-tunneling leakage takes place in reverse biased PN junction which consists of two components. One is diffusion of minority carriers (either electrons or holes) near the edge of depletion region, and the other is generation of electron hole pairs in the depletion region of reverse bias junction. It is an exponential function of reverse bias voltage and junction doping. Junction leakage does not contribute more in the total leakage current.

5. Leakage Reduction Techniques

5.1. Multithreshold Voltage Leakage Reduction Technique. In multithreshold voltage (MVT) technique as shown in Figure 3, a high-threshold sleep control is connected in series with low-V_{th} circuit. In active mode, sleep transistor must be on to provide the standard circuit functionality of SRAM cell. In standby mode, sleep transistor must be off to provide the improved leakage control. Sleep transistor of high threshold must be used; otherwise leakage current will increase making this technique less effective so that low-threshold FinFET transistors are used in the SRAM cell logic and high-threshold transistor as sleepy transistor. High-V_{th} transistors are used for low subthreshold current and low-V_{th} transistors are used to improve the performance of the cell. These two different types of threshold can be developed by changing the channel length. Figures 3(a) and 3(b) show the MVT technique using PMOS and NMOS, respectively.

5.2. Gated-V_{dd} Technique. Leakage associated with SRAM cell creates a major problem in chip designing because of large area. The leakage in cell can be reduced using gated-V_{dd} technique by contributing an extra transistor producing stacking effect. This extra NMOS transistor produces greater impact on leakage current in conjunction with SRAM cell transistors. It happens because gated transistor becomes on in used portions and becomes off during unused portions in SRAM cell. Here, NMOS transistor is connected between ground and source region of NMOS transistors of the cell. Similarly, PMOS transistor can also be connected between the V_{dd} and source region of PMOS transistors in SRAM cell. Gated-V_{dd} transistor becomes on during active mode and switches to off state during standby mode. Leakage current due to this technique can be reduced by stacking effect produced which arises because of the three transistors present between the ground terminal and the bit lines (BL and BLB). Transistor of adequate width must be used to provide isolation from leakage current during read cycle. During PMOS gated V_{dd}, insignificant area overhead and transistor width reduce because of no concern during read operation. So NMOS gated V_{dd} provides better control over the leakage than PMOS gated-V_{dd}. The gated V_{dd} technique is shown in Figure 4.

6. Simulation Results

The 6T FinFET SRAM cell using independent-gate mode is simulated using Cadence virtuoso tool at 27°C in 45 nm technology. In the SRAM cell, the output Q depends on bit line (BL) and QB depends on bit line bar (BLB) when write line (WL) is kept high. Leakage current and leakage power in independent gate FinFET SRAM cell are shown in Figures 5(a) and 5(b), respectively, in which transient analysis between 0 ns and 100 ns has been done and leakage current is calculated to be approximately equal to 120.3 pA and leakage power becomes 21.46 nW.

The leakage current and leakage power in independent-gate FinFET are reduced using multithreshold voltages. Figures 6(a) and 6(b) show leakage current and leakage power

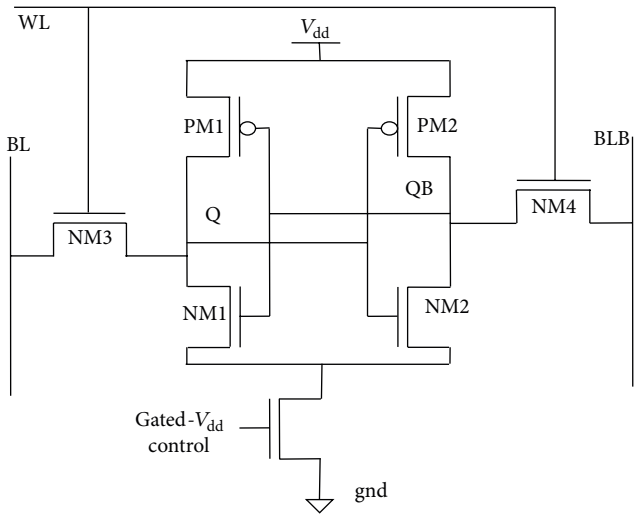
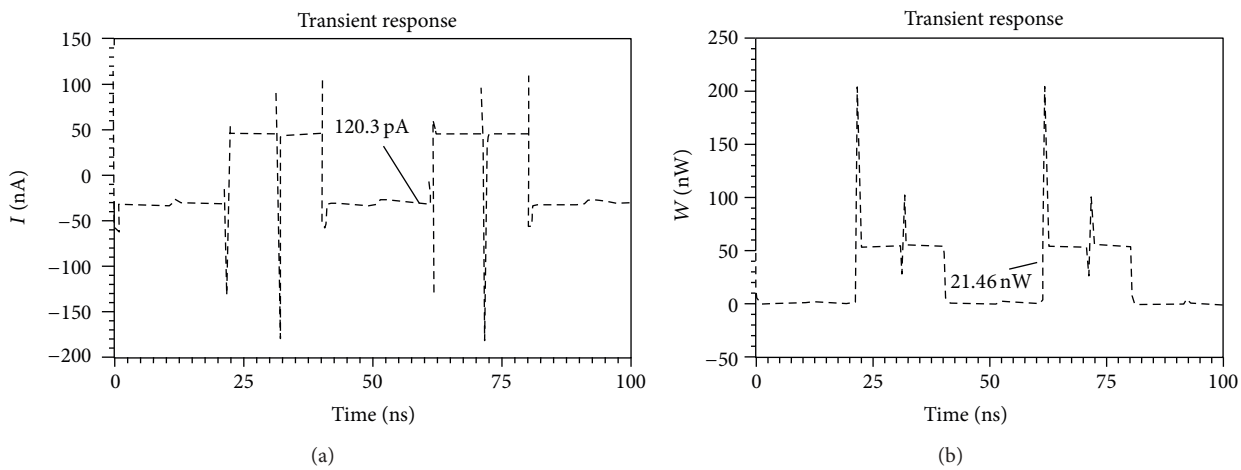
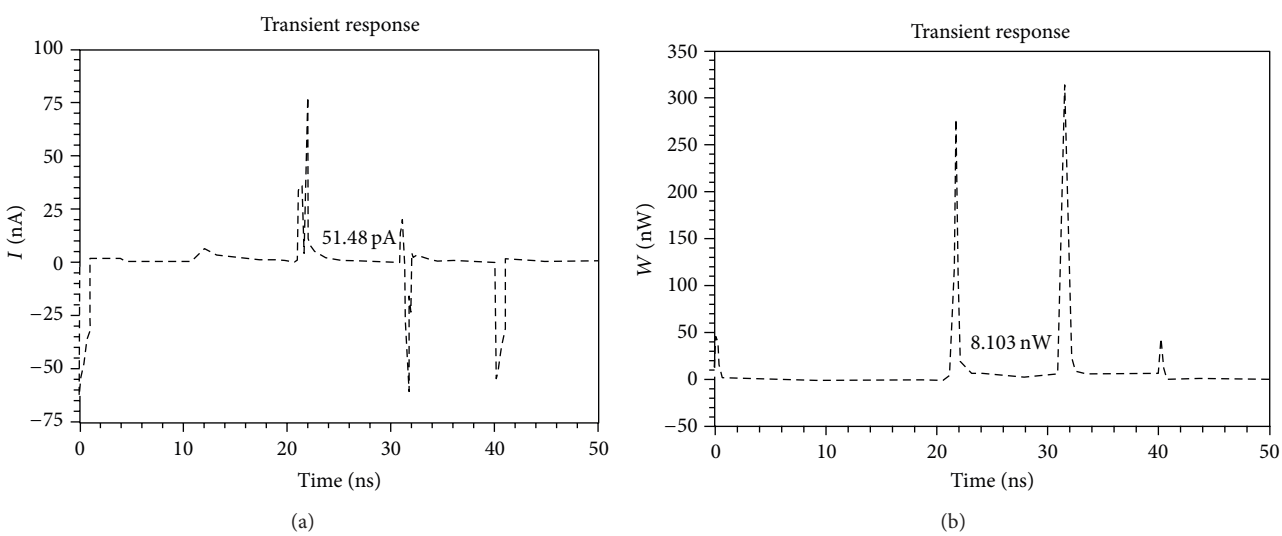


FIGURE 4: Conventional 6T SRAM cell using gated-V_{dd} technique.



(a) (b)

FIGURE 5: Predicted waveforms of leakage current and leakage power in independent-gate FinFET.



(a) (b)

FIGURE 6: Predicted waveforms for leakage current and leakage power in IG FinFET at 0.7 V using PMOS HVT.

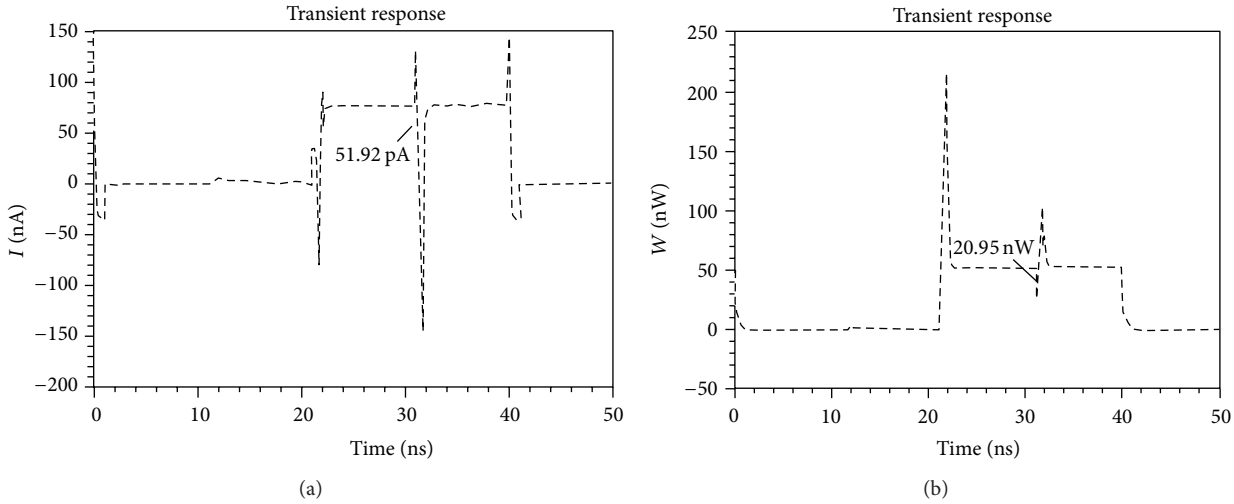


Figure 7: Predicted waveforms for leakage current and leakage power in IG FinFET at 0.7 V using NMOS HVT.

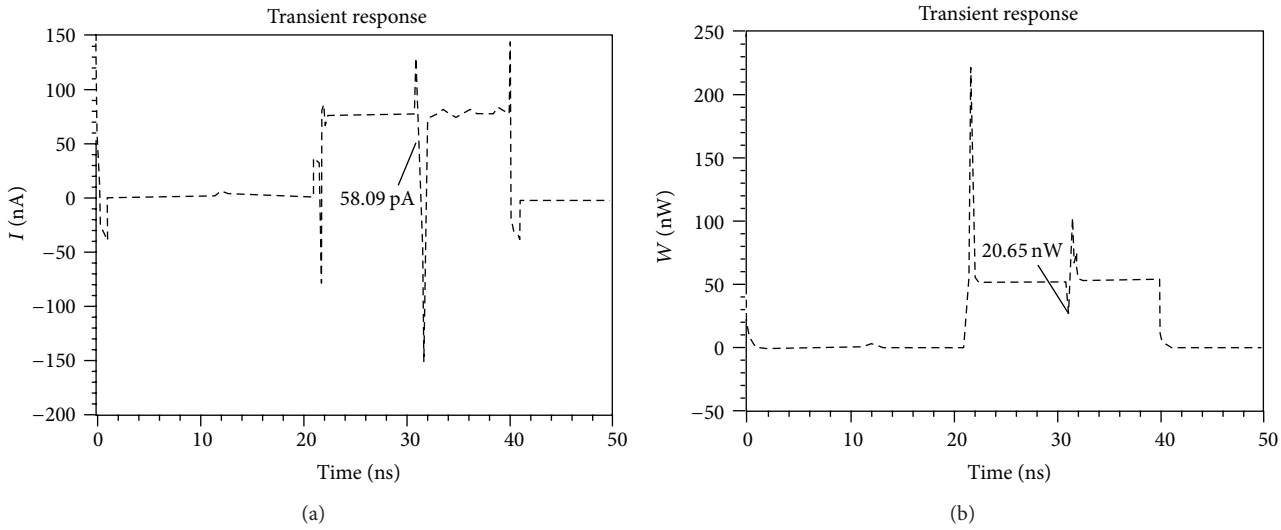


Figure 8: Predicted waveforms for leakage current and leakage power in IG FinFET at 0.7 V using gated-V_{dd} technique.

during standby mode in IG FinFET SRAM cell using PMOS HVT technique. According to this waveform, when elevated-threshold PMOS transistor is connected serially between V_{dd} and low-threshold SRAM cell logic circuit, subthreshold leakage and leakage power reduce allowing the low-threshold circuit to amplify the performance of the device. Transient response of IG FinFET SRAM cell is observed using MVT technique, and leakage current and power have been obtained, which are predicted to be equal to 51.48 pA and 8.103 nW respectively.

Figures 7(a) and 7(b) show leakage current and leakage power waveform of independent-gate FinFET SRAM cell when sleep transistor is kept off throughout hold state using NMOS HVT transistor. When high-threshold NMOS transistor is connected between ground and low-threshold SRAM cell, logic leakage current and leakage power reduce, thereby reducing power consumption and increasing performance. Leakage current and leakage power have been observed to be approximately equal to 51.92 pA and 20.59 nW, respectively.

Simulated independent-gate FinFET SRAM cell is connected with gated-V_{dd} transistor generating stacking effect. NMOS gated-V_{dd} transistor is used because it provides better insulation from leakage current and leakage power than PMOS gated-V_{dd} transistor. The extra gated-V_{dd} transistor becomes off during unused portions of the SRAM cell by providing virtual ground. The leakage current in gated-V_{dd} circuit is 58.09 pA; moreover, leakage power becomes 20.65 nW reducing the total power consumption as shown in Figures 8(a) and 8(b). Figure 9 shows the graphical representation of leakage current, leakage power, and power consumption in conventional, shorted-gate FinFET, and independent-gate FinFET SRAM cells. Figure 10 shows the graphical representation of similar parameters using various techniques.

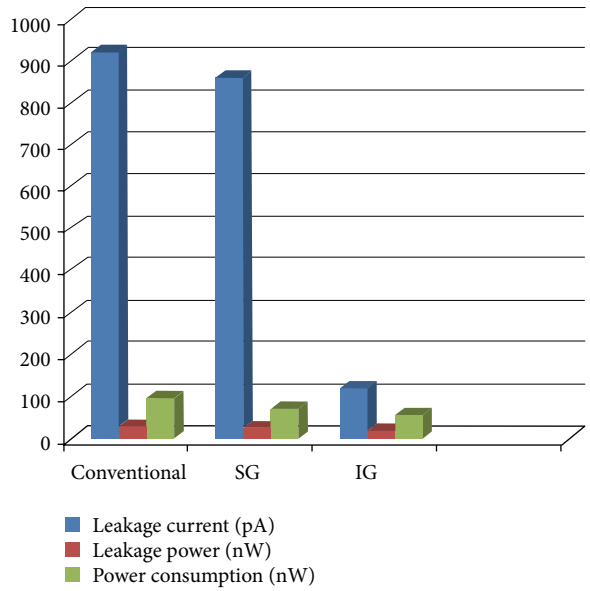


Figure 9: Graphical representation of leakage current, leakage power, and power consumption in 6T SRAM cell design using conventional, shorted-gate, and independent-gate modes.

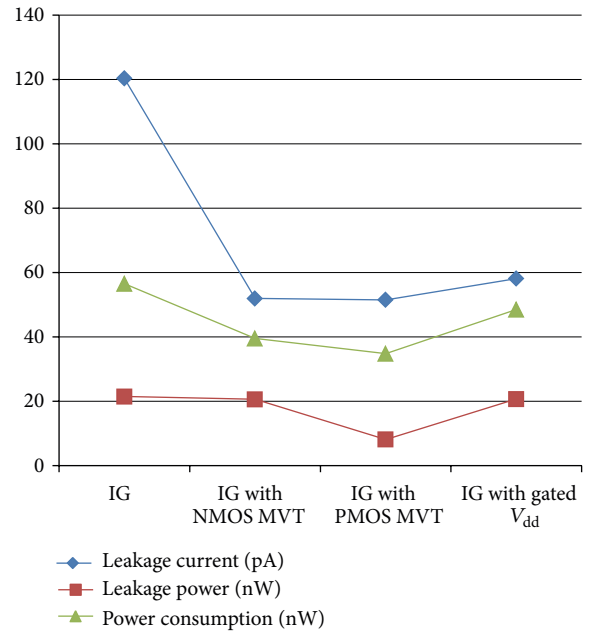


Figure 10: Graphical representation of various parameters such as leakage current, leakage power, and power consumption using independent-gate FinFET, IG FinFET with NMOS MVT, IG FinFET with PMOS MVT, and IG FinFET with gated-V_{dd} techniques in 6T SRAM cell.

7. Conclusion

Since SRAM cell consumes larger cell area in embedded system designs, it should have less leakage current and consume less power to offer better performance. According to the simulated results it is concluded that leakage current and leakage power have reduced to about 94% using independent-gate FinFET in comparison with conventional MOSFET. Leakage current in IG FinFET SRAM cell using NMOS HVT is reduced by approximately 95%. Leakage current using PMOS HVT is reduced by 94%,and using gated-V_{dd} technique, it is reduced by 93%. Similarly, leakage power is reduced by approximately 30% using NMOS HVT, and leakage power is reduced by 76% using PMOS HVT in IG FinFET SRAM cell, whereas leakage power is reduced by ~20%–25% using gated-V_{dd} technique in IG FinFET SRAM cell. Therefore, it can be said that among these leakage reduction techniques, multithreshold voltage technique offers better leakage control over the gated-V_{dd} technique by providing virtual ground and virtual V_{dd} instead of direct supply voltage. MVT technique provides less power consumption and better performance making it suitable for IC design.

Acknowledgments

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