

1 Analysis of negative capacitance and self-heating in organic semiconductor 2 devices

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8 In admittance spectroscopy of organic semiconductor devices, negative capacitance values arise at
9 low frequency and high voltages. This study aims at explaining the influence of self-heating on the
10 frequency-dependent capacitance and demonstrates its impact on steady-state and dynamic experi-
11 ments. Therefore, a one dimensional numerical drift-diffusion model extended by the heat equation
12 is presented. We calculate the admittance with two approaches: a Fourier method that is applied to
13 time domain data and a numerically efficient sinusoidal steady state analysis (S³A), which is based
14 on the linearization of the equations around the operating point. The simulation results coincide
15 well with the experimental findings from reference [H. Okumoto and T. Tsutsui, Appl. Phys.
16 Express **7**, 061601 (2014)] where the negative capacitance effect of an organic device becomes
17 weaker with better cooling of the structure. Linking the frequency- and time-domain with the
18 Fourier approach supports an effortless interpretation of the negative capacitance. Namely, we find
19 that negative capacitance originates from self-heating induced current enhancement. © 2015
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20 I. INTRODUCTION

21 The influence of self-heating on the device performance
22 has been recognized as a major issue in large-area OLEDs.^{1,2}
23 Different remedies were taken to reduce the heat generation
24 on the anode caused by the resistive material. For example,
25 metal grids were added on top of the anode to decrease the
26 potential drop leading to more homogeneous potential, cur-
27 rent, temperature, and light distributions.³ However, in small
28 organic devices heat generation has only recently been of
29 concern.⁴

30 In order to characterize an organic semiconductor de-
31 vice, a number of different techniques are available and com-
32 monly performed. In admittance spectroscopy, negative
33 capacitance values are often observed at high bias and low
34 frequency and have started a controversial debate. Negative
35 capacitance measurements are well known from Si diodes.
36 Numerous explanations⁵ (and references therein) are named
37 as origin or the negative capacitance is considered a parasitic
38 measurement effect.⁶ First occurrence of negative capaci-
39 tance in organic LEDs dates back about a decade.^{7,8} In gen-
40 eral, the same structure also exhibits positive capacitance at
41 different measurement conditions such as frequency, applied
42 voltage, or temperature. A wide range of origins for the neg-
43 ative capacitance have been brought forward for organic
44 semiconductor devices.^{9–13}

45 Most of the references investigating negative capaci-
46 tance are limited to bipolar devices and do not analyze the
47 occurrence in hole-only devices (HODs) or electron-only
48 devices (EODs). Little work has been dedicated to unipolar
49 devices so far. For instance, Refs. 14 and 15 report the

fabrication and measurement of HOD and EOD exhibiting
negative capacitance. The authors attribute the observed neg-
ative capacitance effects to interfacial states. Only recently
self-heating has been identified as another origin for the neg-
ative capacitance in organic semiconductor devices by
Okumoto and Tsutsui¹⁶ for a HOD and bipolar device. Self-
heating of the device changes the capacitance value of the
structure, even in the case of a small device. In Ref. 16, add-
ing a copper block on top of the HOD led to a reduced nega-
tive capacitance value indicating that the device temperature
plays an important role.

60 In this paper, we demonstrate the influence of self-
61 heating in the organic semiconductor with the aid of an
62 extended one dimensional numerical drift-diffusion model
63 on the steady-state current-voltage curve, dark injection tran-
64 sient currents experiment, or also called transient space-
65 charge limited current (T-SCLC) and, most importantly, on
66 the admittance spectroscopy. We will shed light on the
67 occurrence of the negative capacitance in single carrier devi-
68 ces. Furthermore, we attempt to establish a link between the
69 time and the frequency domain to ease the interpretation of
70 the negative capacitance. Therefore, we simulate in the fre-
71 quency domain a negative capacitance and check in the time
72 domain if we can find indications leading to a negative ca-
73 pacitance value.
74

75 II. METHODS

76 A. Mathematical model

77 To model the electrical part of a hole-only device,
78 we apply a one dimensional drift-diffusion model¹⁷ that
79 includes the Poisson equation (1) for the hole density p and
80 the potential ψ

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$$\nabla \cdot (\epsilon_0 \epsilon_r \nabla \psi) = q(-p), \quad (1)$$

$$J_p = -qp\mu \nabla \psi - qD \nabla p, \quad (2)$$

$$\nabla \cdot J_p + q \frac{\partial p}{\partial t} = 0. \quad (3)$$

81 The vacuum permittivity is denoted by ϵ_0 , the relative per-
82 mittivity by ϵ_r , and the elementary charge by q . Furthermore,
83 the continuity equation (3) with the current density J_p (2) is
84 solved where the mobility of the organic semiconductor is
85 given by μ .

86 For simplicity, we assume fixed charge carrier densities
87 at the anode (4) and cathode (5). For a device with thickness
88 L and with N_0 the number of sites, we write

$$p(0) = N_0, \quad (4)$$

$$p(L) = N_0 \exp\left(-\frac{qV_{bi}}{kT}\right), \quad (5)$$

89 where the built-in voltage is denoted by V_{bi} .

90 The classical drift-diffusion model (1)–(3) is only solved
91 in the organic material layer of the hole-only device as
92 shown in Fig. 1.

93 The electrical model is extended by the heat equation
94 (6), where the temperature is given by T . We assume that
95 heat transfer in the device takes place by thermal conduction
96 and that thermal exchange with the surrounding is based on
97 convection and thermal radiation. The heat transfer is calcu-
98 lated for the entire domain of the hole-only device. The heat
99 source term $J_p^2/(q\mu p)$ is restricted to the organic semicon-
100 ductor layer. The heat source therein is given by Joule heat-
101 ing,¹⁸ which is proportional to the electrical resistance of the
102 material. In the other layers, there is no heat source, only
103 heat conduction. In the continuity equation for heat
104 conduction

$$c\rho \frac{\partial T}{\partial t} = \nabla \cdot (k \nabla T) + \frac{J_p^2}{q\mu p}, \quad (6)$$

105 the parameter c stands for the specific heat capacity, ρ for
106 the density, and k for the thermal conductivity.

107 For the thermal part, we use convective and radiative
108 boundary conditions. The heat flux density F is calculated

from the heat transfer coefficient h and the ambient tempera- 109
ture T_{ref} , further the emissivity is given by ϵ and the Stefan- 110
Boltzmann constant by σ 111

$$F = -k \nabla T = -h(T - T_{ref}) - \epsilon \sigma (T^4 - T_{ref}^4). \quad (7)$$

We assume the same temperature for the convective air flow 112
as for the ambient. 113

Note that we assume a temperature independent mobil- 114
ity μ , whereas the diffusion D increases with an enhanced 115
temperature since D is proportional to the temperature T 116

$$D = \frac{kT}{q} \mu. \quad (8)$$

We are aware that organic semiconductors in general exhibit 117
a temperature dependent mobility but as we show here, that 118
does not have to be employed to explain negative capaci- 119
tance. In the remainder of this paper, we will denote the one 120
dimensional drift-diffusion model (1 to 3) with 1D-DD and 121
the extended model (1 to 3 and 6) with 1D-EDD. 122

B. S³A and Fourier simulation method 123

In this section, we introduce two different approaches 124
for calculating the admittance of a sample device. For the 125
sample device with all parameters given in Table I, we only 126
consider the organic semiconductor layer at a constant de- 127
vice temperature of 300 K and solve the 1D-DD model. At a 128
later stage, we also apply the methods to the 1D-EDD 129
model. 130

The admittance $Y = \frac{I^{ac}}{V^{ac}}$ requires the determination of the 131
ac current response I^{ac} to a harmonic voltage modulation V^{ac} 132
 $= V_{offset} + V_0 \cos(\omega t)$. The frequency-dependent admittance 133

TABLE I. Material parameters for all simulations.

Thermal ²⁵			
Material	Density [kg/m ³]	Heat capacity [J/(kgK)]	Conductivity [W/(Km)]
Glass	2.6×10^3	8.2×10^2	3.0
ITO	7.2×10^3	3.4×10^2	8.0
Organic	1.2×10^3	1.7×10^3	2.0×10^{-1}
Al	3.9×10^3	9.0×10^2	2.0×10^1
Air gap	1.2	1.0×10^3	2.5×10^{-2}
Electrical			
Material	Mobility [m ² /(Vs)]	Site density [m ⁻³]	Relative permittivity
Organic	5×10^{-10}	1×10^{26}	3
Boundary conditions			
B.C	Parameter	Value	Units
Thermal	h	10/50	W/(m ² K)
	ϵ	0.92	
Electrical	V_{bi}	0.6	V

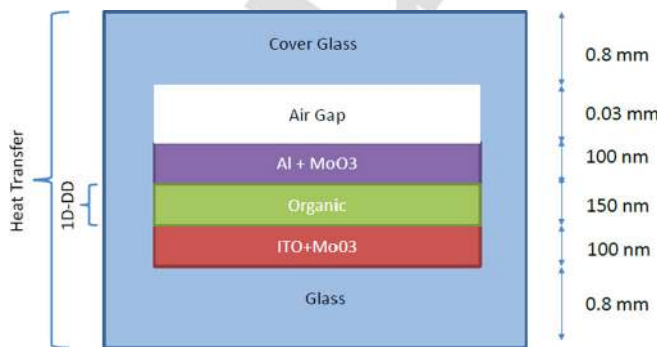


FIG. 1. Structure of HOD and thickness of layers. The heat equations are solved on the entire device domain, while the drift-diffusion model is only solved in the organic layer.

134 can then be decomposed into the conductance G and capaci-
 135 tance C according to $Y(\omega) = G(\omega) + i\omega C(\omega)$.

136 The first approach is the S^3A . In Ref. 22, a more detailed
 137 description of the method is given and was used previ-
 138 ously.^{22–24} We first solve the steady-state equations for
 139 V_{offset} and linearize the system of equations around this oper-
 140 ating point to get the ac equations. For each frequency ω , we
 141 solve the linear ac equations and calculate thereof the admit-
 142 tance $Y(\omega)$.

143 In the second approach, the transient current response
 144 $I(t)$ to a small voltage step ΔV is monitored and Fourier
 145 transformed. This leads to the following expression for the
 146 capacitance C and conductance G as elaborated in detail in
 147 Ref. 5:

$$C(\omega) = C_{geom} + \frac{1}{\Delta V} \int_0^{\infty} \delta j(t) \cos(\omega t) dt, \quad (9)$$

$$G(\omega) = G(0) + \frac{\omega}{\Delta V} \int_0^{\infty} \delta j(t) \sin(\omega t) dt. \quad (10)$$

148 The transient current density $\delta j(t)$ is defined as

$$\delta j(t) = I(t) - I(\infty), \quad (11)$$

149 so that $\delta j(t) \rightarrow 0$ in the steady-state limit ($t \rightarrow \infty$).

150 Applying the formula for the capacitance (9) and con-
 151 ductance (10) to the transient current response to a small
 152 voltage step as shown in Fig. 2, we can calculate the capaci-
 153 tance C and conductance G of the sample device. The tran-
 154 sient current response in Fig. 2 shows according to Ref. 21 a
 155 cusp at

$$t_{DI} = 0.786 \frac{L^2}{\mu(V - V_{bi})}. \quad (12)$$

156 This formula can be useful for mobility determination.

157 A comparison between the two methods is displayed in
 158 Fig. 3. In the work of Ref. 19, the value of $0.75C_{geom}$ is
 159 obtained below the transit frequency. Note that capacitance in
 160 our case is slightly enhanced due to diffusion which was
 161 neglected in Ref. 19, but we have previously shown²⁰ that the
 162 low-frequency capacitance reaches values of $0.8C_{geom}$ (not
 163 simply $0.75C_{geom}$) because the numerical model considers

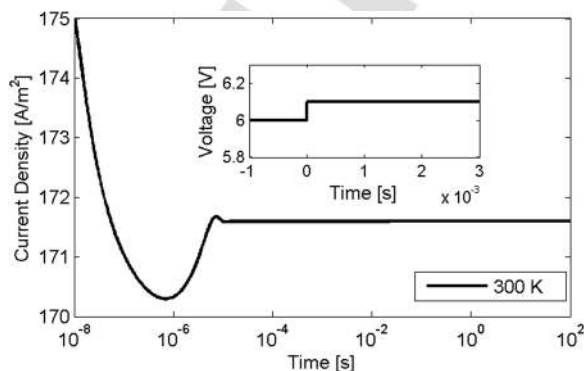


FIG. 2. The current density response over time is shown. A cusp is found and eventually the steady-state is reached. In the inset, the small voltage step is displayed.

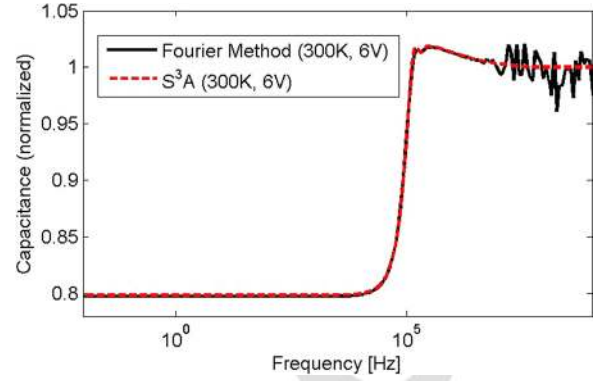


FIG. 3. The capacitance is calculated with two approaches: the black line represents the S^3A solution, while red stands for the Fourier method. At high frequency, the accuracy of the Fourier method is clearly limited.

charge diffusion, too. The negative differential susceptance
 164 $-\Delta B = -\omega(C(\omega) - C_{geom})$ yields a maximum at f_{max} due to
 165 the transit time effect leading to
 166

$$\mu = 1.85 \frac{L^2 f_{max}}{(V - V_{bi})}. \quad (13)$$

167 Comparing the two methods shows that the Fourier
 168 method is less accurate at high frequencies as the accuracy is
 169 dependent on the size of the time step Δt in the transient cur-
 170 rent response ($\Delta t \ll 2\pi f_{high}^{-1}$). Moreover, the applied voltage
 171 step ΔV must be small in order to be in the linear regime of
 172 the device, yet big enough to get an accurate numerical cur-
 173 rent resolution.

174 Despite the fact that the S^3A provides superior numeri-
 175 cal accuracy, the Fourier method allows for an effortless
 176 interpretation of the negative capacitance effects in the time-
 177 domain. We have now two methods at hand that allow for
 178 the determination of the capacitance C and conductance G .
 179 The two methods will be applied in Sec. IV.

180 III. STATIONARY SIMULATIONS

181 First of all, we turn to steady-state simulations and com-
 182 pare the results of the 1D-DD and 1D-EDD model. All param-
 183 eters are given in Table I.

184 In a first step, we perform the most common characteri-
 185 zation technique and calculate the current-voltage curve for
 186 the 1D-DD model for a constant device temperature of
 187 300 K. This result is shown as the black line in Fig. 4. In a
 188 next step, we extend the model by the heat equation on the
 189 entire domain and recalculate the current-voltage curve
 190 (allowing for self-heating of the device) and obtain the red
 191 curve (1D-EDD). At high voltage, self-heating clearly
 192 enhances the current. A change in temperature enhances dif-
 193 fusion (see Eq. (8)) and leads to more carriers in the device.
 194 Thus, the current increases.

195 In Fig. 5, the temperature profile of the entire device at
 196 6 V is displayed at steady-state. We notice that the air gap is
 197 mainly responsible for the temperature difference in the de-
 198 vice. The inset shows the temperature distribution of the
 199 electrodes and the organic layer as indicated by the arrow in

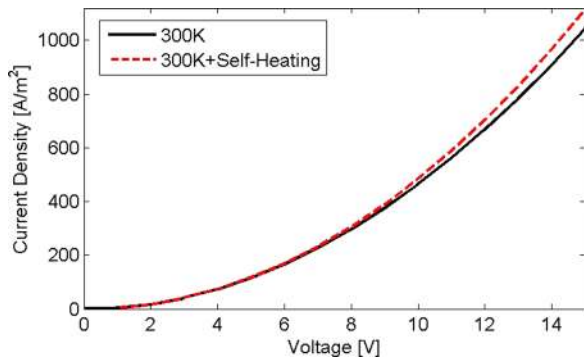


FIG. 4. Current-voltage curves for constant temperature in the device (black) and extended model with self-heating (red). Self-heating rises the current at high voltage.

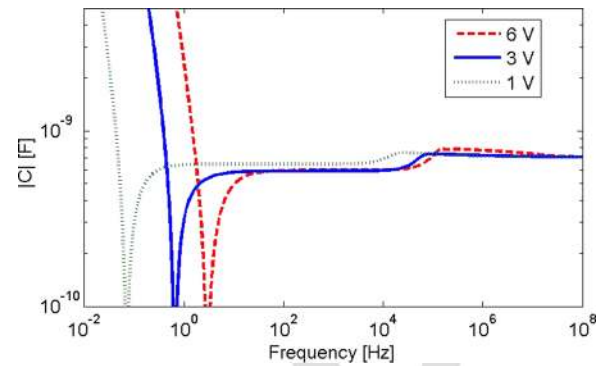


FIG. 6. The absolute value of the capacitance of the 1D-EDD model for different voltages. Including the heat equation leads to a considerable change in the capacitance at low voltage. At low bias, the effect is decreasing.

200 Fig. 5. Joule heating leads to the enhanced temperature in
201 the organic layer.

202 **IV. TRANSIENT SIMULATIONS**

203 The difference between the two models becomes even
204 more distinct when we look at time-dependent measurements
205 and simulations. Calculating the capacitance for the 1D-DD
206 model leads to the well known curve for a HOD as shown in
207 Fig. 3 or Refs. 22–24. The capacitance step at around 10⁵ Hz
208 can be related to the charge carrier mobility.²² Namely, at
209 higher frequency the capacitance approaches the geometric
210 capacitance of the device. Solving the 1D-EDD model with
211 heat transport changes the result vastly. At low frequency
212 and high bias, negative capacitance values are found as
213 shown in Fig. 6. The capacitance step remains at the same
214 position for the same applied voltage independent of self-
215 heating. In Fig. 6, the capacitance values for different
216 applied voltages are displayed for the 1D-EDD model. The
217 higher the applied bias, the more pronounced is the negative
218 capacitance effect.

219 In order to compare the effect of cooling in our model
220 with measurements in Ref. 16, we calculate the capacitance
221 of a HOD with thickness 150 nm as displayed in Fig. 7. By
222 changing the value for the convective cooling parameter *h*

(see 7), we can simulate the effect of a copper block and get 223 AQ2
an excellent agreement with measurement as shown in Fig. 4 224
of Ref. 16. Cooling makes the device less inductive. The 225
thermal parameters for the simulation are taken from Ref. 226
25. 227

The simulations can capture the features of the measure- 228
ments. Without the copper block, the capacitance becomes 229
increasingly negative with lower frequency and only flattens 230
at around 10⁻³ Hz. Cooling the device flattens the capaci- 231
tance curves at around 10⁻² Hz. The two situations show 232
that self-heating can lead to a negative capacitance, even in a 233
hole-only device. To shed light on the source of the negative 234
capacitance, we calculate the transient response for the 1D- 235
DD and 1D-EDD model. In terms of physics, this implies 236
that in the first case the device temperature remains constant 237
and in the second case self-heating is included. In Fig. 8, the 238
transient current density responses are shown for a voltage 239
step of 0.1 V. The current density values of the top curve are 240
higher due to self-heating. Both curves show a transit-time 241
cusp at *t_{DI}* regardless of self-heating. This is in agreement 242
with the top curve which, however, still increases after sev- 243
eral orders of magnitude in time after the cusp. The heat gen- 244
erated in the organic layer is conducted through the device 245
increasing the overall temperature, which again leads to a 246
higher current density in the organic layer. This is a slow 247
thermal process and the final steady-state current density 248

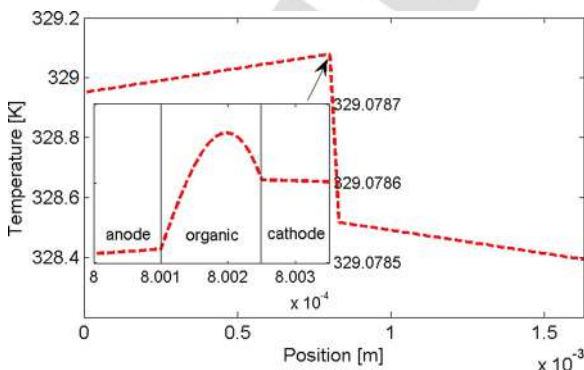


FIG. 5. For an operating voltage of 6 V, the temperature distribution over the entire device is shown in steady state. The biggest temperature drop is over the air gap between the cathode and the encapsulation. The arrow indicates the electrodes and organic layer. They are zoomed in the inset. Joule heating acts as a heat source in the organic material. The generated heat is then transferred to the electrodes.

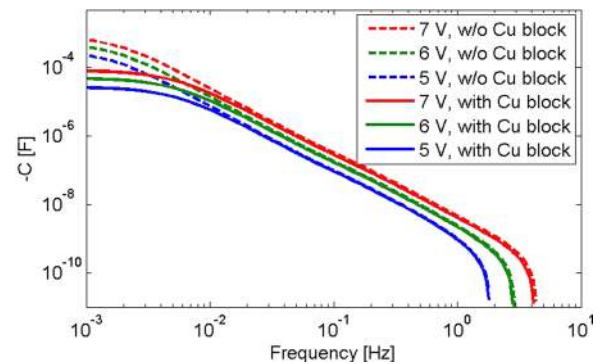


FIG. 7. Simulation of measurement features for different voltages and with and without the copper block. The cooling is modeled by changing the convective cooling boundary conditions. Cooling leads to smaller absolute capacitance values.

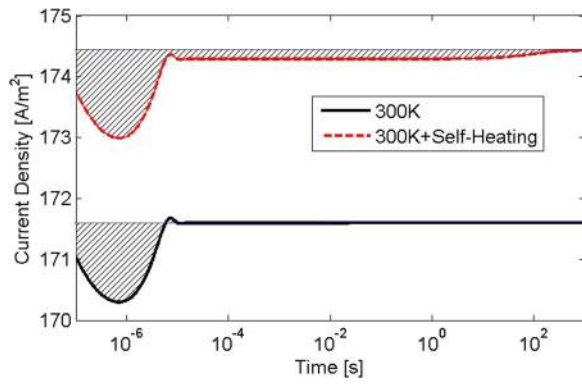


FIG. 8. Current density response for the 1D-DD and the extended 1D-EDD model to a voltage step of 0.1 V at an operating voltage of 6 V. The blue line represents the steady-state value and the reference level for the integral in Eq. (14) for the two cases. In the case of self-heating, the shaded area under the reference line is significantly bigger resulting in a negative capacitance value.

249 value is only reached after a while, approx. 10^2 s here.
 250 Transforming the data from the time domain to the frequency
 251 domain according to Eq. (9) reproduces the negative capaci-
 252 tance effect nicely for the device with self-heating. The absolute
 253 value of the capacitance is shown in Fig. 6 for different
 254 voltages. The curve corresponding to Fig. 8 is at 6 V, while
 255 the curve without self-heating corresponds to Fig. 3. To
 256 understand the negative capacitance occurrence, Ershov⁵ has
 257 pointed out that for low frequencies formula (9) can be
 258 approximated by

$$C(0) = C_{geom} + \frac{1}{\Delta V} \int_0^{\infty} \delta j(t) dt. \quad (14)$$

259 This implies that the integral that we add to the geometrical
 260 capacitance C_{geom} only depends on the transient current
 261 response with respect to its steady-state value as indicated
 262 with the blue line. The shaded area for the 1D-DD is mainly
 263 under the blue line leading to a negative contribution. It is res-
 264 ponsible for the reduction of the geometric capacitance to a
 265 value of approximately $0.8C_{geom}$ in Fig. 3. The shaded area
 266 under the blue line is clearly bigger in the case of self-
 267 heating leading to an even more negative capacitance contri-
 268 bution such that expression (14) turns negative. Note that we
 269 used a logarithmic time scale in Fig. 8 and the initial contri-
 270 bution to the dark injection transient cusp is relatively small
 271 in comparison to the rest of the shaded area. With this
 272 approach, we can easily classify a device with respect to nega-
 273 tive capacitance from its transient current density response.
 274 The temperature increase due to self-heating enhances the
 275 current density order of magnitudes later in time, which is
 276 thus responsible for the negative capacitance effect.

277 In order to investigate the resulting time scale for heat-
 278 ing, in Fig. 9 the simulated transient current density response
 279 is simulated for two distinct thermal model assumptions. The
 280 case of a thermal model including the entire device domain
 281 with the glass substrate is compared to a case where a
 282 reduced thermal model domain only including the organic
 283 semiconductor layer is considered. If the entire device
 284 including the glass substrate is included in the thermal model

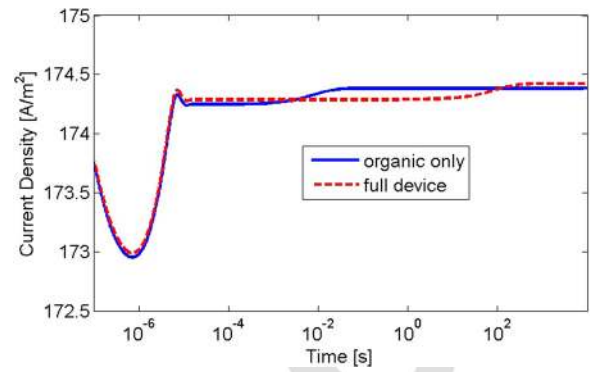


FIG. 9. The simulated transient response to a voltage step of 0.1 V at an operating voltage of 6 V is shown for two assumptions of the thermal modeling domain. If the modeling domain only contains the organic semiconductor layer then the self-heating induced current rise occurs within milliseconds. However, if the entire device including the glass substrate is included in the thermal model domain, then the characteristic time scale for the self-heating-induced current rise occurs at approx. 100 s after turn on, which is a realistic warm up period often observed in experiment. The time of the dark injection transient cusp is determined by the drift-diffusion model and thus identical for both assumptions of the thermal model domain.

domain, then the characteristic time scale for the self-heating- 285
 induced current rise is approx. 100 s after turn on. The 286
 size of the simulation domain changes the observed time lag 287
 when the self-heating starts. The larger the simulation dom- 288
 ain, the longer it takes to heat up and the hotter the device 289
 becomes. This is in agreement with the characteristic time 290
 t_{char} 291

$$t_{char} = \frac{L_{tot}^2}{k_e / (c_e \rho_e)}, \quad (15)$$

for the heat equation. The total device thickness of all layers 292
 and glass is denoted by L_{tot} and the effective thermal materi- 293
 als parameters have a subscript e . As expected, the dark 294
 injection transient time cusp remains at the same position for 295
 the two devices. Comparing the capacitance of the two devi- 296
 ces leads thus to a different frequency where the negative ca- 297
 pacitance effects set in as shown in Fig. 10. The 298
 encapsulation of an organic device is thus crucial for its elec- 299
 trical performance and can change the negative capacitance 300

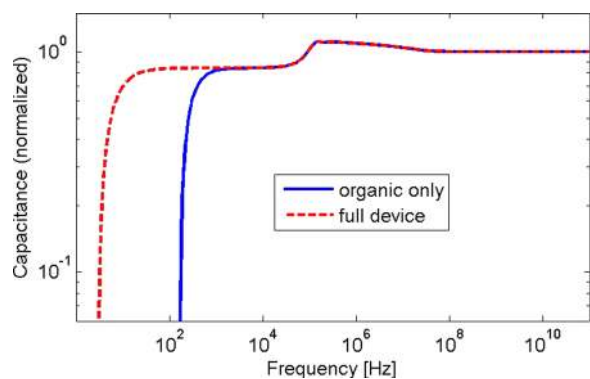


FIG. 10. The corresponding frequency-dependent capacitances to the transients in Fig. 9 are shown. For the more realistic thermal modeling domain including the glass substrate, the drop in capacitance (leading eventually to negative values) occurs at smaller frequencies, then in the simplified thermal model where only the organic semiconductor is considered.

301 behavior. Depending on the measurement regime, some sci- 352
 302 entists may claim that negative capacitance does not even 353
 303 occur, but changing the frequency range, the total device 354
 304 thickness or material around the organic semiconductor may 355
 305 reveal a negative capacitance effect. As indicated in 356
 306 Eq. (15), the characteristic time depends on the total thick- 357
 307 ness of all layers L_{tot} and on the thermal properties of all 358
 308 layers involved. 359

309 V. CONCLUSIONS

310 To identify and understand the origin of negative capaci- 360
 311 tance in organic semiconductor devices, the 1D-DD model 361
 312 of the organic semiconductor layer has been extended by the 362
 313 heat equation on the entire domain. With this model that 363
 314 includes Joule heating as heat source in the semiconductor 364
 315 layer, negative capacitance effects in single carrier devices 365
 316 were investigated. As opposed to large-area devices where 366
 317 the heat generation of the electrodes is considered, we focus 367
 318 on the self-heating in the organic semiconductor layer. 368

319 The model demonstrates the effect of self-heating in 370
 320 terms of the current voltage curve, but more importantly and 371
 321 distinctively, in dynamic characterization. We emphasize 372
 322 that our conclusions were drawn from a model in 1D and 373
 323 there is no need to resort to 3D. The model agrees very 374
 324 nicely with measurements from Ref. 16. Previously, other 375
 325 explanations as trap dynamics, interfacial states, recombina- 376
 326 tion, etc., were named as origin of negative capacitance. 377
 327 These effects, however, would not be affected by adding a 378
 328 copper block on top of the device and could not reproduce a 379
 329 negative capacitance effect by simulation. The 1D-DD 380
 330 model extended by heat conduction allows for a comprehen- 381
 331 sive and consistent description of charge transport taking all 382
 332 major physical processes into account as opposed to simpler 383
 333 models such as presented in Ref. 16 or equivalent circuit 384
 334 models.^{14,15} 385

335 With the aid of the Fourier method, an accessible expla- 386
 336 nation of the negative capacitance has been presented which 387
 337 allows for an interpretation in the time domain, which is gen- 388
 338 erally more intuitive than the frequency domain. 389

339 The analysis, however, has been restricted to a trap-free 390
 340 unipolar, single layer sample with constant mobility and sim- 391
 341 plified boundary conditions. As a next step, a quantitative 392
 342 comparison between measurement and simulation is desired. 393
 343 The model can be further improved by including a 394
 344 temperature-dependent mobility model. In unipolar samples, 395
 345 the negative capacitance effect might be overshadowed by 396
 346 adding trap states if they act on a similar time scale. Trap 397
 347 states usually enhance the capacitance at low frequency,²² 398
 348 while self-heating lowers the capacitance. The signature of 399
 349 trap states in the current voltage curve would lead to a reduc- 400
 350 tion of the current density. In the DITC, a decay after the 401
 351 transient-time cusp represents the trapping process. 402
 411 403

The simulations show the importance of self-heating in 352
 small devices and confirm self-heating as origin of negative 353
 capacitance. Depending on the structure of the samples, this 354
 might lead to undesired effects in the performance. Heat dis- 355
 sipation should be taken into account when fabricating or- 356
 ganic semiconductor devices and be considered in any 357
 electrical characterization technique regardless of dc, ac, or 358
 transient. 359

In conclusion, it is crucial to model the heat generation 360
 and transport in organic semiconductor devices in order to 361
 obtain accurate simulation results at typical operating condi- 362
 tions, i.e., current densities of organic semiconductor devi- 363
 ces. So far, the role of self-heating, especially in small 364
 devices, has been underestimated. It is very likely that our 365
 findings are not restricted to organic semiconductor devices 366
 but would hold for wider classes of materials and devices. 367
 368

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