Analysis of On-Chip Inductance Effects for Distributed RLC Interconnects

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***Abstract*—This paper introduces an accurate analysis of on-chip inductance effects for distributed RLC interconnects that takes the effect of both the series resistance and the output parasitic capacitance of the driver into account. Using rigorous first principle calculations, accurate expressions for the transfer function of these lines and their time-domain response have been presented for the first time. Using these, a new and computationally efficient performance optimization technique for distributed RLC interconnects has been introduced. The new optimization technique has been employed to analyze the impact of line inductance on the circuit behavior and to illustrate the implications of technology scaling on wire inductance. It is shown that reduction in driver output resistance and input capacitance with scaling can make deep submicron designs increasingly susceptible to inductance effects if global interconnects are not scaled. On the other hand, for scaled global interconnects with increasing line resistance per unit length, as prescribed by the International Technology Roadmap for Semiconductors, the effect of inductance on interconnect performance actually *diminishes*. Additionally, the impact of the wire inductance on catastrophic logic failures and IC reliability issues has also been analyzed.**

***Index Terms*—Inductance, ITRS roadmap, optimal buffering, RLC transmission line.**

I. Introduction

A. Inductance Effects in DSM Interconnects

FOR deep submicron interconnects (DSM), on-chip inductive effects arising due to increasing clock speeds, increasing interconnect lengths, and decreasing signal rise times are a concern for signal integrity and overall interconnect performance [1], [2]. Inductance causes overshoots and undershoots in the signal waveforms, which can adversely affect signal integrity. For global wires inductance effects are more severe due to the lower resistance of these lines, which makes the reactive component $(j\omega L)$ of the wire impedance comparable to the resistive component (R), and also due to the presence of significant mutual inductive coupling between wires resulting from longer current return paths [3]. Furthermore, since the global wires are the farthest from the substrate, they are most susceptible to large variations in the current return path and therefore large variations in the inductance. With the recent adoption of Copper as the very large scale integration (VLSI) interconnect metal [4], [5], line resistances have decreased further and as a result, inductive effects have become more prominent. Hence, the traditional lumped or distributed RC model of the interconnects, especially of the global wires, may no longer be adequate since it can result in substantial errors in predicting both delay and crosstalk [6].

Line inductance affects the circuit performance in two distinct ways. Firstly, it can affect the rise/fall time (slew rate) and signal delay/integrity through an interconnect. Traditional delay models of interconnects are based on Elmore delay [7] which does not take into account the inductance of the interconnect. If the line inductance is "small enough," the step response is very similar to the step response obtained by ignoring the inductance and therefore Elmore delay predictions are accurate. However, as the line inductance increases beyond a certain value, the actual delay and Elmore delay diverge and one needs to compute signal delay by accurately modeling line inductance.

Secondly, a VLSI interconnect can be viewed as a lossy distributed RLC transmission line with a characteristic impedance of $Z_0 = \sqrt{(r+sl)/(sc)}$ where r, l, and c are the line resistance, inductance, and capacitance per unit length respectively, and s is the complex frequency $(j\omega)$. If the series output impedance of the driver and the input impedance of the receiver are equal to Z_0, then according to the transmission line theory, there are no reflections present in the system. However, in a practical VLSI circuit, the input impedance of loads is almost exclusively capacitive. Also, the driver size is typically optimized for delay minimization and its output impedance may not necessarily be equal to Z_0. Therefore, in such systems, line inductance may give rise to reflections which result in overshoots and undershoots in voltage waveforms. Voltage overshoot may cause reliability concerns in the circuit, whereas undershoot will, in the best case, cause glitches and, in the worst case, cause false transitions at the output of a gate. Glitches increase the dynamic power dissipation, while false transitions can cause logic errors and severe timing violations. Therefore, it is not only important to precisely compute the inductance of VLSI interconnects, but it is even more critical to analyze their impact on circuit performance and its optimization.

In the past a lot of research effort has been devoted to the areas of inductance computation [2], [8], [9], inductance extraction using both numerical and experimental techniques [2], [10]–[16], and modeling of on-chip inductance [2], [17]–[19] in integrated circuits. However, accurate estimation and modeling of inductance in VLSI interconnects still remains a challenging problem. Since magnetic fields have a much longer spatial range compared to that of electric fields, in practical high-performance

Manuscript received March 24, 2001; revised January 23, 2002. This paper was recommended by Associate Editor R. Saleh.

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Publisher Item Identifier 10.1109/TCAD.2002.800459.

ICs containing several layers of densely packed interconnects, the wire inductances are sensitive to even distant variations in the interconnect topology [12]. Secondly, uncertainties in the termination of neighboring wires can significantly affect the signal return path and the return current distributions and therefore the effective inductance. Although the effective wire inductances in complex three–dimensional (3-D) interconnect structures can be obtained by rigorous electromagnetic field solvers [10], [12], the results are at best approximate for real high-performance VLSI circuits due to the uncertainties in providing valid models of the local physical and electromagnetic environment formed by the orthogonal and parallel interconnects. Also, accurate estimation of effective inductance values requires details of the 3-D interconnect geometry and layout, technology information such as metal resistivity, insulator dielectric constant, etc., and of the current distributions and switching activities of the wires, which are difficult to predict *a priori*. Moreover, at high frequencies the line inductance is also dependent on the frequency of operation.

However, as pointed out earlier, it is extremely crucial to quantify the impact of inductance on the performance of global interconnects and its optimization using repeater insertion, which in turn determines the chip performance. Furthermore, it is of the utmost importance to understand the degree by which future DSM technologies would be impacted by interconnect inductance effects.

B. Scope of This Study

In this work, the transfer function and the time-domain response of a realistic driver–interconnect–load configuration have been presented based on a rigorous analysis [20], [21] in Section II. It is shown in Section III that the driver resistance and output parasitic capacitance have a significant effect on the waveform and delay and must be included for accurate analysis of a realistic driver–interconnect–load structure. Based on the new delay model, a novel methodology for optimum repeater insertion for a distributed RLC interconnect is presented in Section IV. Unlike previous such attempts, our approach is based on the analytical minimization of interconnect delay per unit length. We show that optimum repeater sizes and interconnect lengths can be efficiently computed for given technology and interconnect parameters. In Sections V and VI, we use this methodology to compute the optimum buffer sizes and interconnect lengths for a wide range of line inductances for the ITRS technology nodes. We also show that reduction in minimum-sized driver output resistance and input capacitance with device scaling is primarily responsible for increasing susceptibility of VLSI designs to inductance effects (Section VII) and that these effects can be mitigated to a large extent by scaling the global interconnects with technology. Additionally, the impact of wire inductance on catastrophic logic failure and IC reliability issues has also been analyzed in Section VII.

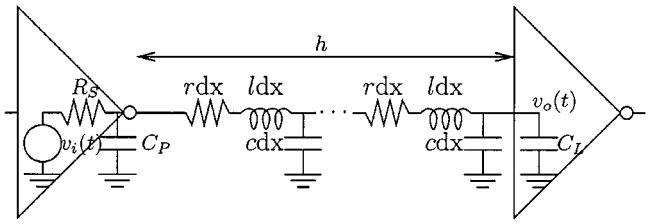

Fig. 1. Equivalent circuit of a driver–interconnect–load segment.

II. Time-Domain Response of a Driver–Interconnect–Load Segment

Consider a uniform line with resistance, capacitance, and inductance per unit length of r, c, and l, respectively, driven by a repeater of resistance R_S and output parasitic capacitance C_P, and driving an identical repeater with load capacitance C_L (Fig. 1). For a given technology, let the output resistance, output parasitic capacitance, and input capacitance of a minimum sized repeater be r_s, c_p, and c_0, respectively. Therefore, if the repeater is k times larger than a minimum sized repeater, $R_S = r_s/k$, $C_P = c_p k$ and $C_L = c_0 k$. For this analysis it is assumed that the repeater resistance and output parasitic capacitance are constant throughout the output voltage transition range.

The ABCD parameter matrix for a uniform RLC transmission line of length h is given by (shown in Appendix):

$$\begin{bmatrix} \cosh(\theta h) & Z_0 \sinh(\theta h) \\ \frac{1}{Z_0}\sinh(\theta h) & \cosh(\theta h) \end{bmatrix}$$

where

$$Z_0 = \sqrt{\frac{r+sl}{sc}}$$

and

$$\theta = \sqrt{(r+sl)sc}.$$

Therefore, the ABCD parameter matrix of the configuration in Fig. 1 is given by the equation shown at the bottom of the page. The input–output transfer function [20] is given by (1), shown at the bottom of the next page.

The step-response of this system is given by $V_o(s) = (1/s)H(s)$ in the Laplace domain. The denominator in (1) can be expressed as an infinite power series in s and in theory the time-domain response can be computed. However, this computation is analytically intractable. Kahng and Muddu [22] suggested using a second-order Padé expansion of the transfer

$$\begin{bmatrix} 1 & R_S \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sC_P & 1 \end{bmatrix} \begin{bmatrix} \cosh(\theta h) & Z_0 \sinh(\theta h) \\ \frac{1}{Z_0}\sinh(\theta h) & \cosh(\theta h) \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sC_L & 1 \end{bmatrix}$$
$$= \begin{bmatrix} (1+sR_SC_P)[\cosh(\theta h)+sC_LZ_0\sinh(\theta h)]+\frac{R_S}{Z_0}\sinh(\theta h)+sC_LR_S\cosh(\theta h) & (1+sR_SC_P)Z_0\sinh(\theta h)+R_S\cosh(\theta h) \\ sC_P[\cosh(\theta h)+sC_LZ_0\sinh(\theta h)]+\frac{1}{Z_0}\sinh(\theta h)+sC_L\cosh(\theta h) & sC_PZ_0\sinh(\theta h)+\cosh(\theta h) \end{bmatrix}$$

function[1] in order to compute the two-pole time-domain response of the following form:

$$v_o(t) = V_0[1 + a_1 \exp(s_1 t) + a_2 \exp(s_2 t)]$$

for appropriate s_is and a_is. Some fitting parameters were introduced in [23] to modify a_is and s_is in the above expression in order to get better matching with SPICE output.

A rigorous time-domain expression for the output of a distributed RLC interconnect with a driver of arbitrary *series* impedance is derived in [24]–[27] *without* explicitly requiring the computation of the Laplace-domain transfer function. However, for a practical driver, the capacitance from output to ground cannot be modeled as a series impedance, and therefore the expression that they derived cannot be easily adapted for a realistic scenario. It is shown in Section III that the output parasitic capacitance of the driver has a significant impact on the signal delay. Moreover, their delay expression involves Bessel functions and cannot be easily used for driver and interconnect optimization for delay minimization which we present later.

Recall that a lumped RLC circuit with one inductance and one capacitance has a two-pole transfer function. Therefore, the two pole approximation effectively ignores the distributed nature of the RLC interconnect. Therefore, for better accuracy, higher order terms also need to be considered [21]. In this work, we consider a fourth-order Padé expansion of (1), i.e.,

$$H(s) \approx \frac{1}{1 + sb_1 + s^2 b_2 + s^3 b_3 + s^4 b_4} \tag{2}$$

where

$$\begin{aligned}
b_1 =& R_S(C_P + C_L) + \frac{rch^2}{2!} + R_S ch + C_L rh \\
b_2 =& \frac{lch^2}{2!} + \frac{r^2c^2h^4}{4!} + R_S(C_P + C_L)\frac{rch^2}{2!} \\
&+ (R_S ch + C_L rh)\frac{rch^2}{3!} + (C_L lh + R_S C_P C_L rh) \\
b_3 =& \frac{c^3r^3h^6}{6!} + \frac{2c^2rlh^4}{4!} + R_S(C_P + C_L)\left[\frac{lch^2}{2!} + \frac{r^2c^2h^4}{4!}\right] \\
&+ (R_S ch + C_L rh)\left[\frac{lch^2}{3!} + \frac{r^2c^2h^4}{5!}\right] \\
&+ (C_L lh + R_S C_P C_L rh)\frac{rch^2}{3!} + R_S C_P C_L lh \\
b_4 =& \frac{c^2l^2h^4}{4!} + \frac{3c^3r^2lh^6}{6!} + \frac{c^4r^4h^8}{8!} \\
&+ R_S(C_P + C_L)\left[\frac{c^3r^3h^6}{6!} + \frac{2c^2rlh^4}{4!}\right] \\
&+ (R_S ch + C_L rh)\left[\frac{c^3r^3h^6}{7!} + \frac{2c^2rlh^4}{5!}\right] \\
&+ (C_L lh + R_S C_P C_L rh)\left[\frac{lch^2}{3!} + \frac{r^2c^2h^4}{5!}\right] \\
&+ \frac{R_S C_P C_L rch^3}{3!}.
\end{aligned}$$

[1]Their driver–interconnect configuration did not include C_P and included a driver inductance L_S in series with R_S.

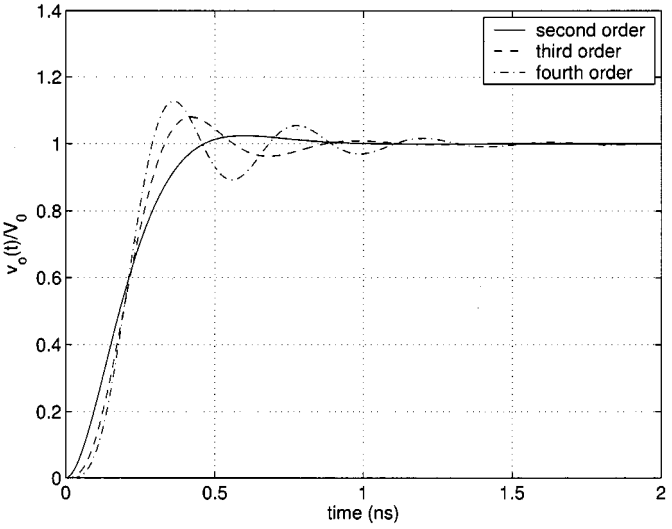

Fig. 2. Second-, third-, and fourth-order response of the driver and interconnect structure of Fig. 1.

The Laplace-domain step-response can be expressed as

$$V_0(s) = V_0\left[\frac{1}{s} + \sum_{i=1}^{4}\frac{d_i}{s - s_i}\right]$$

for appropriate residues (d_is) and poles (s_is), and the time-domain step-response, which is the inverse Laplace-transform of $(1/s)H(s)$, can be calculated as [21]

$$\begin{aligned}
v_o(t) = V_0[1 &+ d_1 \exp(s_1 t) + d_2 \exp(s_2 t) \\
&+ d_3 \exp(s_3 t) + d_4 \exp(s_4 t)].
\end{aligned}$$

Fig. 2 compares the output voltage of the interconnect system in Fig. 1 for a 3.3-mm-long minimum-width metal 6 line for 180-nm technology node (ITRS 1999) with $r = 36\,281\ \Omega$/m, $c = 269$ pF/m, $l = 4\ \mu$H/m, which is driven by an inverter which is 174 times larger than the minimum sized inverter in that technology using a second-, third-, and fourth-order Padé approximation of (1). Note that output waveforms of these three approximations are significantly different and will lead to different time delays. In Fig. 2, it can be noticed that the 60% delay is identical for the three cases. However, this is true only for the specific combination of parameters chosen in this example and

$$\begin{aligned}
H(s) =& \frac{V_o(s)}{V_i(s)} \\
=& \frac{1}{[1 + sR_S(C_P + C_L)]\cosh(\theta h) + \left[\frac{R_S}{Z_0} + sC_L Z_0 + s^2 R_S C_P C_L Z_0\right]\sinh(\theta h)}
\end{aligned} \tag{1}$$

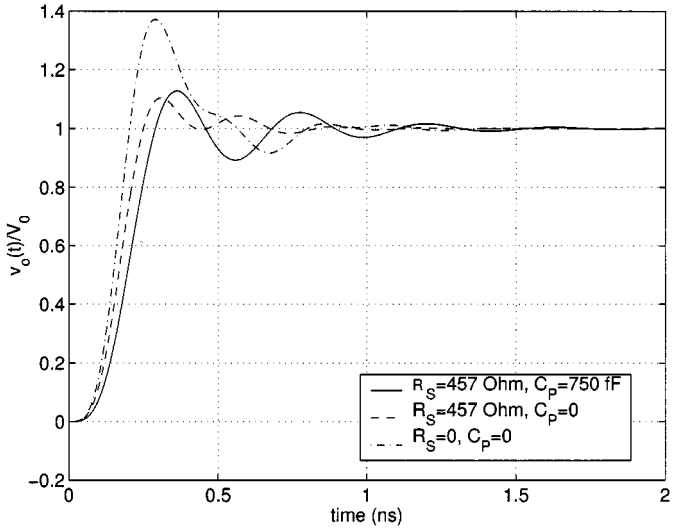

Fig. 3. Step response of the driver and interconnect structure for three cases: 1) R_S and C_P the same as in Fig. 2; 2) $C_P = 0$; and 3) $C_P = 0$ and $R_S = 0$. Other parameters are same as those for Fig. 2.

is not true for any other combination or for other delay fractions. It should be noted that the delay is not a smooth function of l for a fourth-order response. Therefore, if a fourth-order response is used for delay computation and optimization, the resulting optimum interconnect lengths and driver sizes may also not be smooth functions of l. However, the magnitude of the resulting *kink* is very small as will be illustrated later.

III. Effect of Driver Characteristics on Time-Domain Response

Driver resistance R_S and output capacitance C_P have a significant effect on the waveform and delay. Previous analyses have either considered ideal drivers, i.e., ignored both R_S and C_P[23] or ignored C_P [22], [24]–[27]. Ignoring R_S leads to large errors in delay expressions and interconnect length optimization for delay minimization cannot be performed if $R_S = 0$. Ignoring C_P also introduces nonnegligible errors in delay computation if C_P is comparable to C_L and line capacitance. For DSM technologies, the parasitic output capacitance is actually larger than C_L and therefore must also be accounted for. Fig. 3 shows that the step response as well as the delay for distributed RLC lines are significantly affected if R_S or C_P are ignored [21].

IV. Performance Optimization Methodology

Ismail and Friedman [28], [29] presented empirical formulas for finding the optimum buffer size and interconnect length to minimize the delay in an interconnect of a fixed length. An empirical expression for the 50% delay, which was obtained by curve-fitting circuit simulation results, was minimized, and optimized values of repeater size and interbuffer interconnect length were plotted. Using these plots, empirical formulas for optimized values of repeater size and interconnect length were obtained using curve fitting. However, the delay formula is applicable only if the ratio of total line capacitance to load capacitance (ch/c_0k) and the ratio of source resistance to total line

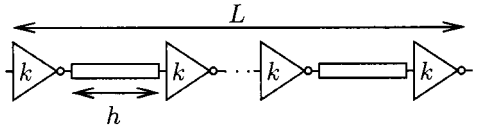

Fig. 4. Long interconnect broken up into buffered segments.

resistance (r_s/krh) is between 0 and 1. Furthermore, C_P is not considered in their formulation which seriously compromises the validity of the curve-fitted parameters.

We now present a new approach [20] of optimizing repeater sizes and interconnect lengths which does not suffer from the limitations of the approach of [28], [29]. In our approach the delay (3) is directly solved using numerical techniques for any values of f without any curve fitting with circuit simulation results.

For a step input, the $f \times 100\%$ (where $0 \leq f < 1$) delay, τ, (i.e., $v(\tau) = fV_0$) is the solution to the following:

$$1 - f + \sum_i d_i \exp(s_i \tau) = 0. \tag{3}$$

For given values of d_is and s_is, the above equation can be solved numerically (for instance, using Newton–Raphson method) to compute the value of τ.

Consider a long interconnect of length L. In order to minimize its delay, the line is broken up into buffered segments of length h, each of which is driven by a buffer of size k and has a delay τ (Fig. 4). The overall delay of the line is given by

$$\text{total delay } = \frac{L}{h}\tau.$$

Therefore, in order to minimize the total delay, we seek to minimize the *delay per unit length* τ/h. Setting the derivative of delay per unit length with respect to h and k to zero we have

$$\frac{\frac{\partial \tau}{h}}{\partial h} = 0 \Rightarrow \frac{\partial \tau}{\partial h} = \frac{\tau}{h} \tag{4}$$

$$\frac{\frac{\partial \tau}{h}}{\partial k} = 0 \Rightarrow \frac{\partial \tau}{\partial k} = 0. \tag{5}$$

Differentiating (3) with respect to h and k and using (4) and (5) we get

$$0 = g_1 = \sum_i \left[\frac{\partial d_i}{\partial h} + d_i \left(\tau \frac{\partial s_i}{\partial h} + \frac{\tau}{h} s_i \right) \right] \exp(s_i \tau) \tag{6}$$

$$0 = g_2 = \sum_i \left[\frac{\partial d_i}{\partial k} + d_i \tau \frac{\partial s_i}{\partial k} \right] \exp(s_i \tau). \tag{7}$$

Equations (6) and (7) can be numerically solved to obtain values of buffer size $k_{\text{opt}_{RLC}}$ and interconnect length $h_{\text{opt}_{RLC}}$ which minimize the delay per unit length [20]. We used the Newton–Raphson method for this purpose and observed that convergence is achieved in less than six iterations in all cases. The computation steps involved in each Newton iteration are as follows.

1) Find b_is, s_is, and d_is[2] and their derivatives w. r. t. h and k.

[2]The expressions of s_i and d_i are fairly tedious and are omitted for clarity.

2) Compute τ by numerically solving (3).
3) Compute $g_{1,2}$ using (6) and (7) and their derivatives w. r. t. h and k.
4) Solve

$$\begin{bmatrix} \frac{\partial g_1}{\partial h} & \frac{\partial g_1}{\partial k} \\ \frac{\partial g_2}{\partial h} & \frac{\partial g_2}{\partial k} \end{bmatrix} \begin{bmatrix} \Delta h \\ \Delta k \end{bmatrix} = \begin{bmatrix} g_1 \\ g_2 \end{bmatrix}.$$

Therefore, this entire optimization step is extremely efficient. Note that the only approximations in the above optimization steps are:

1) use of (2) instead of (1) for the transfer function;
2) constant r_s and c_p for the entire voltage range.

V. Results and Discussion

We now apply our optimization technique to the top-level metal interconnects for 180-, 130-, 100-, 70-, and 50-nm technology nodes as per ITRS specifications [30]. To obtain the interconnect capacitance per unit lenght, full 3-D capacitance extraction of dense wiring networks was performed using FASTCAP [31]. Here, we summarize our results for the 180-nm technology node and point out the salient characteristics of our performance optimization solution. The effect of technology scaling will be addressed in Section VI.

It should be pointed out that a real VLSI interconnect is not an isolated line as shown in Fig. 1 but is embedded in a large multilevel interconnect system. Therefore, a significant amount of coupling, both capacitive and inductive, can exist between interconnects. Typically, interconnects on one layer of metal are routed in one direction, and on the neighboring metal layers interconnects are routed in orthogonal direction. Therefore, there is minimal capacitive coupling between interconnects on adjacent metal layers. Additionally, lines on one metal layer couple only to their two nearest neighboring lines. The effective line capacitance can therefore change due to Miller effect depending on the switching activity on these two nearest neighboring lines. Since the aspect ratios of interconnects in DSM technologies is typically greater than one, effective line capacitance can vary by as much as 4×. However, as pointed out earlier, since magnetic fields have much longer spatial range compared to electric fields, line inductance values are sensitive to switching activities even in distant lines and therefore experience much larger variation and uncertainty in effective line inductance. In our experiments, for simplicity we have assumed that line capacitance is fixed and concentrated on variations in line inductances. These results can be easily modified to incorporate variations in line capacitance as well.

First consider the case of optimum repeater insertion by considering only the line resistance and capacitance and optimizing the Elmore delay. The total Elmore delay of interconnect of length L (Fig. 4) is given by

$$t_{\text{Elmore}} = \frac{L}{h}\left[\frac{r_s}{k}(c_p k + c_0 k) + \frac{r_s}{k}ch + rhc_0 k + \frac{1}{2}rch^2\right].$$

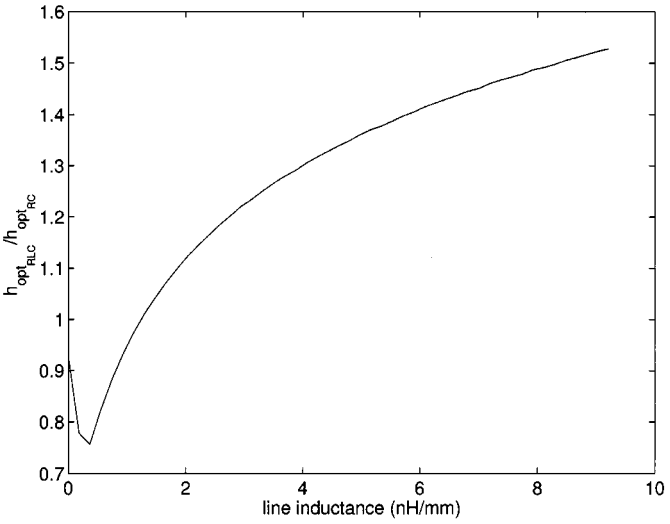

Fig. 5. $h_{\text{opt}_{RLC}}/h_{\text{opt}_{RC}}$ as a function of line inductance for 180-nm technology.

Therefore, the optimum repeater size $k_{\text{opt}_{RC}}$ and interconnect length $h_{\text{opt}_{RC}}$ is given by

$$h_{\text{opt}_{RC}} = \sqrt{\frac{2r_s(c_0 + c_p)}{rc}}$$
$$k_{\text{opt}_{RC}} = \sqrt{\frac{r_s c}{rc_0}}.$$

Furthermore, the delay of one segment of length $h_{\text{opt}_{RC}}$ driven by a buffer of size $k_{\text{opt}_{RC}}$ is given by

$$\tau_{\text{opt}_{RC}} = 2r_s(c_0 + c_p)\left(1 + \sqrt{\frac{2c_0}{c_0 + c_p}}\right).$$

Note that $\tau_{\text{opt}_{RC}}$ is independent of r and c and, therefore, the wiring level. Thus, it can be treated as a technology parameter.

In general, for a given technology, r_s, c_p, and c_0 cannot be easily determined. Moreover, r_s and c_p are voltage dependent. Therefore, for this study, we find $h_{\text{opt}_{RC}}$ and $k_{\text{opt}_{RC}}$ by SPICE simulations. These simulations also provide $\tau_{\text{opt}_{RC}}$. Using the above equations, r_s, c_p, and c_0 can be then determined for that particular technology. Furthermore, for the simulations, we used a ring oscillator, and hence the frequency of the ring oscillator was used for the analysis presented in this paper at a given technology node.

We now show the effect of including line inductance in the optimization as derived in Section IV. It should be noted that l is not a fixed parameter for a given technology and metal layer but depends on the current return path and varies substantially with input vectors. However, a worst case number for line inductance in a dense 3-D interconnect array can be determined as follows: the line inductance would be greatest if the current return path is through the substrate. Let this inductance be $l_{\max}$. We have carried out delay minimization for $0 \leq l < l_{\max}$.

Fig. 5 plots the ratio of the optimum interconnect length $h_{\text{opt}_{RLC}}$ and the interconnect length optimized for Elmore delay, $h_{\text{opt}_{RC}}$. Fig. 6 plots the ratio of the optimum buffer

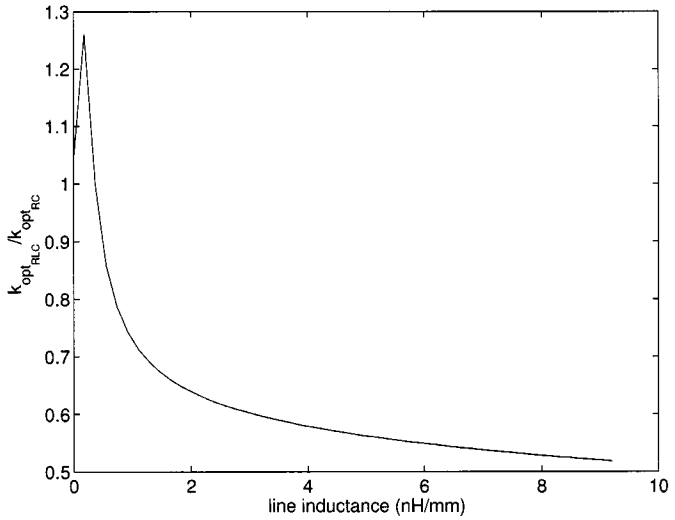

Fig. 6. $k_{\mathrm{opt}_{RLC}}/k_{\mathrm{opt}_{RC}}$ as a function of line inductance for 180-nm technology.

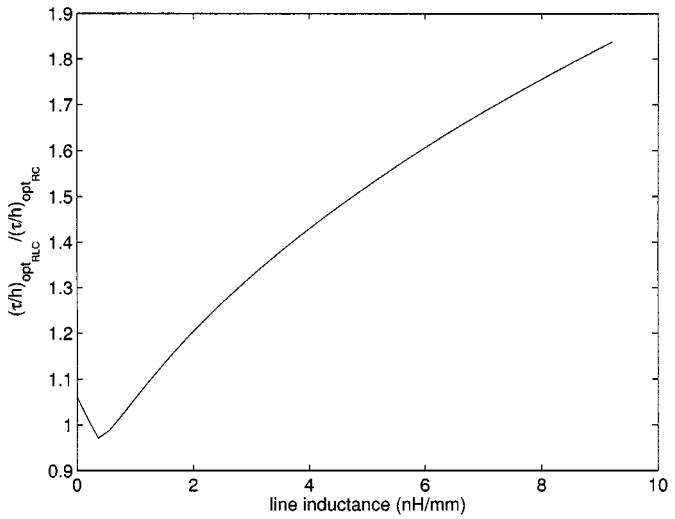

Fig. 7. Ratio of optimum delay per unit length, $(\tau/h)_{\mathrm{opt}_{RLC}}$, and $(\tau/h)_{\mathrm{opt}_{RC}}$ as a function of line inductance l for 180-nm technology.

size $k_{\mathrm{opt}_{RLC}}$ and the buffer size optimized for Elmore delay, $k_{\mathrm{opt}_{RC}}$. These plots also corroborate the observations made in [2] that with increasing line inductance l, the RLC interconnect increasingly resembles an ideal LC transmission line and the delay becomes progressively linear with interconnect length. Therefore, $h_{\mathrm{opt}_{RLC}}$ increases as the line inductance is increased and $k_{\mathrm{opt}_{RLC}}$ reduces and asymptotes to a value for which the driver output impedance is equal to the characteristic impedance of the line. Fig. 7 plots the ratio of optimized interconnect delay per unit length with and without considering line inductance as a function of l. As expected, the optimized interconnect delay per unit length increases as line inductance increases.

As discussed earlier, in a realistic scenario, it is very difficult to predict the effective interconnect inductance because the current return path varies a lot for different input vector patterns. As a result, it is difficult to target a specific value of the line inductance l and optimize the buffer size and interconnect length for

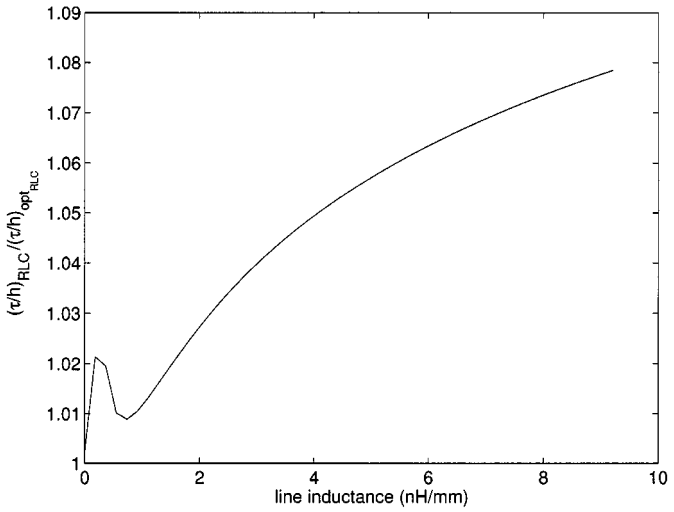

Fig. 8. Ratio of delay of an RLC line with $h = h_{\mathrm{opt}_{RC}}$ and $k = k_{\mathrm{opt}_{RC}}$, and delay corresponding to $h = h_{\mathrm{opt}_{RLC}}$ and $k = k_{\mathrm{opt}_{RLC}}$ as a function of l for 180-nm technology.

TABLE I
TECHNOLOGY AND EQUIVALENT CIRCUIT MODEL PARAMETERS FOR TOP LAYER METAL FOR DIFFERENT TECHNOLOGY NODES BASED ON THE ITRS 1999. t_{ins} IS THE INSULATOR THICKNESS BELOW THE TOP LAYER METAL AND ϵ_r IS THE DIELECTRIC CONSTANT OF THE INTER-LAYER INSULATOR

Tech. node (nm)	180	130	100	70	50
width (nm)	525	382.5	280	195	137.5
height (nm)	1155	1033	756	546	399
t_{ins} (nm)	7699	6664	6022	5571	4116
ϵ_r	3.75	3.1	1.9	1.5	1.25
r (kΩ/m)	36.3	60.1	103.9	206.6	401.3
c (pF/m)	269	240	154	125	106
$l_{\max}$ (nH/mm)	9.2	10.9	13.5	17.9	18.8
$h_{opt_{RC}}$ (mm)	3.33	2.5	2.22	1.32	1.06
$k_{opt_{RC}}$	174	151	110	82	53
$\tau_{opt_{RC}}$ (ns)	0.165	0.147	0.125	0.089	0.071
r_s (kΩ)	8	9.5	10	15.8	12.5
c_0 (fF)	1.9	1.7	1.5	1.3	1.2
c_p (fF)	4.8	3.5	2.5	1.5	0.75

that value of l. Therefore, it is useful to determine the increase in the interconnect delay for a given buffer size and interconnect length as the line inductance l is varied and compare it with the RLC-based optimum delay for the corresponding values of l. As an example, suppose the driver size and interconnect length are chosen to be $k_{\mathrm{opt}_{RC}}$ and $h_{\mathrm{opt}_{RC}}$, respectively, i.e., without considering line inductance. For nonzero l, the RLC delay per unit length of this line would be greater than the RC delay. If l were known beforehand, one could optimize the driver size and interconnect length to potentially get a lower interconnect delay per unit length $(\tau/h)_{\mathrm{opt}_{RLC}}$, as compared to the unoptimized case. Fig. 8 plots the ratio of these two delays as a function of l. For the 180-nm technology the worst case increase in delay

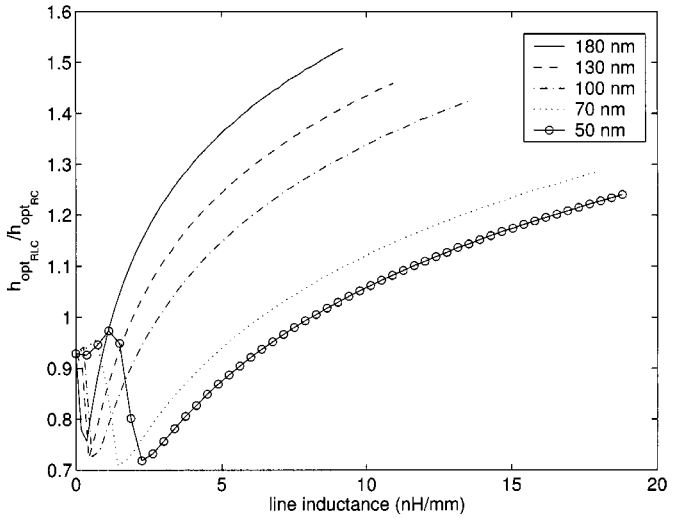

Fig. 9. $h_{\mathrm{opt}_{RLC}}/h_{\mathrm{opt}_{RC}}$ as a function of line inductance l for various technology nodes.

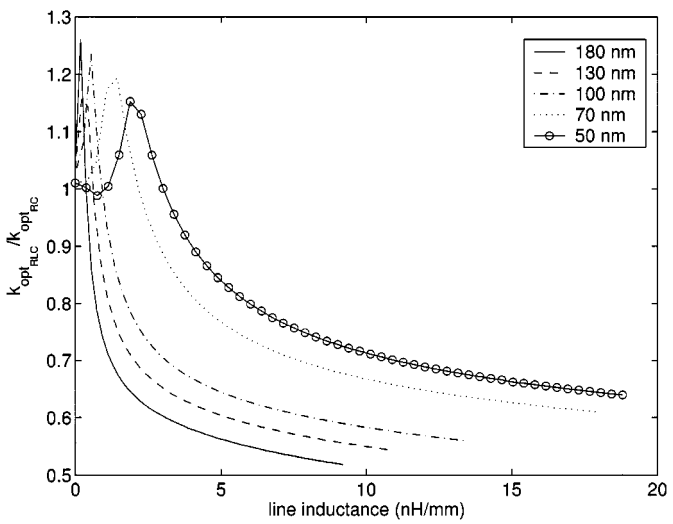

Fig. 10. $k_{\mathrm{opt}_{RLC}}/k_{\mathrm{opt}_{RC}}$ as a function of line inductance l for various technology nodes.

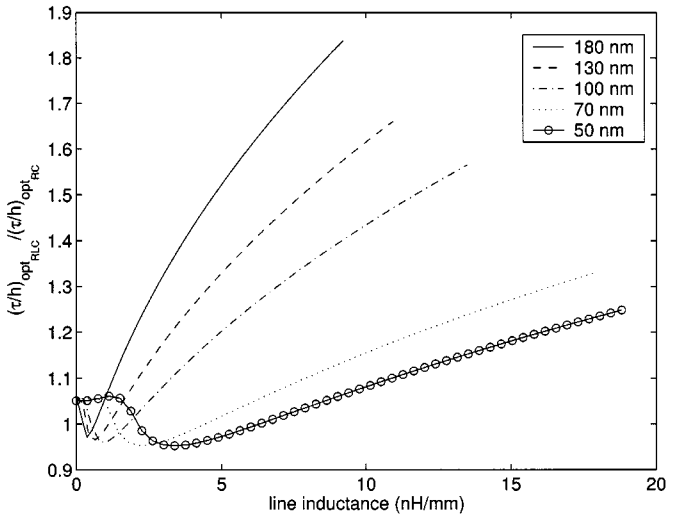

Fig. 11. Ratio of optimum delay per unit length, $(\tau/h)_{\mathrm{opt}_{RLC}}$, and $(\tau/h)_{\mathrm{opt}_{RC}}$ as a function of line inductance l for various technology nodes.

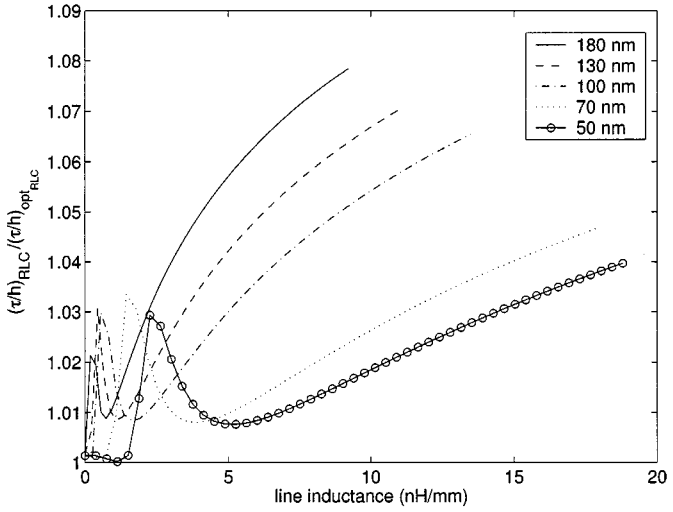

Fig. 12. Ratio of RLC delays per unit length of an interconnect with $h = h_{\mathrm{opt}_{RC}}$ and $k = k_{\mathrm{opt}_{RC}}$ and with $h = h_{\mathrm{opt}_{RLC}}$ and $k = k_{\mathrm{opt}_{RLC}}$ as a function of l for various technology nodes.

over the optimized RLC case is 8%. Therefore, even if the line inductance were known precisely, in the best case, there would be a meager 8% improvement in the delay per unit length [20].

VI. Effect of Technology Scaling

We now consider the effect of inductance with technology scaling. Various technology parameters are shown in Table I and are based on ITRS data. Note that r increases dramatically with scaling as the line dimensions of the top level metal layers also scale. Figs. 9–12 plot the ratios of $h_{\mathrm{opt}_{RLC}}$ and $h_{\mathrm{opt}_{RC}}$, $k_{\mathrm{opt}_{RLC}}$ and $k_{\mathrm{opt}_{RC}}$, $(\tau/h)_{\mathrm{opt}_{RLC}}$ and $(\tau/h)_{\mathrm{opt}_{RC}}$, and the ratio of RLC delay per unit length of an interconnect with $h = h_{\mathrm{opt}_{RC}}$ and $k = k_{\mathrm{opt}_{RC}}$, and RLC delay with $h = h_{\mathrm{opt}_{RLC}}$ and $k = k_{\mathrm{opt}_{RLC}}$ as a function of l, respectively, for various technology nodes. For all these figures, note that effect of inductance on performance is reducing as the technology scales [21]. This is best illustrated by Fig. 11 where we observe that the ratio of optimal RLC delay per unit length to optimal RC delay per unit length becomes closer to one as the technology scales even though $l_{\max}$ is increasing as the technology scales. Similarly, as shown in Fig. 12, the RLC delay per unit length penalty incurred by using the RC optimum repeater size and interconnect length decreases with technology scaling. Another way of visualizing the same phenomenon is to use the concept of critical inductance. For illustration purposes, consider the second-order approximation of the transfer function in (1), i.e.,

$$H(s) \approx \frac{1}{1 + b_1 s + b_2 s^2}.$$

This second-order system is *critically damped*, *overdamped*, and *underdamped* when $b_1^2 - 4b_2$ is equal to, greater than, or less than zero, respectively. The response of an overdamped system is very similar to an RC line, whereas the response of an underdamped system can be considerably different from an RC line. Since b_1 and b_2 are functions of h and k and b_2 is a

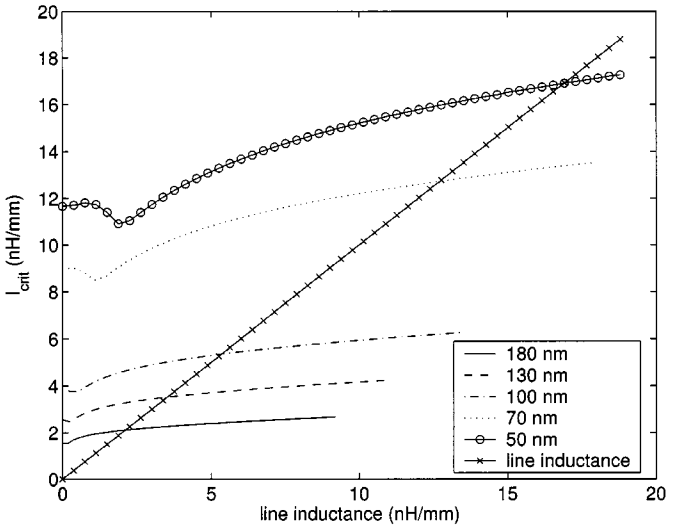

Fig. 13. Critical inductance $l_{\rm crit}$ as a function of line inductance l for various technology nodes.

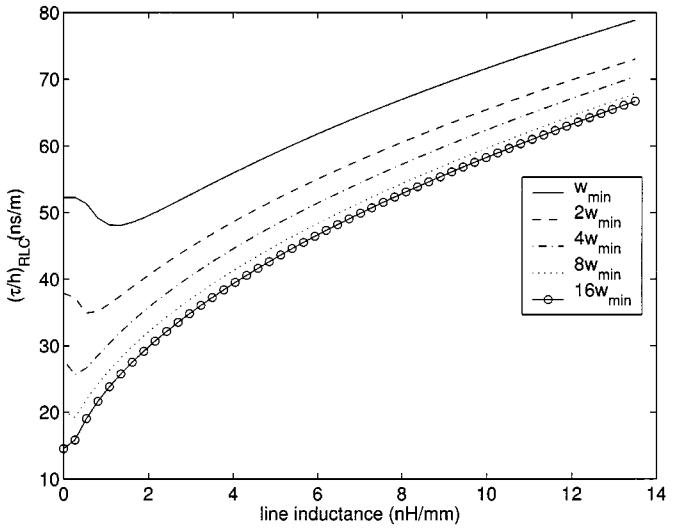

Fig. 14. Delay per unit length for five different line widths for 100-nm technology node as a function of line inductance.

function of l, at $h = h_{{\rm opt}_{RLC}}$ and $k_{{\rm opt}_{RLC}}$, a value $l = l_{\rm crit}$ can be obtained for which

$$b_1^2|_{h=h_{{\rm opt}_{RLC}},k=k_{{\rm opt}_{RLC}}} - 4\, b_2|_{h=h_{{\rm opt}_{RLC}},k=k_{{\rm opt}_{RLC}},l=l_{\rm crit}} = 0$$

i.e., the system will be critically damped. $l_{\rm crit}$ is given by (8) shown at the bottom of the page, where

$$\begin{aligned} b_1 &= b_1|_{h=h_{{\rm opt}_{RLC}},k=k_{{\rm opt}_{RLC}}} \\ h &= h_{{\rm opt}_{RLC}} \\ k &= k_{{\rm opt}_{RLC}}. \end{aligned}$$

Fig. 13 plots this critical inductance as a function of l. Recall that the system is overdamped if $l < l_{\rm crit}$. We find that $l_{\rm crit}$ increases as the technology scales. From Fig. 13, it can also be observed that the overdamped criterion $(l < l_{\rm crit})$ is being satisfied for a bigger range of line inductances as the technology scales, which also implies the diminishing effect of line inductance with technology scaling [21].

The above analysis has been carried out assuming that the width of the topmost metal layer is the minimum width prescribed by the ITRS data. However, to reduce signal delay interconnects, which are wider than the minimum width, are often used in high-performance design. For these lines, the resistance per unit length is smaller and therefore inductive effects can become significant. As an illustration, consider the top layer metal in 100-nm technology node. Five different metal widths are considered: $w_{\rm min}$, $2w_{\rm min}$, $4w_{\rm min}$, $8w_{\rm min}$, and $16w_{\rm min}$. $h_{{\rm opt}_{RC}}$ and $k_{{\rm opt}_{RC}}$ are recomputed for each of these widths. Fig. 14 plots the RLC delay per unit length as a function of l when an interconnect of length $h_{{\rm opt}_{RC}}$ is driven by a buffer of size $k_{{\rm opt}_{RC}}$ for each of these line widths. As expected, for very small values of l, the delay of the wider lines is much smaller but as l increases, the advantage of using wider lines diminishes as the difference between the delays per unit length for different line widths reduces.

VII. Inductance Effects in Unscaled Global Lines

A. Effect of Technology Scaling

Earlier technology scaling predictions, such as NTRS [32], proposed that the metal lines on the topmost metal layer should not be scaled with technology. The main motivation behind this approach was to make sure that delay of these global lines does not increase and adversely affect performance. However, line inductance was not accounted for in these predictions. With technology scaling and increasing clock speeds, the inductive component of the line impedance becomes the dominant factor of the overall line impedance and can adversely affect the performance with scaling. To investigate this phenomenon further, the experiments of Section VI were repeated with the dimensions of global lines fixed at values corresponding to the 180-nm technology, i.e., width of 525 nm, height of 1155 nm, distance from substrate of 7.7 μm, and dielectric constant of the interlayer dielectric of 3.75. Similar to Fig. 12 in Section VI, Fig. 15 plots the ratio of delay per unit length of an RLC line with $h = h_{{\rm opt}_{RC}}$ and $k = k_{{\rm opt}_{RC}}$ and the RLC delay with $h = h_{{\rm opt}_{RLC}}$ and $k = k_{{\rm opt}_{RLC}}$ as a function of l. In sharp contrast to Fig. 12, this ratio increases with technology scaling indicating the increasing importance of inductance effects and the need for taking the line inductance into account for performance optimization. This fact is further corroborated in Fig. 16 which plots the critical inductance as a function of line inductance for different technologies

$$l_{\rm crit} = \frac{\frac{b_1^2}{4} - \frac{r^2c^2h^4}{4!} - R_S(C_P + C_L)\frac{rch^2}{2!} - (R_Sch + C_Lrh)\frac{rch^2}{3!} - R_SC_PC_Lrh}{\frac{ch^2}{2!} + C_Lh} \tag{8}$$

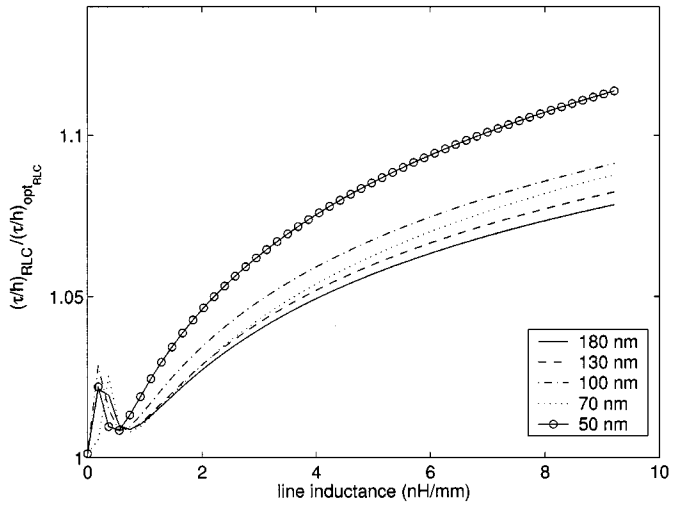

Fig. 15. Ratio of delay corresponding to $h = h_{\mathrm{opt}_{RC}}$ and $k = k_{\mathrm{opt}_{RC}}$ and delay corresponding to $h = h_{\mathrm{opt}_{RLC}}$ and $k = k_{\mathrm{opt}_{RLC}}$ as a function of l for various technology nodes with unscaled global lines.

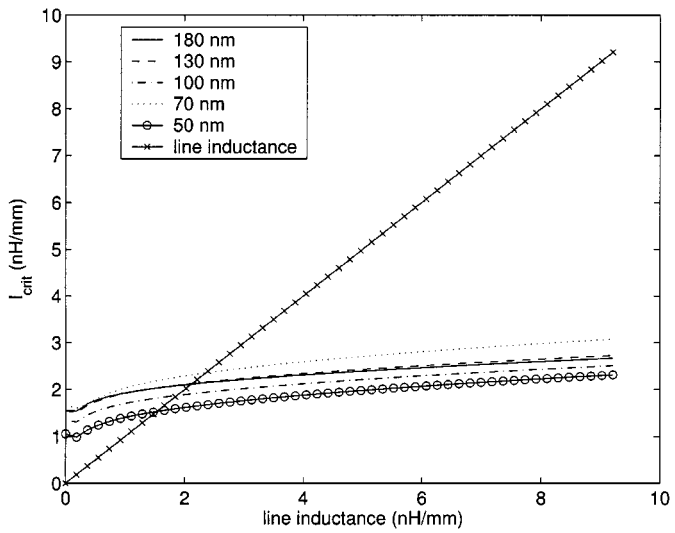

Fig. 16. Critical inductance as a function of line inductance for various technology nodes with unscaled global lines.

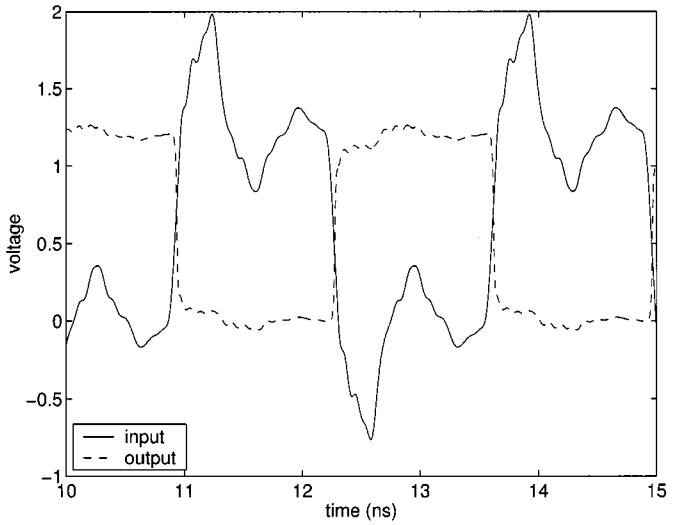

Fig. 17. Voltage waveform at the input and output of an inverter in a five-stage ring oscillator with $l = 1.8$ nH/mm.

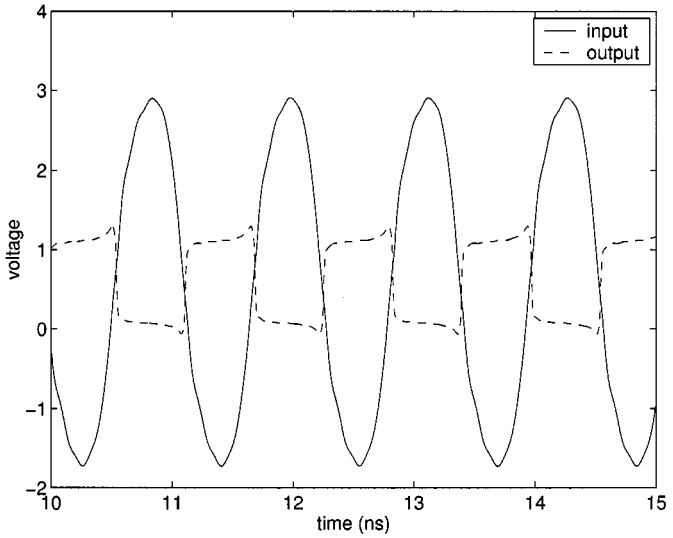

Fig. 18. Voltage waveform at the input and output of an inverter in a five-stage ring oscillator with $l = 2.2$ nH/mm.

with unscaled global lines. It can be observed that for unscaled global lines, the value of l_{crit} *decreases* with scaling, i.e., the line becomes susceptible to inductance effects for a larger range of l [20].

B. Catastrophic Failures Due to Inductance

The decrease in l_{crit} with technology scaling for unscaled global lines implies that the driver–interconnect–load structure is underdamped for a large range of line inductance. As pointed out earlier, the step response of an underdamped system exhibits overshoot and undershoot. This overshoot and undershoot can cause catastrophic failures both in terms of device life–time degradation and errors during the operation of the logic circuits.

1) Logic Failures: As an illustration of this phenomenon, consider a five-stage ring oscillator in the 100-nm technology node in which each stage consists of an inverter of size $k_{\mathrm{opt}_{RC}}$ driving an interconnect of length $h_{\mathrm{opt}_{RC}}$. Fig. 17 shows the voltage waveform at the input and output of an inverter in this ring oscillator obtained from SPICE simulation. The line capacitance is assumed to be 1.8 nH/mm. Note that even though the input waveform shows a significant amount of overshoot and undershoot, the inverter output is relatively "clean." However, if l is increased, the undershoot can become large enough to cause the inverter to switch and since this inverter is a part of a ring oscillator, the false switching propagates throughout the chain and the period of oscillation becomes very small. Fig. 18 shows the voltage waveform at the input and output of an inverter in this ring oscillator with a line inductance of 2.2 nH/mm. Note that with a small increase in l, the period of oscillation is less than half of the corresponding period for $l = 1.8$ nH/mm. To illustrate this phenomenon further, Fig. 19 plots the period of oscillation as a function line inductance. Around $l = 2$ nH/mm, the period drops sharply indicating the onset of false switching in the circuit. A similar behavior was observed for a five-stage buffered RLC line which was excited by a square wave at one

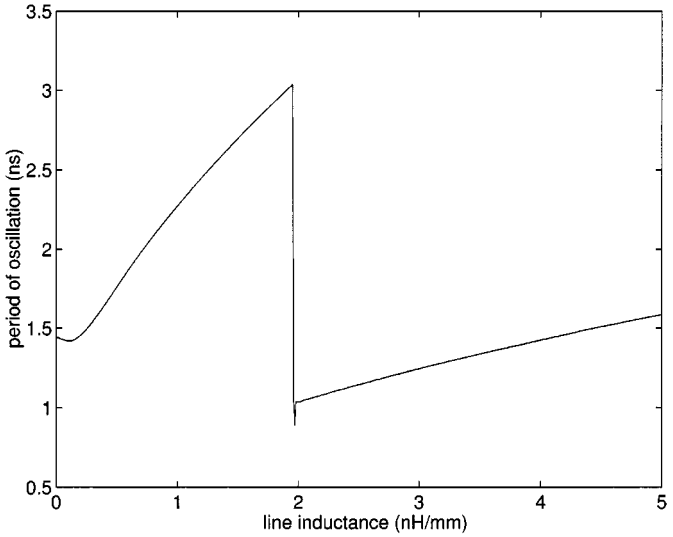

Fig. 19. Period of oscillation for the five-stage ring oscillator as a function of line inductance.

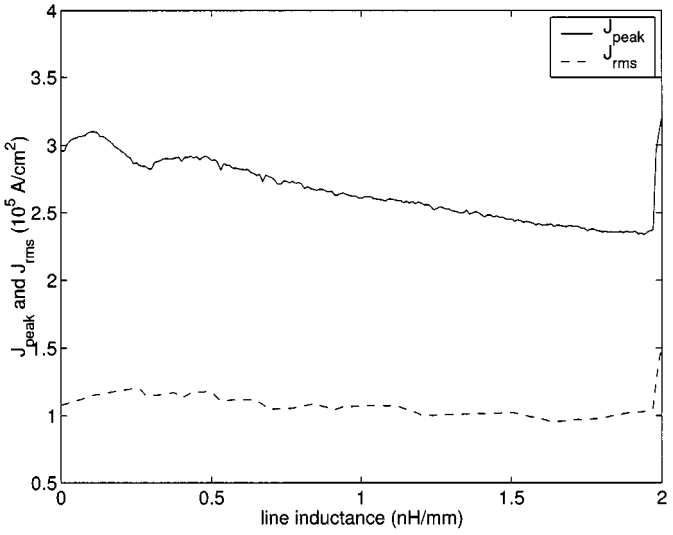

Fig. 20. Peak and rms interconnect densities versus line inductance for 100-nm technology top-level metal using SPICE simulation.

end with the other end connected to an identical repeater. Therefore, this behavior is not an artifact of the ring oscillator configuration. However, for the 180-nm technology node, this phenomenon is not observed for $0 \leq l < 9$ nH/mm. This again indicates that designs in 100-nm technology will be more susceptible to inductance effects as compared to the 180-nm technology designs.

2) Reliability Failures: As shown in Figs. 17 and 18 the voltage at the repeater input is greater than V_{DD} due to overshoot. Since this voltage is applied at the gate of an MOS transistor, this can cause oxide reliability problems [33], [34]. In current technologies the supply voltage is limited by the electric field that can be reliably sustained in the oxide. In DSM technologies, the supply voltage is also scaling with gate oxide thickness in order for the oxide electric field to stay below some critical value [34]. Hence, if the gate voltage is greater than V_{DD} due to overshoot, device reliability can degrade rapidly due to gate oxide wear out.

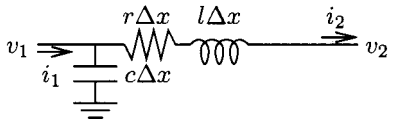

Fig. 21. Infinitesimally small segment of a uniform RLC line.

It was shown in [35] that if interconnect rms and peak current densities increase beyond a certain limit, interconnect reliability can be affected due to increased Joule heating and electromigration of the wire. We, therefore, investigated the effect of line inductance on interconnect reliability. Fig. 20 plots the peak and rms current densities in the interconnect for the five-stage ring oscillator as a function of l. It can be observed that the peak and rms current densities do not change appreciably as l increases to the point of catastrophic logic failure. Therefore, the interconnect reliability does not degrade as the line inductance varies.

VIII. Conclusion

In conclusion, this paper has introduced an accurate analysis of on-chip inductance effects for distributed RLC interconnects. Unlike previous works, the effect of both the series resistance and the output parasitic capacitance of the driver has been taken into account. Using rigorous analysis, accurate expressions for the transfer function of these lines and their time-domain response have been presented for the first time. It is shown that complete driver characteristics must be included in the analysis of distributed RLC interconnect structures for accurately computing their delay. Furthermore, an optimal repeater insertion scheme for distributed RLC interconnects has also been presented using a novel performance optimization technique. Most importantly, the degree of impact of inductance on interconnect performance has been analyzed in detail for future DSM technologies based on the ITRS. Contrary to conventional wisdom, it is shown that the effect of inductance on interconnect performance will actually diminish for scaled global interconnects. However, if global interconnects are not scaled with technology, inductance effects become increasingly dominant and can even lead to catastrophic logic failures and reliability concerns.

Appendix
ABCD Parameters for a Uniform RLC Line

For various reasons it is desirable to derive the ABCD parameters of a uniform distributed RLC line of resistance, capacitance, and inductance per unit length of r, l, and c and length L. First consider a small element of length Δx as shown in Fig. 21. For this circuit

$$\begin{aligned} v_1 &= v_2 + (r + sl)\Delta x i_2 \\ i_1 &= i_2 + v_2 sc\Delta x \\ \begin{bmatrix} v_1 \\ i_1 \end{bmatrix} &= \begin{bmatrix} 1 & (r+sl)\Delta x \\ sc\Delta x & 1 \end{bmatrix} \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} = E \begin{bmatrix} v_2 \\ i_2 \end{bmatrix}. \end{aligned}$$

The advantage of ABCD parameters is that the ABCD parameters of a cascade of two linear systems is the product of ABCD parameter matrices of the individual systems. Therefore, for an

$$\begin{aligned}\begin{bmatrix}1 & a\\ b & 1\end{bmatrix}^n &= \frac{1}{\sqrt{a+b}}\begin{bmatrix}\sqrt{a} & \sqrt{a}\\ \sqrt{b} & -\sqrt{b}\end{bmatrix}\begin{bmatrix}(1+\sqrt{ab})^n & 0\\ 0 & (1-\sqrt{ab})^n\end{bmatrix}\frac{\sqrt{a+b}}{2\sqrt{ab}}\begin{bmatrix}\sqrt{b} & \sqrt{a}\\ \sqrt{b} & -\sqrt{a}\end{bmatrix}\\ &= \frac{1}{2\sqrt{ab}}\begin{bmatrix}\sqrt{a} & \sqrt{a}\\ \sqrt{b} & -\sqrt{b}\end{bmatrix}\begin{bmatrix}\sqrt{b}(1+\sqrt{ab})^n & \sqrt{a}(1+\sqrt{ab})^n\\ \sqrt{b}(1-\sqrt{ab})^n & -\sqrt{a}(1-\sqrt{ab})^n\end{bmatrix}\\ &= \frac{1}{2}\begin{bmatrix}(1+\sqrt{ab})^n+(1-\sqrt{ab})^n & \sqrt{\frac{a}{b}}\left[(1+\sqrt{ab})^n-(1-\sqrt{ab})^n\right]\\ \sqrt{\frac{b}{a}}\left[(1+\sqrt{ab})^n-(1-\sqrt{ab})^n\right] & (1+\sqrt{ab})^n+(1-\sqrt{ab})^n\end{bmatrix}\end{aligned} \tag{A1}$$

$$E^n = \frac{1}{2}\begin{bmatrix}\left(1+\theta\frac{L}{n}\right)^n+\left(1-\theta\frac{L}{n}\right)^n & Z_0\left[\left(1+\theta\frac{L}{n}\right)^n-\left(1-\theta\frac{L}{n}\right)^n\right]\\ \frac{1}{Z_0}\left[\left(1+\theta\frac{L}{n}\right)^n-\left(1-\theta\frac{L}{n}\right)^n\right] & \left(1+\theta\frac{L}{n}\right)^n+\left(1-\theta\frac{L}{n}\right)^n\end{bmatrix} \tag{A2}$$

RLC line of length L with each section of length Δx, the overall ABCD parameter matrix is

$$E^n = \begin{bmatrix}1 & (r+sl)\Delta x\\ sc\Delta x & 1\end{bmatrix}^n \text{ where } n = \frac{L}{\Delta x}.$$

We need to find the limit of the above matrix as $n \to \infty$.

The above limit can be computed in the following manner. Let E be diagonalized as $E = W\Lambda W^{-1}$ where Λ is a diagonal matrix of eigenvalues of E, and W is the eigenvector matrix. Then $E^n = W\Lambda^n W^{-1}$. The matrix E can be diagonalized as

$$\begin{bmatrix}1 & a\\ b & 1\end{bmatrix} = \frac{1}{\sqrt{a+b}}\begin{bmatrix}\sqrt{a} & \sqrt{a}\\ \sqrt{b} & -\sqrt{b}\end{bmatrix}\begin{bmatrix}1+\sqrt{ab} & 0\\ 0 & 1-\sqrt{ab}\end{bmatrix} \times\frac{\sqrt{a+b}}{2\sqrt{ab}}\begin{bmatrix}\sqrt{b} & \sqrt{a}\\ \sqrt{b} & -\sqrt{a}\end{bmatrix}$$

where

$$\begin{aligned}a &= (r+sl)\Delta x\\ b &= sc\Delta x.\end{aligned}$$

Therefore, E^n can be written as (A1), shown at the top of the page. Let

$$\begin{aligned}Z_0 &= \sqrt{\frac{b}{a}} = \sqrt{\frac{r+sl}{sc}}\\ \theta &= \sqrt{(r+sl)sc} = \frac{\sqrt{ab}}{\Delta x} = \frac{\sqrt{ab}}{\frac{L}{n}}.\end{aligned}$$

Substituting these in (A1), the expression for E^n becomes (A2), shown at the top of the page. Using the identity

$$\lim_{n\to\infty}\left(1+\frac{x}{n}\right)^n = \exp(x)$$

it follows that the ABCD parameter matrix for a distributed RLC transmission line of length L is given by

$$\begin{bmatrix}\cosh(\theta L) & Z_0\sinh(\theta L)\\ \frac{1}{Z_0}\sinh(\theta L) & \cosh(\theta L)\end{bmatrix}.$$

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