Analysis of On-Chip Spiral Inductors Using the Distributed Capacitance Model

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***Abstract*—In this paper, a distributed capacitance model (DCM) for monolithic spiral inductors is developed to predict the equivalent capaciting coupling capacitances C_p between the two terminals and the equivalent capacitance between the metal track and the substrate $C_{\rm sub}$. Therefore, the characteristics of inductors such as the S parameter, the quality factor Q, and the self-resonant frequency $f_{\rm SR}$ can be predicted by its series inductance, equivalent capacitances, and series resistance. A large number of inductors have been implemented in 0.25- and 0.35-μm CMOS processes to demonstrate the prediction accuracy. For planar and multilayer inductors, DCM can provide a quick and accurate assessment to the design of monolithic spiral inductors.**

***Index Terms*—Distributed capacitance model (DCM), miniature three-dimensional inductor, on-chip inductor, stacked inductor.**

I. Introduction

MONOLITHIC inductors have been developed for a long time, and their characteristics, including loss mechanism, inductance, etc., have been surveyed in detail. This is one of the key components that determines the performance of RF circuits such as the noise figure of low-noise amplifiers [1], the phase noise of oscillators [2], etc. Until now, the monolithic inductor modeling focused on the analysis of the series inductance L_s and series resistance R_s rather than parasitic capacitances in the inductor. With higher operating frequencies, the parasitic capacitances will affect inductors more significantly. In this brief, distributed capacitance models (DCMs) of inductors are developed to accurately quantify the equivalent capacitive coupling capacitances C_p between the two terminals and the equivalent capacitance between the metal track and the substrate $C_{\rm sub}$.

II. Characteristics of On-Chip Spiral Inductor

A monolithic inductor can be simply modeled as shown in Fig. 1, where L_s is the inductance, R_s is the series resistance, and $R_{\rm sub}$ is the substrate resistance. The one-port inductor model not only avoids unnecessary complexity but also preserves the inductor characteristics. The quality factor Q of an inductor is an important parameter, which significantly affects the performances of RF circuits and systems. Thus, the Q is the most commonly quoted performance parameter of an inductor. The self-resonant frequency $f_{\rm SR}$ can be defined as the frequency while Q drops to zero. The impedance of the inductor becomes capacitive if the operation frequency exceeds the $f_{\rm SR}$. The Q of an inductor can be defined as [3]

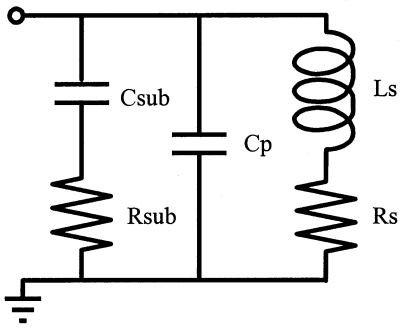

Fig. 1. Compact on-chip inductor model.

$$Q = 2\pi \cdot \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy loss in one oscillation cycle}} = \frac{\mathrm{Im}(Z_L)}{\mathrm{Re}(Z_L)}. \quad (1)$$

III. Distributed Capacitance Model

Z_L can be calculated by inductor parameters such as L_s, R_s, C_p, $C_{\rm sub}$, and $R_{\rm sub}$. The series inductance L_s has been studied for a long time, and there are many methodologies to calculate L_s, such as Greenhouse's formula [4], empirical expressions [5], ASITIC [6], and physics-based closed-form expression [7]. While these literatures and simulators have addressed various highly accurate methodologies to calculate inductance value, there are fewer papers to accurately quantify C_p and $C_{\rm sub}$ in the inductor, which also significantly affect the inductor characteristics especially at high frequencies.

A. Equivalent Capacitance Formula

To accurately quantify C_p and $C_{\rm sub}$ in inductors, the proposed DCM can analytically calculate them rather than qualitatively approximate. The fundamental assumptions of DCM can be derived from the voltage distribution over the inductor, which is called voltage profile in [8]. For simplicity, the following assumptions are made.

1) The wiring metal width is much larger than the spacing, i.e., when one calculates the inductor's area and length, one can ignore spacing.
2) Voltage distribution is proportional to the lengths of the metal tracks, i.e., if the metal track is longer, the voltage drop on the track is larger [8].

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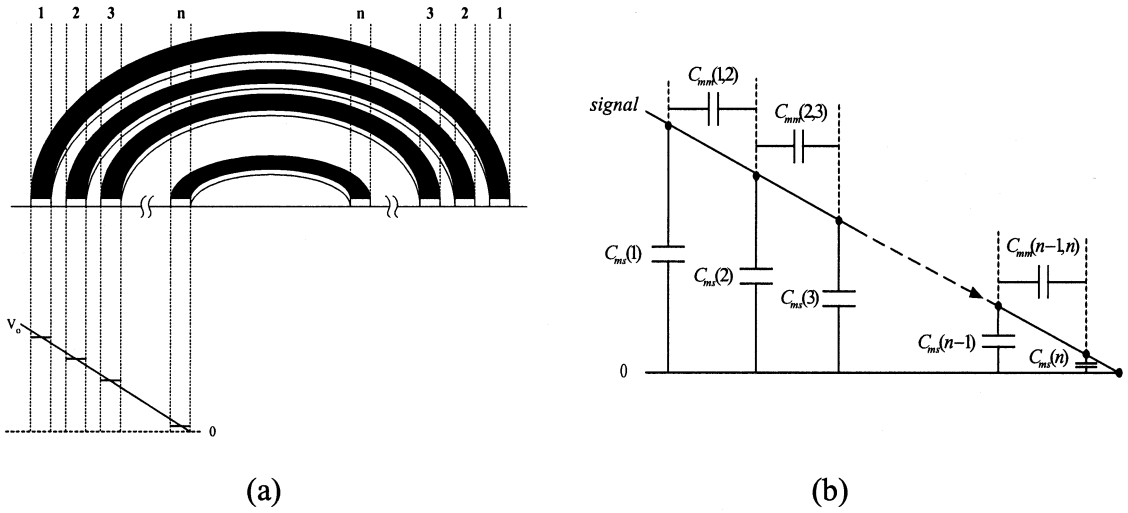

Fig. 2. (a) Voltage profile. (b) Distributed capacitance model of the n-turn planar inductor.

3) In the same turn, the voltage is regarded as constant and it is determined by averaging the beginning voltage and the ending voltage of the turn.

In order to generalize the equivalent capacitance formula, suppose that a planar inductor has inner radius r, metal width w, and n turns. The voltage profile across the planar inductor is shown in Fig. 2(a), where the outermost turn is numbered as first turn and the innermost turn is numbered as nth turn, and the top metal layer is regarded as mth metal layer.

First, the lengths of each turn can be defined as $l_1, l_2, \ldots, l_n$, and the total length is defined as $l_{\text{tot}}(= l_1 + l_2 + \cdots + l_n)$. Each track area is defined as $A_1, A_2, \ldots, A_n$, from first to nth turn.

As shown in Fig. 2(a), the beginning voltage $V(k)_{\text{beg}}$ and the ending voltage $V(k)_{\text{end}}$ of the kth turn can be expressed as

$$V(k)_{\text{beg}} = V_0\,(1 - (h_1 + h_2 + \cdots + h_{k-1})) \tag{2a}$$
$$V(k)_{\text{end}} = V_0\,(1 - (h_1 + h_2 + \cdots + h_{k-1} + h_k)) \tag{2b}$$

where $h_k \equiv (l_k/l_{\text{tot}})$ and V_0 is given as the applied voltage across the inductor.

According to assumption 3, the voltage of the kth turn of the planar inductor can be derived as

$$\begin{aligned} V(k) &= \tfrac{1}{2}\,[V(k)_{\text{beg}} + V(k)_{\text{end}}] \\ &= \tfrac{1}{2}\,V_0\,[2 - (h_1 + h_2 + \cdots + h_{k-1}) \\ &\qquad - (h_1 + h_2 + \cdots + h_k)] \\ &= \tfrac{1}{2}\,V_0\,[2 - d(k-1) - d(k)] \end{aligned} \tag{3}$$

where $d(k) \equiv h_1 + h_2 + \cdots + h_{k-1} + h_k$. So, the electrical energy stored in the capacitor between the kth turn metal layer and the substrate can be expressed as

$$\begin{aligned} E_{c,ms}(k) &= \tfrac{1}{2}\,C(k) \cdot V(k)^2 \\ &= \tfrac{1}{2}\,C_{ms}A_k \cdot V(k)^2 \end{aligned} \tag{4}$$

where C_{ms} represents the capacitance per unit area between the mth metal layer and the substrate. The voltage difference between the kth and $(k+1)$th turn can be expressed as

$$\begin{aligned} \Delta V(k,\, k+1) &= V(k) - V(k+1) \\ &= \tfrac{1}{2}\,V_0\,[d(k+1) - d(k-1)]. \end{aligned} \tag{5}$$

Thus the electrical energy stored in the capacitor between the kth and $(k+1)$th turn can be expressed as

$$\begin{aligned} E_{c,\,mm}(k) &= \tfrac{1}{2}\,C(k) \cdot \Delta V(k,\, k+1)^2 \\ &= \tfrac{1}{2}\,C_{mm}l_k \cdot \Delta V(k,\, k+1)^2 \end{aligned} \tag{6}$$

where C_{mm} represents the capacitance per unit length between adjacent metal tracks. The electrical energy stored in the equivalent capacitor of the inductor can be divided into two parts: one is in the metal-to-metal capacitor, i.e., $E_{c,\,\text{metal–metal}}$, and the other is in the metal-to-substrate capacitor, i.e., $E_{c,\,\text{metal–sub}}$, and it can be derived as

$$\begin{aligned} E_{c,\,\text{total}} &= \tfrac{1}{2}\,C_{\text{eq}}V_0^2 \\ &= E_{c,\,\text{metal–metal}} + E_{c,\,\text{metal–sub}} \\ &= \sum_{k=1}^{n-1} E_{c,\,mm}(k) + \sum_{k=1}^{n} E_{c,\,ms}(k) \\ &= \tfrac{1}{2}\,C_pV_0^2 + \tfrac{1}{2}\,C_{\text{sub}}V_0^2. \end{aligned} \tag{7}$$

Thus, the DCM of a planar inductor is as shown in Fig. 2(b), and the equivalent capacitances C_p and C_{sub} are derived. They can be expressed as

$$C_p = \sum_{k=1}^{n-1} \tfrac{1}{4}\,C_{mm}l_k\,[d(k+1) - d(k-1)]^2 \tag{8a}$$
$$C_{\text{sub}} = \sum_{k=1}^{n} \tfrac{1}{4}\,C_{ms}A_k\,[2 - d(k-1) - d(k)]^2. \tag{8b}$$

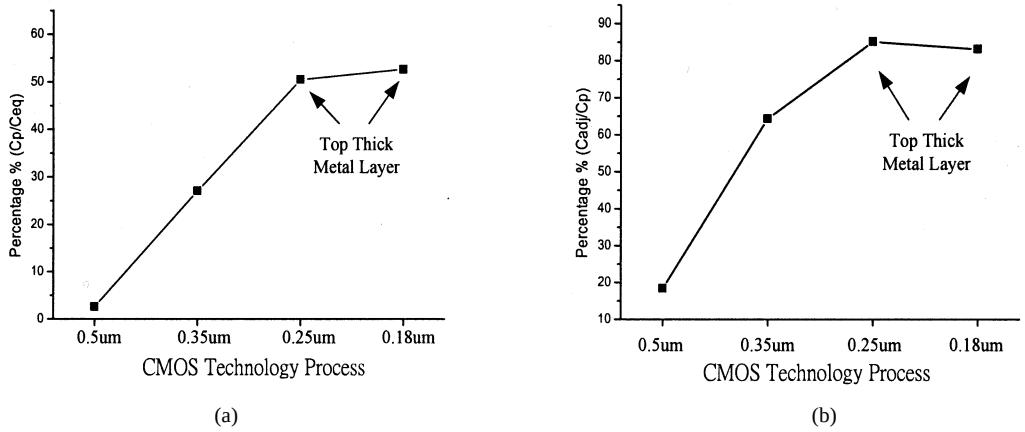

Fig. 3. Simulation results. (a) $C_p/C_{\rm eq}$. (b) $C_{\rm adj}/C_p$.

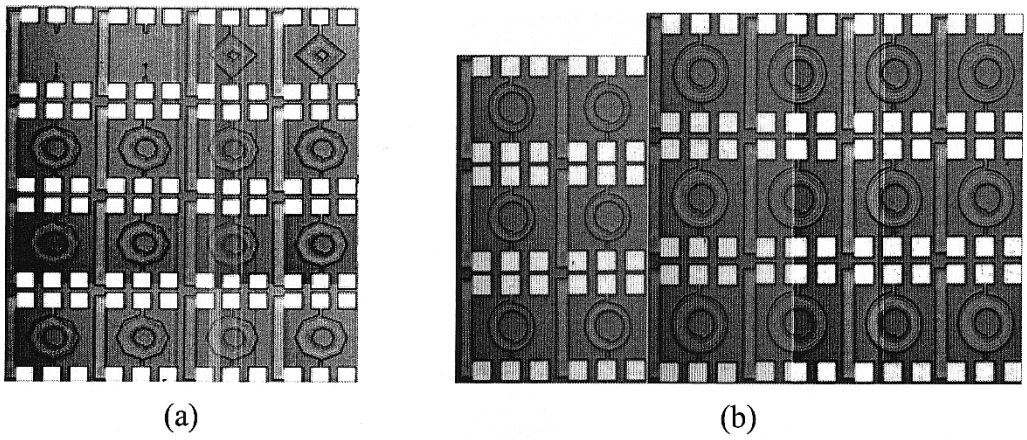

Fig. 4. Die photos of the inductors in: (a) 0.35-μm and (b) 0.25-μm CMOS processes.

Referring to (7), the total equivalent capacitance of the planar inductor can be expressed as

$$C_{\rm eq} = \sum_{k=1}^{n-1} \tfrac{1}{4}\, C_{mm} l_k \left[d(k+1) - d(k-1)\right]^2 + \sum_{k=1}^{n} \tfrac{1}{4}\, C_{ms} A_k \left[2 - d(k-1) - d(k)\right]^2 . \quad (9)$$

Actually, the inductors have the underneath path for connection. Thus, C_p is composed of adjacent-track capacitance, i.e., $C_{\rm adj}$ and overlap one between the inductor and the underneath path, i.e., $C_{\rm underpass}$, where $C_{\rm underpass}$ can also be calculated by DCM. In the same manner as stacked inductors [8] and miniature three-dimensional (3-D) inductors [9], the total parasitic capacitance C_p and $C_{\rm sub}$ can be accurately quantified.

Without DCM, C_p and $C_{\rm sub}$ of a planar inductor can be commonly treated as [10]

$$C_p = n \cdot w^2 \cdot C_{m,\,m-1}$$
$$C_{\rm sub} = \tfrac{1}{2} \cdot w \cdot l_{\rm total} \cdot C_{ms} \quad (10)$$

where $C_{m,\,m-1}$ is the unit area capacitance between the inductor and the underneath path. With the continuously shrinking metal spacing and thick top metal layer, ignoring the adjacent-track capacitance [11] is no longer valid. For planar inductors using the minimum metal spacing implemented in the top metal layer, with $r = 50$ μm, $w = 10$ μm, and $n = 4$, Fig. 3(a) shows the simulated percentage of C_p over $C_{\rm eq}$ with different processes [12], [13]–[15], and the simulated percentage of $C_{\rm adj}$ over C_p is also depicted in Fig. 3(b). The simulation results clearly demonstrate the adjacent-track capacitance $C_{\rm adj}$ cannot be neglected in deep-submicron process and needs to be accurately quantified to capture the behaviors of inductors.

B. Design Guidelines Obtained From DCM

In the intuitive viewpoint of (1), the total parasitic capacitance in an inductor should be minimized. Based on this standpoint, some design guidelines can be obtained from DCM for planar inductors. In order to reduce $C_{\rm adj}$, the metal spacing of an inductor should not be the minimum metal spacing, which actually plays an important role of C_p in deep-submicron process. Furthermore, to attain a high-Q inductor, the inductor conduction loss can be reduced by increasing metal width. However, the wider metal width drastically increases the parasitic capacitance, thus degrading the self-resonant frequency. These tradeoffs can be accurately evaluated by DCM.

IV. Model Validiation

In order to verify the accuracy, a large amount of planar inductors have been fabricated in a 0.35-μm one-poly four-metal and 0.25-μm one-poly five-metal CMOS processes as shown in

TABLE I
$C_{\rm eq}$ AND $f_{\rm SR}$ OF PLANAR AND STACKED INDUCTORS IN 0.35-μm ($w = 10\ \mu$m, $sp. = 1\ \mu$m, AND $w^* = 15\ \mu$m) AND 0.25-μm ($w = 15\ \mu$m, $sp. = 2.2\ \mu$m) CMOS PROCESSES

Ind. Config.	L(nH)	r	n	Mea. C_{eq}(fF)	Sim. C_{eq} w/i DCM	Sim. C_{eq} w/o DCM	C_{eq} Error w/i DCM	C_{eq} Error w/o DCM	Mea. f_{SR} (GHz)	Sim. f_{SR} w/i DCM	Sim. f_{SR} w/o DCM	f_{SR} Error w/i DCM	f_{SR} Error w/o DCM
0.35-µm Planar	3.4	70	3	47.6	44.1	59.0	7.3%	24.2%	12.5	13.0	11.2	4.0%	11.6%
0.35-µm Planar	4.0	50	4	47.9	45.8	66.7	4.5%	39.2%	11.5	11.7	9.7	2.1%	15.7%
0.25-µm Planar	3.6	90	3	31.7	30.8	44.8	2.8%	41.3%	14.9	15.1	9.8	1.3%	16.1%
0.25-µm Planar	4.3	100	3	35.4	34.3	47.8	3.1%	35.1%	12.9	13.1	8.5	1.6%	14.1%
0.35-µm Stacked	7.3	30	2	54.2	52.4	377.4	3.3%	596.3%	7.8	8.2	3.0	5.1%	61.5%
0.35-µm Stacked	16.7	30	3	90.2	86.3	579.5	4.1%	542.4%	4.1	4.3	1.6	4.8%	60.9%
0.35-µm 3D*	7.5	30	2	31.2	32.5	637	4.1%	1941.6%	10.4	10.0	2.3	4.0%	77.8%
0.35-µm 3D	9.7	40	2	35.3	37.8	471.8	7.1%	1236.5%	8.6	8.0	2.3	6.9%	73.2%

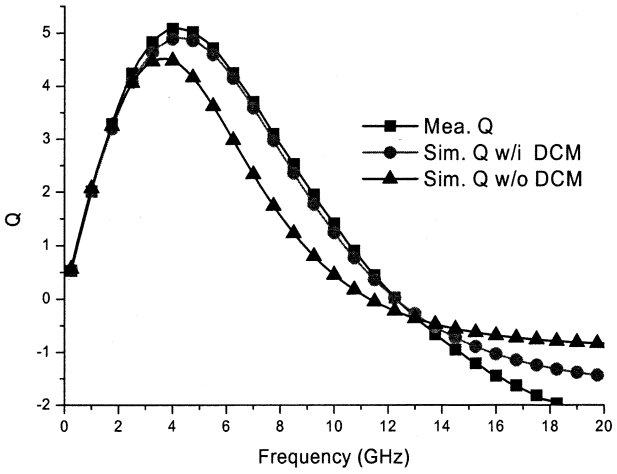

Fig. 5. Measured and simulated Q of the 0.35-μm 3.4-nH planar inductor.

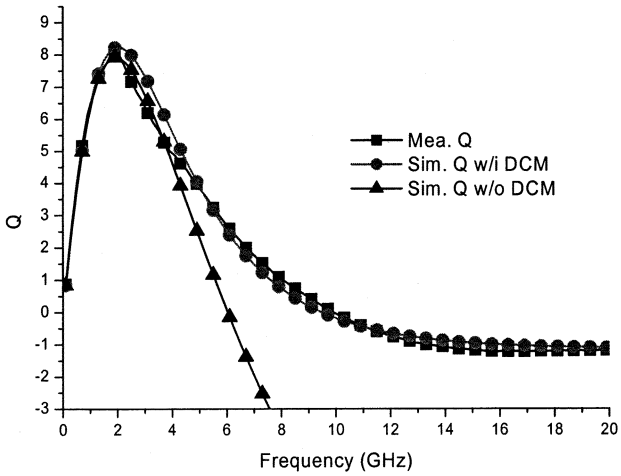

Fig. 6. Measured and simulated Q of the 0.25-μm 6.1-nH planar inductor.

Fig. 4. The prototype chips also include the de-embed pads to calibrate the pad parasitic capacitance [16]. The S parameters were measured by an HP8510C network analyzer and Cascade Microtech Probe Station using coplanar ground–signal–ground probes.

A. Equivalent Capacitance Formula Validation

The self-resonant frequency of an inductor can be determined as $f_{\rm SR} = (2\pi\sqrt{L_{\rm eq}C_{\rm eq}})^{-1}$. In conjunction with inductance value (9), (10) can be applied to calculate the $f_{\rm SR}$. Table I shows the measured and simulated $f_{\rm SR}$ and $C_{\rm eq}$ of planar, stacked, and miniature 3-D inductors [8], [9] for cases with and without DCM to demonstrate the accuracy. The prediction error of $C_{\rm eq}$ with DCM is less than 8%, and the error without DCM is larger than 24%, at least. The prediction error of $f_{\rm SR}$ with DCM is less than 7%, and the error without DCM is larger than 12%, at least.

B. Q Factor Computation and Comparison

According to the compact inductor model, whose L_s and R_s are extracted from measured data [17], the Q of the compact model of inductors can be acquired and are compared to the measured one. Fig. 5 shows the measured and simulated Q with

TABLE II
MEASURED AND SIMULATED Qs OF INDUCTORS IN 0.35-μm ($w = 10\ \mu$m, $sp. = 1\ \mu$m AND $w^* = 15\ \mu$m) AND 0.25-μm ($w = 15\ \mu$m, $sp. = 2.2\ \mu$m) CMOS PROCESSES AT 6 GHz

Ind. Config.	L(nH)	Mea. Q	Sim. Q w/i DCM	Error	Sim. Q w/o DCM	Error
0.35-μm Planar	3.4	4.40	4.31	2.1%	3.20	27.3%
0.35-μm Planar	4.0	4.00	4.20	5.0%	2.64	34.0%
0.25-μm Planar	4.3	5.21	4.85	6.9%	3.51	32.6%
0.25-μm Planar	6.1	2.58	2.39	7.4%	-0.15	105.8%
0.35-μm Stacked	4.9	6.88	6.38	7.2%	-4.95	171.9%
0.35-μm Stacked	7.3	5.15	4.80	6.8%	-6.51	226.4%
0.35-μm 3D*	7.5	3.60	3.94	9.4%	-8.06	323.8%
0.35-μm 3D	9.7	2.71	2.48	8.5%	-6.88	353.8%

and without DCM of the 0.35-μm planar inductor with $r = 70\ \mu$m, $w = 10\ \mu$m, and $n = 3$. Fig. 6 shows the measured and simulated Q with and without DCM of the 0.25-μm planar inductor with $r = 80\ \mu$m, $w = 15\ \mu$m, and $n = 4$. It shows good agreements between the measured and simulated Qs, which are based on the DCM, and the other simulated Qs without DCM do not, especially at high frequencies. Table II shows the measured and simulated Q with and without the DCM to demonstrate the accuracy. The prediction error of Q factor with DCM is less than 9%, and the prediction error without DCM is at least larger than 27% at 6 GHz.

V. CONCLUSION

Below 2 GHz, there is not much deviation between the measured characteristics and the simulated ones with and without DCM. With the higher operating frequency exceeding 3 GHz, the simulated characteristics with DCM still agree well with the measured ones, but the simulated ones without DCM do not. By means of DCM, the adjacent-track capacitance and the inductor-to-substrate capacitance can be quantified accurately rather than estimated qualitatively.

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