Analysis of Optimal Operation Conditions for GaN-based Power Converters

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***Abstract*—The use of Gallium Nitride (GaN) devices allows breaking the performance barriers of conventional silicon-based (Si) low power converters by increasing the operating frequency while reducing system power losses. This paper evaluates the influence of the current ripple, switching frequency and number of GaN devices on the performance of a bi-directional buck converter. Furthermore, hard-switching and soft-switching operation modes are evaluated, identifying the optimal operation conditions for GaN-based power converters. Analytical and simulation models are employed and the obtained results are experimentally validated on a 3 kW GaN-based bi-directional buck converter.**

***Index Terms*—Gallium Nitride, soft-switching, hard-switching**

I. Introduction

The rapid evolution of power electronics results in higher efficiency and higher power density conversion systems. Until recent years, most of these power converters have been developed on silicon (Si) power devices. Even if Si semiconductors present a good balance between performance and cost, the limits in terms of power density, operation temperature, and the switching frequency of Si-based switches are close to be reached [1]. Wide-bandgap (WBG) devices promise to break the performance barriers of conventional Si-based power converters, increasing operating frequency while reducing power losses [1]. In these terms, silicon carbide (SiC) and gallium nitride (GaN) are the most promising materials because of their beneficial properties and current availability. GaN and SiC larger energy gap and better electric field characteristic than Si result in higher breakdown voltage capability for a thinner material. Consequently, the on-state resistance ($R_{ds,on}$) can be reduced, achieving lower conduction losses. Furthermore, although Si presents higher electron mobility than SiC and GaN, the high saturation velocity of WBG devices results in an improvement high switching frequency operation [2].

While SiC devices have already been put into practice for high power applications [3], the trend of GaN devices has been move from microwave solutions [4] to power applications with higher voltage requirements (>200 V), in recent years. The interest of GaN-based transistors is mainly associated with the high electron mobility layer, also known as the two-dimensional electron gas (2DEG). There are mainly three types of GaN switches available: GaN cascode, which is internally built with a low-voltage Si-MOSFET and normally on GaN; insulated gate high-electron-mobility transistor (HEMT); and non-insulated gate injection transistor (GIT).

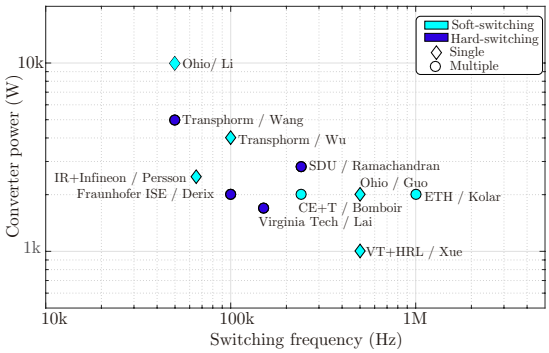


Fig. 1: Power vs. frequency map of GaN-based power converter prototypes proposed in literature.

Referring to GaN-based power converters, GaN devices have been implemented in topologies with soft-switching capability to operate at high switching frequencies (200 kHz - 1 MHz) (see Fig. 1). Topologies such as dual active bridge [5], totem pole [6] or full-bridge [7] are proposed, achieving high power densities (>8 kW/l) as it is presented in [8], [9]. Furthermore, in medium/high power converters (>2 kW), multiple GaN devices are paralleled [10], [11] or interleaved [8], [9], [12]–[14], usually with soft switching operation. However, there is not an established tendency for GaN devices for medium/high power solutions, as it can be observed from Fig. 1.

In this paper, the performance of a GaN-based bi-directional buck converter is evaluated in terms of the inductor current ripple, switching frequency and number of GaN devices connected in parallel. High inductor current ripples will be interesting for interleaved converters, reducing the output current ripple while achieving soft-switching transitions. The main contribution of the paper is the analysis of these design parameters and operation conditions to search the optimal implementation of GaN devices on medium/high power converters. The influence of this operation conditions is theoretically analyzed, and finally verified with experimental measurements.

This work is organized as follows. Section II describes the static and dynamic characteristics of the selected GaN devices. Section III evaluates the design operation conditions influence on the performance of a GaN-based buck converter. Section IV presents the developed GaN-based buck converter prototype, which will be used to validate the results obtained in previous sections. Finally, Section V draws some conclusions about the influence of operation conditions on the performance of GaN-based power converters.

II. GaN devices for power applications

The compact size of these devices makes difficult to operate in high current range (≥ 10 A) without parallel-connected devices, in spite of 60 A announced GaN devices (47 A @100°C). Thus, it is essential to identify the impact of parallelization and operation conditions on the characteristics of GaN devices. For that purpose, a general theoretical analysis is presented for a bi-directional buck converter (see Fig. 2), along with a performance analysis of GaN devices.

A. Thermal management

GaN devices require complex thermal management to extract the heat from such small thermal pad [15]. The device is assumed to be mounted on a heatsink (see Fig. 2), which is at T_{hs} temperature, via thermal interface material (TIM). Then, the losses limit $P_{d,lim}$ of semiconductors is obtained evaluating junction-to-case ($R_{th_{j-c}}$) and case-to-heatsink ($R_{th_{c-hs}}$) thermal resistances.

$$P_{d,lim} = \frac{T_{j,max} - T_{hs}}{R_{th_{j-c}}(A_e) + R_{th_{c-hs}}(A_e)} \tag{1}$$

being $T_{j,max}$ the semiconductor junction temperature limit.

Moreover, $R_{th_{j-hs}}$ and $R_{th_{c-hs}}$ are inversely proportional to the effective area (A_e) of devices, which increases with the number of parallel devices (N_p) (2)

$$\begin{aligned} R_{th_{j-c}}(A_e) &= r_{th_{j-c}}/(A_e \cdot N_p) \\ R_{th_{c-hs}}(A_e) &= r_{th_{c-hs}}/(A_e \cdot N_p) \end{aligned} \tag{2}$$

where $r_{th_{j-c}}$ and $r_{th_{c-hs}}$ are junction-to-case and case-to-heatsink specific thermal resistance (mm^{2}K/W), respectively.

Considering GaN devices with low stray inductance package, i.e. small size packages, the impact of thermal resistances is too high, reducing the thermal cooling capability. Nevertheless, the use of N_p number of devices increases the power dissipation capability for a junction-to-heatsink specific resistance (r_{th_j-hs})

$$P_{d,lim} = \frac{T_{j,max} - T_{hs}}{r_{th_{j-hs}}} \cdot (A_e \cdot N_p) \tag{3}$$

Hence, optimum number of devices has to be considered to satisfy the maximum allowed semiconductor losses for a $T_{j,max}$ design constraint and the minimum power losses.

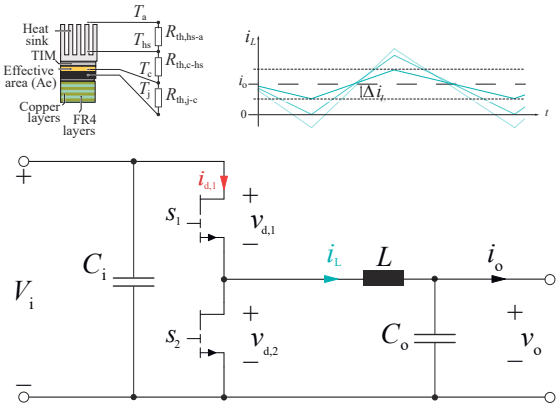


Fig. 2: GaN-based bi-directional buck converter thermal and electrical circuit.

B. Power losses distribution

Regarding power losses of switches, it is a well-known fact that conduction losses are scaled down with N_p number of switches, resulting in lower conduction losses according to (4).

$$P_c = I_{d,rms}^2 \cdot R_{ds,on}(T_j)/N_p \tag{4}$$

where $I_{d,rms}$ is the device RMS current, which is dependent on the average current I_o and current ripple Δi_L (5).

$$I_{d,rms} = \sqrt{I_o^2 + \Delta i_L^2/3} \tag{5}$$

Moreover, during dead-time t_{dt} power switches are reverse conducting, incurring in losses, which can be a limiting factor if the ratio between dead-time and switching period is relevant.

$$P_{dt} = (v_{sd,on} I_{on} + v_{sd,off} I_{off}) t_{dt} f_s \tag{6}$$

where v_{sd} is the reverse drain-to-source voltage drop for the switching currents (I_{on} and I_{off}). These losses will be also relevant for devices with high v_{sd}.

Furthermore, considering a triangular current with an average current I_o (see Fig. 2), I_{on} decreases with the current ripple, while I_{off} switching current increases (7). Thus, the current ripple has not a great influence on total power losses, considering that the reverse voltage variation is not important.

$$\begin{aligned} I_{on} &= I_o - \Delta i_L \\ I_{off} &= I_o + \Delta i_L \end{aligned} \tag{7}$$

Switching losses for a hard-switching transition consist of turn-on and turn-off losses (8), which are proportional to switching frequency f_s and can be scaled by the switched voltage V_d for a reference switching voltage $V_{d,ref}$ [16].

$$P_s(V_d) = [E_{on}(I_{on}, V_{ref}) + E_{off}(I_{off}, V_{ref})] \cdot f_s \cdot \frac{V_d}{V_{ref}} \tag{8}$$

where turn-on (E_{on}) and turn-off (E_{off}) energies are dependent on switching currents I_{on} and I_{off}, respectively.

An approximation of E_{on} and E_{off} for a given V_d voltage can be made using a second order polynomial, considering N_p number of devices.

$$E_s(V_d) = \left(c(V_d) \cdot \left(\frac{I_s}{N_p} \right)^2 + b(V_d) \cdot \frac{I_s}{N_p} + a(V_d) \right) \cdot N_p = \frac{c(V_d)}{N_p} \cdot {I_s}^2 + b(V_d) \cdot I_s + a(V_d) \cdot N_p \tag{9}$$

being I_s the switching current, I_{on} for turn-on and I_{off} for turn-off transient.

Turn-on main losses of GaN devices are related to output capacitance self charging/discharging ($E_{oss}(V_d)$), which are only dependent on V_d, and the overlapping of switching voltage v_d and switching current i_d ($E_{vi}(V_d, I_{on})$) [16]. Reverse recovery energy is negligible for GaN devices, being one of the most relevant characteristic to reduce the impact of turn-on losses on hard-switching operation. Hence, considering this turn-on loss distribution and the second order approximation (9), the term which is independent of the current ($a_{on}(V_d)$) is obtained (10)

$$a_{on}(V_d) \approx Q_{oss}(V_d) V_d \quad \text{where} \quad Q_{oss}(V_d) = \int_0^{V_d} C_{oss}(v_d) dv_d \tag{10}$$

being $C_{oss}(v_d)$ the voltage-dependent parasitic output capacitance, which is the same for high-side and low-side devices. On the contrary, as turn-off transient does not present zero-current losses ($a_{off}(V_d) \approx 0 \mu J$), all turn-off losses are related to the v_d and i_d overlapping.

Moreover, an increase of the current ripple can result on soft-switching operation. If the current ripple is 100% of I_o, zero-current-switching (ZCS) is achieved, being switching losses only related to the output capacitance (E_{oss}). Besides, if the current ripple is increased until I_{on} is negative zero-voltage-switching (ZVS) transition can be accomplished, as long as ZVS operation conditions are fulfilled.

C. Conditions for soft-switching

For ZVS operation it is crucial to specify the conditions under which the ZVS can be achieved. This requires a minimum current ($I_{on,min}$) of the inductive component (L), that charges/discharges output capacitances within the dead-time. The required energy of the inductance for ZVS can be derived for the energy balance (11).

$$\frac{1}{2} L I_{on,min}^2 > \frac{1}{2} N_p (C_{oss_1} + C_{oss_2}) V_d^2 \tag{11}$$

where C_{oss_1} is the high-side switch capacitance and C_{oss_2} the low-side switch capacitance.

Moreover, a resonant analysis of the circuit is performed, in order to define ZVS conditions more precisely during the dead-time. In a buck converter, ZVS is achieved if the switch node voltage of the top device (v_{d1}) excess input voltage V_i, turning-on the body diode of s_1 (see Fig. 2). Then, the minimum current for a ZVS condition is obtained by (12) within a minimum dead-time [17]

$$I_{on,min} > \sqrt{\frac{(C_{oss_1} + C_{oss_2}) V_i (V_i - 2V_o) N_p}{L}}, \tag{12}$$

$$t_{dt,min} = \frac{1}{\omega_o} \left(\tan^{-1} \left(\frac{V_o}{I_{on,min}} \right) + \frac{\pi}{2} \right). \tag{13}$$

However, if conditions presented before are not fulfilled, incomplete ZVS occurs. This means that the top side switch turns-on before the resonant transition with a voltage ΔV_d. As it is analyzed in [18] ΔV_d can be calculated solving the energy balance (11) and then obtaining the delivered energy for the incomplete ZVS

$$E_{\Delta V} = N_p \cdot V_d \cdot (Q_{oss}(V_d) - Q_{oss}(V_d - \Delta V_d)) \tag{14}$$

D. Performance analysis

In this paper the performance of 600 V 30 A GaN GIT devices are analyzed using SPICE models. Forward and reverse conduction characteristics present low conduction resistance for forward conduction but not for open state reverse conduction [see Fig. 3(a)]. Free-wheeling reverse conduction of GaN devices have a higher reverse voltage drop, leading to specially consider an optimal dead-time which minimizes this effect for high-switching frequency operation. Regarding the conduction resistance of the analyzed devices, the analyzed GaN device shows up a low conduction resistance with a positive thermal coefficient, as it is depicted in Fig. 3(a). Thus, in case of paralleling devices, the positive thermal coefficient enables a natural balancing of current sharing through devices.

Switching losses are obtained integrating the ($v_d(t) \cdot i_d(t)$) over turn-on and turn-off switching times. Figure 3(b) presents energy curves for different switching voltages. Considering turn-on and turn-off approximation terms (9), switching energy E_s per device is obtained as a function of Δi_L and N_p.

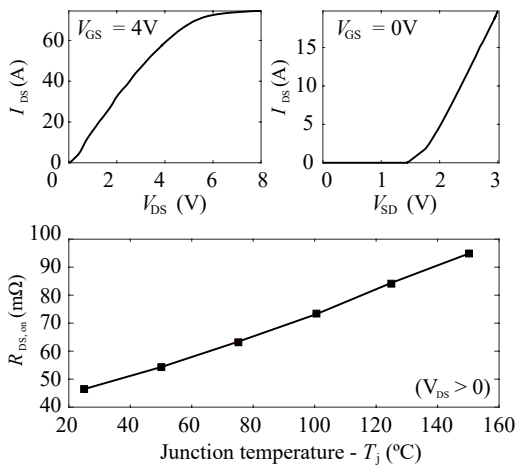
$$E_s = \Delta i_L^2 \frac{c_{off} + c_{on}}{Np} + \Delta i_L \left(2 I_o \frac{c_{off} - c_{on}}{N_p} + b_{off} - b_{on} \right) + \gamma \tag{15}$$

being γ the factor which is independent of the current ripple.

$$\gamma = N_p Q_{oss} V_d + \frac{I_o^2 (c_{off} + c_{on})}{N_p} + I_o (b_{off} + b_{on}) \tag{16}$$

As it can be deduced from Fig. 3(b), turn-on and turn-off energy curves present a linear tendency being $b_{on} >> c_{on}$ and $b_{off} >> c_{off}$. Then, the total switching losses can be approximated to

$$E_s \approx \underbrace{(I_o - \Delta i_L) b_{on} + N_p Q_{oss} V_d}_{E_{on}} + \underbrace{(I_o + \Delta i_L) b_{off}}_{E_{off}} \tag{17}$$



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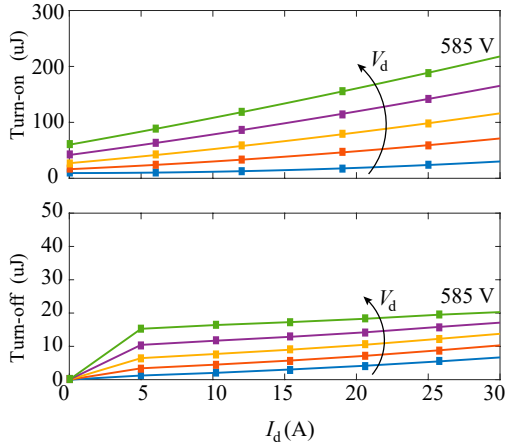


(b)

Fig. 3: GaN GIT device characteristics analysis, based on SPICE models. (a) Forward conduction and reverse open state (V_{GS} = 0 V) conduction characteristic, along with on-state resistance at different junction temperatures. (b) Switching energies at different switching voltages (V_d).

Besides, the total switching losses increment ΔE_s as a function of Δi_L is derived from (17).

$$\Delta E_s \approx \Delta i_L (b_{off} - b_{on}) \tag{18}$$

Thus, if b_{on} is bigger than b_{off}, total switching energies are reduced when Δi_L increases (18). This assumption is valid for GaN switches, which presents higher turn-on than turn-off losses, as it is compared in Fig. 3(b). Furthermore, the switching losses also increase with the output capacitance losses for N_p number of devices (17).

In addition, total power losses difference is obtained as a function of Δi_L and N_p for the same I_o (19).

$$P_d = \frac{R_{ds,on}(T_j)}{N_p}\frac{\Delta i_L^2}{3} + f_s[\Delta i_L (b_{off} - b_{on})] + N_p Q_{oss} V_d \tag{19}$$

An increase of the current ripple results on a reduction of turn-on losses, being possible to achieve ZVS operation. This feature will be interesting for high-switching operation. Nevertheless, with higher current ripple turn-off losses increase, this will be a limiting factor for power devices with high b_{off} (**??**). In addition, the RMS current, and thus conduction losses, also increase with the current ripple, being relevant especially when working at low switching frequencies (19).

Regarding parallelization, the use of parallel devices reduces conduction losses while increasing switching losses. Then, when conduction losses are the most relevant factor for power losses, paralleling devices is presented as the most suitable solution. Besides, the use of parallel-connected devices is also essential for high-switching frequencies, due to the limited thermal cooling capability of such small devices. Thus, in order to increase the cooling capability paralleled devices are used to increase the power losses limit (**??**).

Thus, a trade-off between the power dissipation capability (3) and power losses (19) has to be considered when choosing N_p number of devices. A more detailed evaluation is presented considering the influence of these parameters (Δi_d, f_s, N_p, t_{dt}) on converter level performance.

III. GaN-based power converter design evaluation

The performance of a GaN-based bi-directional buck converter is evaluated for the specifications shown in Table I. The influence of parallelization, current ripple, switching frequency and dead-time of GaN devices is analyzed in this section. Namely, semiconductors devices and inductive components have to be considered for the estimation of power losses, assuming ceramic capacitors with negligible power losses as input and output capacitors (C_i, C_o).

Semiconductors losses are evaluated for an evenly distributed power losses with a conduction resistance at a junction temperature of 120 °C. Regarding switching losses, characteristics obtained from the SPICE model [see Fig. 3(b)] are considered, along with the analytical expressions for soft-switching operation (14).

The current ripple of a buck converter is related to the output inductance L, which is defined by (20):

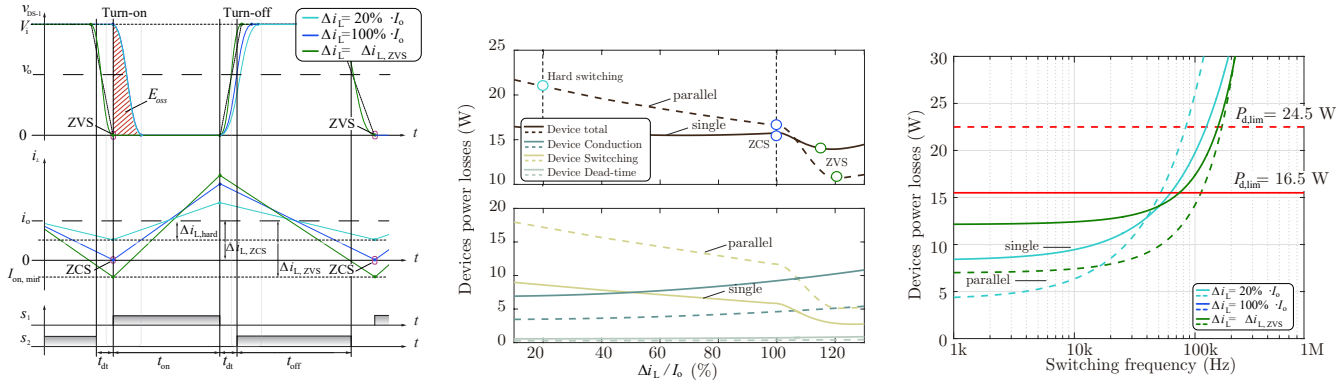
$$\Delta i_L = \frac{V_i(1-\delta)\delta}{2Lf_s} \tag{20}$$

where V_i is the input voltage and δ the duty cycle, providing δ=0.5 the maximum current ripple.

A. Analysis conditions

An analysis of the current ripple and switching frequency influence has been performed comparing single device with two parallel-connected devices.

For the current ripple analysis, a switching frequency of 100 kHz and an output current of 10 A with a duty cycle of 0.7



(a) (b) (c)

Fig. 4: Current ripple and switching frequency influence on a GaN-based bi-directional buck converter: (a) 20%, 100% and $\frac{\Delta i_{L,ZVS}}{I_o}$ comparison, achieving hard switching, ZCS and ZVS, respectively (I_o=10 A). Analysis of devices power losses, comparing single with parallel-connected (dashed lines) GaN devices: (b) varying the current ripple and (c) for different switching frequencies, evaluating the thermal dissipation limit ($P_{d,lim}$).

TABLE I: Bi-directional buck electrothermal specifications.

Description	Symbol	Value	Unit
Input voltage	V_i	350	V
Output voltage	V_o	245	V
Output current	I_o	10	A
Ambient, junction temperature	T_a, T_j	25, 120	°C
Heat-sink-to-ambient resistance	$R_{th,h-a}$	2.25	°C/W
Case-to-heat-sink resistance	$R_{th,c-h}$	2.9	°C/W
Junction-to-case resistance	$R_{th,j-c}$	1	°C/W

are considered. Then, varying the output inductance, different current ripples are achieved (20). Low current ripple (20%) presents hard switching for all the commutations (turn-on and turn-off) whereas the current ripple of 100% reduces turn-on switching losses, due to ZCS condition, as it is depicted in Fig. 4(a). A current ripple higher than 100% reduces even more these losses for specific conditions. A dead-time which ensures ZVS operation for the turn-on current (12) is selected.

Hence, the increase of the current ripple results in different operation modes defining three operation areas: hard switching ($\frac{\Delta i_L}{I_o}$<100%), ZCS ($\frac{\Delta i_L}{I_o}$=100%), and ZVS ($\frac{\Delta i_{L,ZVS}}{I_o}$) [see Fig. 4(a)].

Switching frequency influence is also evaluated under the same operation conditions for the three current ripples which provide three different operation modes: 20%, 100% and >100%.

B. GaN devices performance

Analyzing the power losses of GaN devices, the use of parallel devices for low current ripple results in higher power losses, due to the high relevance of switching losses, as it is depicted in Fig. 4(b). Nevertheless, as current ripple increases, switching losses are reduced and then the use of parallel devices reduces total power losses. For the frequency analysis, as 100% current ripple presents similar performance than low current ripple, only two current ripples are depicted in Fig. 4(c). The increase of the current ripple presents better performance than low current ripple approach, when paralleling devices or/and at high-switching frequencies.

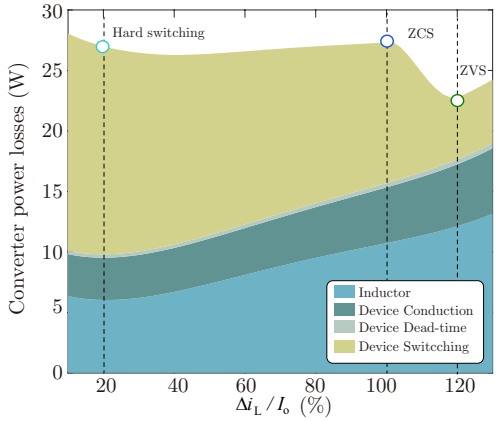
In addition, the power losses limit of single device and paralleled devices is obtained, solving (3) for the specifications presented in Table I. Paralleling GaN switches reduce power losses for low switching frequencies, due to conduction losses reduction (4). However, for higher switching frequencies, although paralleling devices increase power losses, paralleling could be also interesting in high switching frequency due to higher power dissipation capability [see Fig. 4(c)].

C. Power converter performance

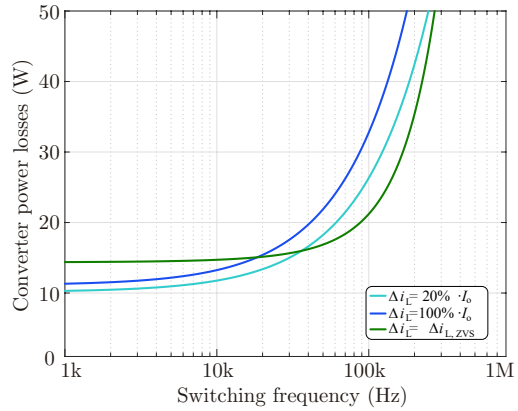
Power devices conduction losses and inductance losses increase with the current ripple, as it is presented in Fig. 4(b). However, switching losses are reduced mainly due to lower turn-on switching currents and the great difference between turn-on and turn-off energy of GaN devices (18). Results show that, for these specifications, the lowest power losses are achieved for Δi_L=$\Delta i_{L,ZVS}$. Figure 4(c) shows that for low switching frequencies (<30 kHz), hard-switching operation presents the lowest power losses due to low current ripple, reducing the high impact of RMS current. However, as the switching frequency increases, switching losses become relevant, being $\Delta i_{L,ZVS}$ the most interesting operation point due to the impact of the output capacitance losses on GaN devices.

IV. Experimental Results

The GaN-based bi-directional buck converter presented in [15] is used to validate the results obtained in previous sections. This converter is composed by a power board based



(a)



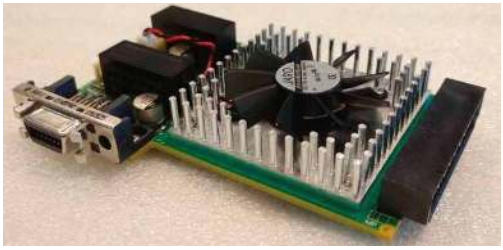
(b)

Fig. 5: Power converter performance analysis: (a) distribution of power losses for different current ripples ($\Delta i_L/I_o$) and (b) comparison of buck converter power losses, varying the switching frequency for the three current ripples.

on two paralleled GaN GIT devices. The gate-loop length is equal for paralleled GaN devices, providing identical turn-on and turn-off times for the two parallel devices. Identical gate resistances circuits are employed in order to drive parallel-connected devices from the same driver and control, keeping a good thermal balancing. Thermography of the power converter under operation shows that there is a minor temperature difference between paralleled devices [see Fig. 6(b)]. Regarding the thermal management, the power board is cooled using PCB capabilities, Cu inlay and heat spreading, achieving a total power dissipation limit of 25.6 W [15].

A. Test setup

In order to validate the theoretical analysis, the influence of different current ripples on power devices is experimentally measured. For a switching frequency of 20 kHz three output inductors are designed to compare the performance of three current ripples. In Fig. 7 the voltage of top device is depicted for three current ripples: 20%, 100% and >100%. Low current



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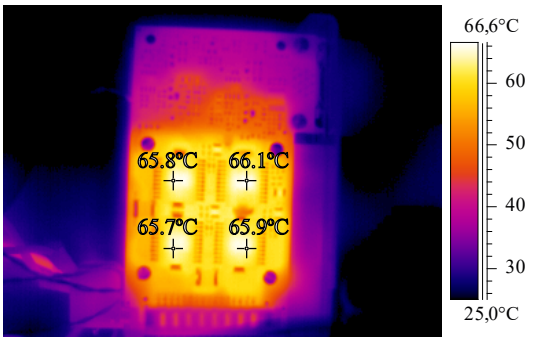

(b)

Fig. 6: GaN-based power converter prototype presented in [15]: (a) modular GaN-based bi-directional buck converter and (b) thermal distribution of GaN switches.

ripple presents a hard-switching transition, as it is depicted in Fig. 7(a). For the 100% current ripple the switch-node voltage is not discharged and thus, a hard-switching transition with ZCS is shown in Fig. 7(b). On the contrary, for the ZVS current ripple, the depicted v_{d1} shows up a complete soft-switching when turning-on the power switch [see Fig. 7(c)].

For the estimation of experimental power losses, heatsink and ambient temperature are measured together with input and output power values. Devices power losses ($P_{d,loss}$) are obtained from the thermal equivalent heat-sink resistance ($R_{th_{hs-a}}$) and the measured heatsink-to-ambient temperature difference ($\triangle T_{hs}$ = T_{hs} - T_a) (21), when the thermal equilibrium is achieved

$$P_{d,loss} = \frac{\triangle T_{hs}}{R_{th_{hs-a}}}. \tag{21}$$

In order to obtain the precise thermal resistance, the measured point has to be calibrated by measurements. Hence, a constant controlled current (I_d) is fed into the power board, measuring $\triangle T_h$ for different controlled power levels. Then, power losses for a measured $\triangle T_{hs}$ are obtained [see Fig. 8(a)]. In addition, the voltage drop of devices has also been measured, in order to obtain $R_{ds_{on}}(T_j)$ and thus, the junction temperature T_j is estimated from the Fig. 3(a). The measured $P_{d,loss}$ consist of conduction P_c, switching P_s and P_{dt} dead-time power losses of devices. Measuring the RMS current of those switches ($I_{d,RMS}$) and with the $R_{ds_{on}}(T_j)$,

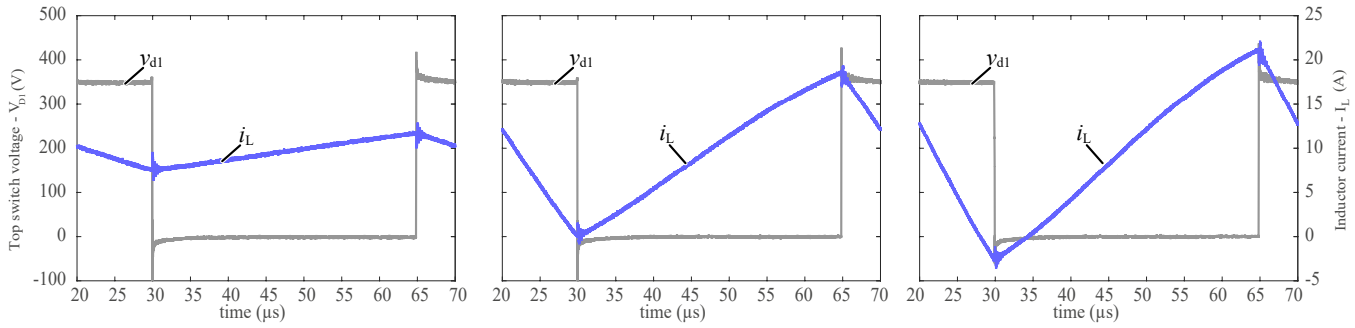

Fig. 7: Experimental measurements with different current ripples: (a) 20%, (b) 100%z and (c) $\frac{\Delta i_{ZVS}}{I_o}$.

conduction losses are known and hence the switching losses plus dead-time losses are calculated

$$P_s + P_{dt} = P_{d,loss} - R_{DS_{on}}(T_j) \cdot I^2_{d,RMS}. \tag{22}$$

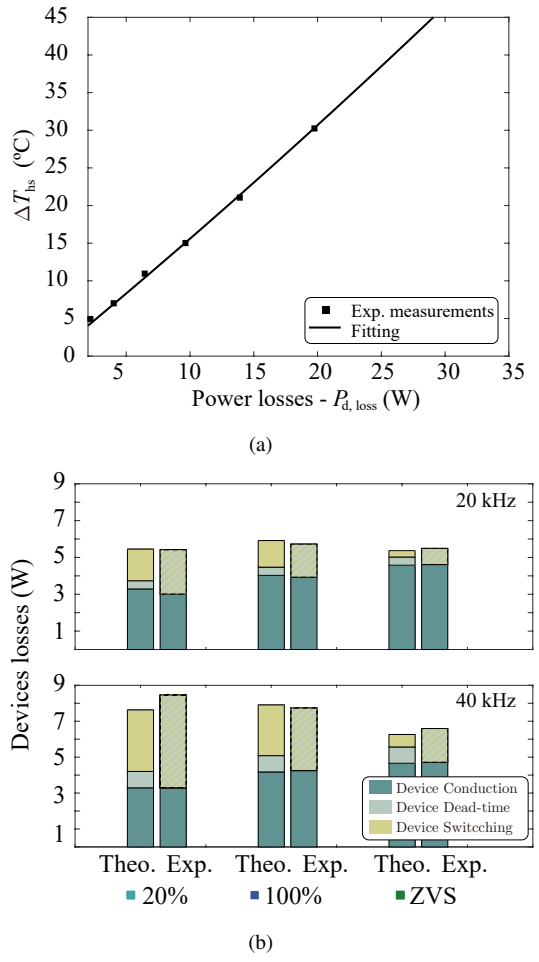

Fig. 8: Analysis of devices power losses, comparing different current ripples: (a) relation between heatsink temperature increment and power losses and (b) distribution of devices power losses (I_o=10 A / V_i=350 V).

B. Measurement results

In Fig. 8(b) a good match between theoretical and experimental measurements is observed with a difference mainly related to the conduction losses. Hence, it is demonstrated how even for such low switching frequency (see Fig. 8(b)- 20 kHz) the influence of the switching losses is reduced as the current ripple increases. However, the increase of the conduction losses leads to achieve similar power losses. Furthermore, when switching losses are more relevant (see Fig. 8(b)- 40 kHz) the increase of the current ripple results on even lower power losses [see Fig. 8(b)].

V. Conclusions

Although GaN switches present low power losses the complexity to extract the heat from such small devices limits the use of these devices in power applications. This paper analyzes the influence of different operation conditions in order to reduce GaN devices power losses and increase thermal cooling capability. On the one hand, the increase of the current ripple reduces power losses for high switching frequencies (>40 kHz). The great difference between turn-on and turn-off energies , along with low conduction resistance of GaN devices leads to a reduction of devices losses. Moreover, the increase of the current ripple, ensuring ZVS avoids turn-on losses and allows high switching frequency operation. On the other hand, the use of parallel connected devices results in higher thermal limit, being possible to achieve higher output currents. Then, parallel-connected devices are not only used to reduce the power losses at low switching frequencies but also to increase the thermal cooling capability. Hence, the use of parallel-connected devices will be essential for medium/high power converters.

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