# ANALYSIS OF PATTERN-DEPENDENT AND TIMING-DEPENDENT FAILURES IN AN EXPERIMENTAL TEST CHIP

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**ABSTRACT**

*This paper presents the results for very detailed studies of pattern and timing-dependent failures from the 309 dies in the retest of an experimental test chip. 22 out of the 50 CUTs with pattern-dependent failures had test escapes if the test sets were reordered. Some timing-dependent failures became timing-independent combinational (TIC) defects at very low voltage. Multiple-detect single stuck fault test sets have high transition fault coverage. Most dies with TIC or non-TIC defects were close to gross failures or next to the wafer periphery.*

## 1. INTRODUCTION

A test chip has been designed and manufactured to be used in an experiment that was designed to evaluate the effectiveness of different test techniques. This paper is part of a series that reported the experimental results from this experiment [1-5]. The design of the experiment and architecture of the test chip were described in ITC'95 [1-2]. The experimental setup of the retest was described in VTS'98 [5]. In ITC'95 and ITC'96, the experimental results from the wafer probe were presented. Based on the results reported in ITC'95 and ITC'96, 309 out of 5491 dies that passed the Stage 1 tests in the wafer probe were selected for further investigation. The 309 dies were packaged by using 120-pin ceramic pin grid array packages and tested with an Advantest T6671E VLSI Test System. The Advantest T6671E VLSI Test System has a clock rate of 125MHz. The objectives of the retest were presented in VTS'98 [5] and listed below:

1. *Collecting accurate IDDQ measurements.*
2. *Characterizing Very-Low-Voltage (VLV) only failures.*
3. *Investigating pattern-dependent failures.*
4. *Characterizing timing-dependent failures.*
5. *Investigating repeatability of the results from the wafer probe.*

The experimental results of IDDQ and Very-Low-Voltage (VLV) testing from the retest were reported in VTS'98 [5]. This paper presents the analysis of the following items based on the experimental results from the retest:

1. *Repeatability.*
2. *Pattern-dependent failures.*
3. *Timing-dependent failures.*
4. *Multiple-detect single stuck fault (SSF) test sets.*
5. *Defect distribution.*

The test chip uses the LSI Logic LFT150K FasTest array series. The nominal supply voltage is 5V and the effective channel length is 0.7 µm. The test chip contains five CUTs. Two CUTs (MUL and SQR) are datapath logic. The other three (STD, ELM, and ROB) are control logic, which perform the same function but are implemented in different ways [1-2]. The test chip is a 25k gate CMOS gate array with 64 input pins and 32 output pins. The five CUTs occupy approximately 50% of the chip area. the rest of the chip is used by test support circuitry. There are three data sources and three clocking modes in this experiment. They were used in both the wafer probe and the retest.

During the retest, each CUT was tested at four different speeds at nominal supply voltage. Besides the three test speeds used in the wafer probe, we added a test speed that is at least three times slower than the rated test speed. All CUTs were tested at three different supply voltages: 5V, 2.5V, and 1.7V.

In order to compare two-pattern tests and at-speed tests, two different timing setups were used. For one, the cycle time for the first vector in each vector pair was at least 3 times slower than the rated cycle time. For another, the cycle time for the first vector in each vector pair was the same as the rated cycle time.

We added several new test sets in the retest. The new test sets include multiple-detect SSF test sets provided by University of Iowa [6], delay fault test sets from University of Southern California [7], and IDDQ test sets generated by using vendors' ATPG tools. To investigate pattern-dependent defects, we added test sets that were modified from the original SSF test sets.

Table 1 summarizes the dies used in the retest. The detailed discussion of the die selection criteria was presented in VTS'98 [5]. A die is classified as having CUT sampling failures if one or more of its CUTs failed at least one Boolean test at nominal voltage. A die is classified as having *IDDQ failures* if its maximum IDDQ

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measurement exceeded a current limit. A die is classified as having *VLV-only failures* if it passed all the sampling (Boolean) tests at the nominal supply voltage but failed some sampling tests at very low voltage. The behavior of a *combinational defect* only depends on the input pattern applied and does not depend on previous patterns. The behavior of a *timing-independent defect* does not depend on the clock speed (less than or equal to the rated speed) at the nominal operating voltage. A *timing-independent combinational (TIC) defect* has both properties of a combinational defect and a timing-independent defect [4]. A defect that is either timing-dependent or pattern-dependent (non-combinational) is classified as a *non-TIC defect*. If the failure counts of a TIC defect matched those of a SSF, it is classified as a *SSF TIC defect*. Otherwise, it is a *non-SSF TIC defect*.

Table 1 Summary of the packaged dies for the retest

| Defect class | Total number of dies based on [3] and [4] | Number of packaged dies |
|---|---|---|
| CUT sampling failures | 125 | 122 |
| VLV-only failures | 23 | 20 |
| IDDQ failures | NA | 1 |
| good dies | NA | 166 |
| Total | NA | 309 |

This paper is organized as follows. Section 2 describes the experimental setup for the retest. Section 3 compares the results from the retest and the wafer probe. Section 4 analyzes the dies that had pattern-dependent failures. Section 5 discusses the dies that had timing-dependent failures. Section 6 shows the results of multiple-detect SSF test sets. Section 7 shows the defect distribution of all defect classes shown in this experiment. Section 8 concludes the paper.

## 2. EXPERIMENTAL SETUP

The test plan for the retest is similar to the one for the wafer probe. A two-stage testing strategy was used in the retest. Stage 1 tests consist of gross parametric tests and test support circuitry tests. Stage 2 tests consist of actual CUT tests, which include verification, exhaustive, pseudo-random, weighted-random, stuck-at, transition, path delay, gate delay, signature analysis, IDDQ, and VLV tests. We only describe the additional test sets and test conditions used in the retest. The test plan of the wafer probe can be found in [2-4]. For Stage 1 tests, we used the tests applied in the wafer probe. We added new test sets and test conditions in the Stage 2 tests.

### 2.1 Supply Voltage

In the wafer probe, all Boolean test sets were run at 5V and 1.7V. We added another supply voltage, 2.5V, in the retest. Chang and McCluskey have studied the supply voltage for VLV testing [8-9]. 1.7V is within the proposed supply voltage, $2V_t$ to $2.5V_t$. Only one extra supply voltage was added due to the consideration of the tester time for each packaged unit.

### 2.2 Test Timing

The test sets were applied at three different clock speeds in the wafer probe. A very slow clock speed was added when testing at nominal supply voltage in the retest to differentiate timing-dependent defects from timing-independent defects. The very slow clock speed is 3 times slower than the rated speed. Table 2 lists the clock speeds used at nominal supply voltage.

Table 2 Clock speeds used at 5V for the retest

| Test timing | Clock speed |
|---|---|
| **r**-rated timing | rated speed of each CUT |
| **s**-slow timing | slower than rated speed (2/3 rated) |
| **ss**-very slow timing | much slower than rated speed (less than 1/3 rated) |
| **f**-fast timing | faster than rated speed (15% for MUL and SQR, 5% for others) |

At 2.5V and 1.7V, we used two clock speeds for all Boolean tests. A very slow clock speed was used at each supply voltage to investigate if VLV-only failure is timing dependent. Tables 3 and 4 list the clock speeds used at 2.5V and 1.7V.

Table 3 Clock speeds used at 2.5V for the retest

| Test timing | Clock speed |
|---|---|
| **r**-rated timing | 1/3 rated speed at 5V |
| **ss**-very slow timing | 1/6 rated speed at 5V |

Table 4 Clock speeds used at 1.7V for the retest

| Test timing | Clock speed |
|---|---|
| **r**-rated timing | 1/5.6 rated speed at 5V |
| **ss**-very slow timing | 1/8 rated speed at 5V |

### 2.3 Data Sources

There are three data sources in this experiment. The data can be directly loaded from ATE to the input registers that are located at the inputs of all CUTs. In *simulated scan*, before each vector is applied, a shifted version of the vector is loaded to the input register. There are several LFSRs on the chip that can generate input vectors internally. LFSRs were used to generate the exhaustive tests or super-exhaustive tests in the retest.

### 2.4 Clocking Modes

As shown in Fig. 1, the test chip was designed to have different input and output clocks. The input clock is used to apply data to the CUTs and the output clock is used to sample the outputs of the CUT. All registers are positive edge triggered flip-flops.

In the DIrect clocking mode (DI), both input clock and output clocks are the same external clock which is provided by the tester. In the PUlse-width mode (PU), the input clock comes from the tester but the output clock is

the inverted version of the input clock. These two clocking modes are shown in Figure 2a and 2b respectively.

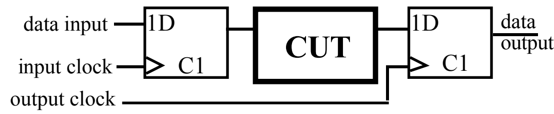


Figure 1 Input and output clock

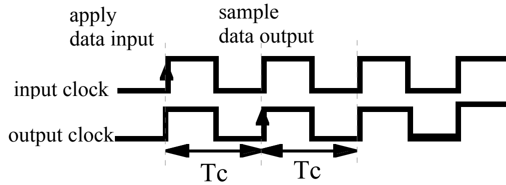


Figure 2a Direct clocking mode (DI)

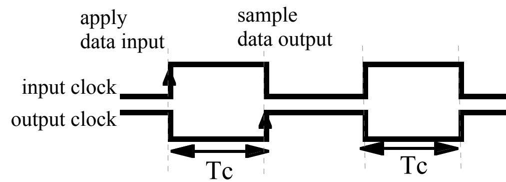


Figure 2b Pulse-width clocking mode (PU)

A two-pattern test requires a vector pair <V1,V2>. The *initialization vector* <V1> is applied and once the circuit has settled, the *test vector* <V2> is applied. In order to evaluate the effect of the wait time between <V1> and <V2>, two different timing setups were used. They are:

**a.** Direct clocking mode with the wait time between <V1> and <V2> to be three cycle time, $3T_c$.

**b.** Direct clocking mode with the wait time between <V1> and <V2> to be one cycle time, $T_c$.

The timing waveforms are shown in Figure 3a and 3b respectively.

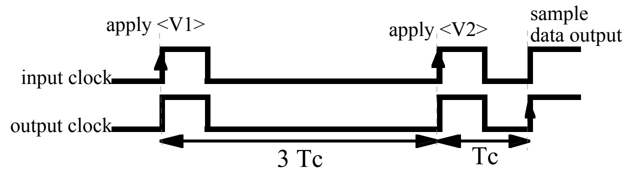


Figure 3a DI mode, wait time = $3T_c$

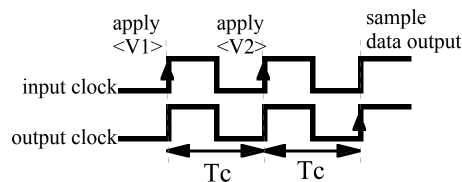


Figure 3b DI mode, wait time = $T_c$

## 2.5 IDDQ Measurements

Special care was taken during IDDQ measurements. There are four input pins with pull-up resistors. These four pins are the control pins for the embedded CrossCheck array [10]. When measuring IDDQ currents, all four of these pins were tied to the supply voltage source of the tester to eliminate the static current due to the voltage difference between $V_{dd}$ and $V_{IH}$. The resolution of the current measurement is 2 nA. The wait time before each IDDQ measurement is 1ms.

Researchers have reported data on IDDQ measurements at different supply voltages [11]. In the retest, we did IDDQ measurements at 5.25V, 2.5V, and 1.7V. $V_{IH}$ was set to the supply voltage and $V_{IL}$ was set to 0V for all IDDQ measurements. No output pins were loaded during the IDDQ measurements.

## 2.6 Test Ordering

The exhaustive tests were applied at nominal supply voltage for rated timing after the Stage 1 tests and before all CUT tests. All CUT tests were applied at 5V first. CUTs were then tested at 2.5V and 1.7V. Before applying IDDQ test sets, the exhaustive test sets were applied again at nominal supply voltage for rated timing. The IDDQ test sets were applied afterward. After measuring IDDQ values for all IDDQ test sets, the exhaustive test sets were applied at nominal supply voltage for rated timing again. The exhaustive test sets were applied in this way to verify the repeatability of the behavior of each die.

## 2.7 Test Sets

Based on the results of the wafer probe, we added several test sets for the retest. Some new test sets were contributed by University of Iowa and University of Southern California. We also used some updated commercial tools, such as Mentor Graphics and Sunrise's ATPG tools, to generate new test sets. To study the causes of pattern-dependent failures, we modified some of the original test sets. We describe each new test set in turn.

### Single Stuck-at Fault Tests (SSF Tests)

We have multiple-detect single stuck-at test sets with more resolution for the retest. In the wafer probe, there were only one 5-detect and one 15-detect SSF test sets. In the retest, we added 2-detect, 3-detect, 4-detect, 5-detect, 7-detect, 10-detect, 12-detect, and 15-detect SSF test sets. Unlike the two multiple-detect SSF test sets, which were generated by ad-hoc techniques, the new multiple-detect SSF test sets were generated by university ATPG tools that were built to generate multiple-detect SSF test sets. We also had more 100% SSF test sets that were generated by latest version commercial tools. These test sets include compact SSF test sets and SSF test sets based on pin fault model.

### Delay Test Sets

These include path delay fault test sets generated by university tools and transition fault test sets generated by a latest version commercial tool. These test sets are only available for three control logic CUTs, STD, ELM, and ROB.

**IDDQ Test Sets**

Two types of IDDQ test sets were added. One was generated by ATPG tools that use the pseudo stuck-at model. The vectors in the other type were selected from a set of functional vectors. The static current of each vector was measured and recorded.

**Test Sets Modified from Original Test Sets**

In the wafer probe, there were significant amount of CUT sampling failures that were pattern-dependent. A CUT with *pattern-dependent defects* behaved differently when the pattern preceding each vector was changed. In the wafer probe, simulated scan data source mode was used for design verification, SSF, switch-level, weighted-random, and stuck-open test sets. We modified these test sets in four different ways:

**a.** Insert an all-one vector in front of each vector.
**b.** Insert an all-zero vector in front of each vector.
**c.** Insert a bitwise complemented vector in front of each vector.
**d.** Reverse the vector sequence in the original test set.

These modified vectors were only applied through parallel load data source.

**Exhaustive Test Sets**

We added exhaustive test sets for the two low voltage tests in the retest. The results of these exhaustive test sets can be used as references for the results from the two low voltage tests.

## 3. REPEATABILITY

For the 122 dies that failed some Boolean tests at nominal supply voltage in the wafer probe, there are 113 dies that failed some Boolean tests at nominal supply voltage for the same CUT(s). One die that had non-TIC defects at nominal supply voltage in the wafer probe passed all the Boolean tests at nominal supply voltage. This die, however, failed some Boolean tests at 2.5V and 1.7V. The fail counts at 1.7V from the retest matched the fail counts measured from the wafer probe. As happened in the wafer probe, there are three dies that had two CUTs failing some Boolean tests at nominal supply voltage. Three out of 122 dies failed the Stage 1 tests in the retest. The other five passed all the tests in the retest. For the 20 dies that had VLV-only failures in the wafer probe, 19 dies repeated the results in the retest. The other one passed all the tests in the retest. The cause of the mismatch is identified as the wafer map problem. We do not include these dies in the discussion for the rest of this paper. There were three CUTs that passed all the tests in the wafer probe and failed some CUT Boolean tests at nominal supply voltage in the retest. The results of these CUT sampling failures will be selectively used in this paper.

We also compared the fail counts of each CUT sampling failure between the results from the wafer probe and those from the retest. We used the fail counts measured when the data source is parallel load and the clock is in pulse-width generated clocking mode. Moreover, the fail counts of two test speeds, rated and very slow, were used for the comparison. There were 31 CUT sampling failures having exactly the same fail counts as those measured from the wafer probe. Among these 31 CUT sampling failures, 14 were classified as having SSF TIC defects, 14 were classified as having non-SSF TIC defects, and the other three were classified as having non-TIC defects. 51 CUT sampling failures had similar fail counts as those measured from the wafer probe. For these 51 CUT sampling failures, most of the test sets that used in both the wafer probe and the retest had exactly the same fail counts from both the wafer probe and the retest. The fail counts of the other test sets were close, although not exactly the same. 21 of these 51 CUT sampling failures were classified as having SSF TIC defects, nine were classified as having non-SSF TIC defects, and the other 21 were classified as having non-TIC defects. There were 35 CUT sampling failures whose fail counts were different between the ones measured from the wafer probe and from the retest for at least half of the applied test sets. Among these 35 CUT sampling failures, three were classified as having SSF TIC defects, another three were classified as having non-SSF TIC defects, and the other 29 were classified as having non-TIC defects.

Most of the CUT sampling failures with TIC defects had either identical or close fail counts between the wafer probe and the retest. On the other hand, most CUT sampling failures with non-TIC defects had different fail counts between the wafer probe and the retest. Table 5 summarizes the repeatability results.

Table 5 Repeatability of the retest results

| Comparison | Number | Defect classes |
|---|---|---|
| Identical | 31 | 14 SSF TIC, 14 non-SSF TIC, and 3 non-TIC |
| Close | 51 | 21 SSF TIC, 9 non-SSF TIC, and 21 non-TIC |
| different | 35* | 3 SSF TIC, 3 non-SSF TIC, and 29 non-TIC |

* this includes the one that had non-TIC defects in the wafer probe but became having VLV-only failures in the retest.

## 4. PATTERN-DEPENDENT FAILURES

Based on the results from the wafer probe, we found that some CUT sampling failures had different fail counts for different data sources even when the test set was run at the same test speed. As shown in Sec. 2, we modified each SSF test set in four different ways to further characterize pattern-dependent failures.

In the retest, there were 50 CUTs that had pattern-dependent failures. Among these 50 CUTs, there were four that were classified as having TIC defects in the wafer probe and one new CUT sampling failures. 22 out of the 50 CUTs had test escapes for at least one modified SSF test set. The Venn diagram is shown in Fig. 4.

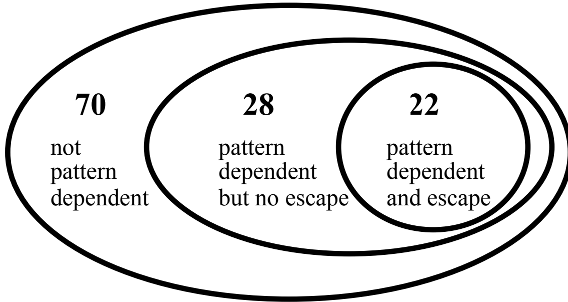


Figure 4 Venn diagram of pattern-dependent failures

None of these 22 CUT sampling failures were classified as having SSF TIC defects in the wafer probe. However, one of these 22 CUT sampling failures was classified as having non-SSF TIC defect in the wafer probe. Here are some observations based on these results:

**a.** 44% of the pattern-dependent defects become test escapes when the test set is reordered or modified.

**b.** The test results of SSF test sets for SSF TIC defects depend neither on the vector preceding each vector in the original SSF test set nor the vector ordering.

**c.** Some CUTs with TIC defects may become pattern-dependent or even have test escapes when the original test set is reordered or modified.

## 5. TIMING-DEPENDENT FAILURES

We added a very slow timing in the retest to investigate if test escapes could occur for the CUTs with timing failures when a test was run at a very slow speed. Table 6 shows the test escapes of SSF test sets and Table 7 shows the test escapes of two-pattern tests for the 120 defective CUTs. These 120 CUTs include the 117 CUTs that failed the same CUT(s) for some Boolean tests at nominal supply voltage for both the wafer probe and retest and the other three CUTs that passed all the tests in the wafer probe but failed some Boolean tests at nominal supply voltage in the retest. Two test timings (**r**: rated; **ss**: very slow) and two clocking modes (PU and DI) are listed for comparison. The distribution of test escapes at rated timing between PU and DI clocking modes is also shown.

Table 6 Test escapes of SSF test sets

| | Clocking mode | PU | | DI | | Test escapes distribution (rated timing) | | |
|---|---|---|---|---|---|---|---|---|
| Test set | Test timing | **r** | **s s** | **r** | **s s** | PU-only | PU and DI | DI-only |
| 2.1 | SSF Tool 1 (100%, gate faults) | 8 | 13 | 12 | 15 | 0 | 8 | 4 |
| 2.2 | SSF Tool 2 (100%, gate faults) | 5 | 10 | 9 | 11 | 0 | 5 | 4 |
| 2.3 | SSF Tool 2 (100%, pin faults) | 6 | 10 | 11 | 11 | 0 | 6 | 5 |
| 2.4 | SSF Tool 3 (100%, pin faults) | 9 | 12 | 14 | 15 | 0 | 9 | 5 |
| 2.5 | SSF Tool 3 (100%, compressed) | 4 | 7 | 8 | 8 | 0 | 4 | 4 |
| 2.6 | SSF Tool 4 (100%, gate faults) | 7 | 11 | 9 | 12 | 0 | 7 | 2 |
| 2.7 | SSF Tool 4 (99.0%) | 8 | 12 | 10 | 14 | 0 | 8 | 2 |
| 2.8 | SSF Tool 4 (98.0%) | 10 | 14 | 12 | 15 | 0 | 10 | 2 |
| 2.9 | SSF Tool 4 (95.0%) | 13 | 16 | 17 | 17 | 0 | 13 | 4 |
| 2.10 | SSF Tool 4 (90.0%) | 18 | 21 | 20 | 22 | 1 | 17 | 3 |
| 2.11 | SSF Tool 4 (80.0%) | 24 | 27 | 25 | 27 | 0 | 24 | 1 |
| 2.12 | SSF Tool 4 -- Min 5 Det/Fault | 3 | 8 | 7 | 10 | 0 | 3 | 4 |
| 2.13 | SSF Tool 4 -- Min 15 Det/Fault | 3 | 8 | 6 | 10 | 0 | 3 | 3 |
| 10.1 | SSF Tool 3 (100%, new version) | 12 | 15 | 16 | 16 | 0 | 12 | 4 |
| 11.1 | SSF Tool 11 (100%, gate faults) | 6 | 10 | 8 | 11 | 0 | 6 | 2 |
| 11.2 | SSF Tool 11 -- Min 2 Det/Fault | 5 | 10 | 8 | 12 | 0 | 5 | 3 |
| 11.3 | SSF Tool 11 -- Min 3 Det/Fault | 3 | 8 | 8 | 9 | 0 | 3 | 5 |
| 11.4 | SSF Tool 11 -- Min 4 Det/Fault | 3 | 8 | 8 | 9 | 0 | 3 | 5 |
| 11.5 | SSF Tool 11 -- Min 5 Det/Fault | 3 | 8 | 7 | 9 | 0 | 3 | 4 |
| 11.6 | SSF Tool 11 -- Min 7 Det/Fault | 4 | 8 | 7 | 10 | 1 | 3 | 4 |
| 11.7 | SSF Tool 11 -- Min 10 Det/Fault | 3 | 9 | 7 | 10 | 0 | 3 | 4 |
| 11.8 | SSF Tool 11 -- Min 12 Det/Fault | 3 | 8 | 7 | 10 | 0 | 3 | 4 |
| 11.9 | SSF Tool 11 -- Min 15 Det/Fault | 3 | 8 | 7 | 10 | 0 | 3 | 4 |
| 12.1 | SSF Tool 12 (100%, compressed) | 7 | 11 | 11 | 12 | 0 | 7 | 4 |
| 12.2 | SSF Tool 12 (100%, pin faults) | 10 | 13 | 12 | 14 | 0 | 10 | 2 |
| 3.1 | Switch-level ATPG | 9 | 12 | 10 | 12 | 0 | 9 | 1 |
| 4.1 | Pseudo-Random/Exhaustive | 2 | 7 | 5 | 8 | 0 | 2 | 3 |

Based on Tables 6 and 7, we made the following observations:

**a.** Mostly, test escapes increased as test speed decreased.
**b.** High fault coverage SSF test sets performed better than low coverage ones. (test sets 2.6-2.10)
**c.** Although SSF test sets do not target non-TIC defects, some SSF test sets detected most non-TIC defects when applied at rated timing.
**d.** From test sets 11.1 to 11.5, the performance of multiple-detect SSF test sets improved as the number of detects increase.
**e.** There were more defective CUTs detected by the PU clocking mode than by the DI clocking mode.

Some defective CUTs were detected only by the DI clocking mode. Table 8 lists the test escapes of the two-pattern test sets. As described in section 2.4, DI clocking mode with two wait time ($3T_c$ and $T_c$) are listed for comparison. The distribution of test escapes between this two wait time is also shown. Table 8 shows that three-cycle wait time performed almost the same as one-cycle wait time. The experimental results showed that the length of wait time in two-pattern tests had little effect on the test result.

There were seven CUTs that failed some tests for the rated timing at nominal supply voltage but passed *all* the tests at very slow timing at the same supply voltage in the retest. There was one CUT that failed some tests for the rated timing at nominal supply voltage but passed *some* tests at very slow timing at the same supply voltage in the retest. Figure 5 shows the characterization results of these eight CUTs. The detailed information of these eight CUTs can be found in the appendix (Table A-3).

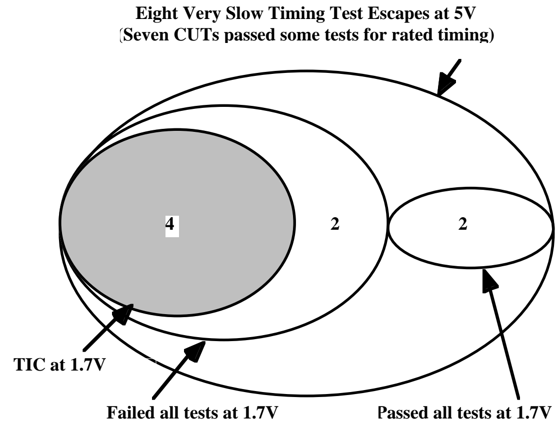


Figure 5 VLV test results for CUTs with very slow timing escapes

Table 7 Test escapes of two-pattern tests

| Test set | Clocking mode / Test timing | PU r | PU s s | DI r | DI s s | PU-only | PU and DI | DI-only |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Test escapes distribution (rated timing) | | |
| 6.1 | Stuck-Open ATPG (equiv. gate) | 4 | 9 | 9 | 11 | 0 | 4 | 5 |
| 7.1 | Transition Fault, ATPG Tool 5 | 6 | 11 | 11 | 12 | 0 | 6 | 5 |
| 8.1* | Gate Delay Fault -- X-> 0 | 13 | 15 | 14 | 15 | 1 | 12 | 2 |
| 8.2* | Gate Delay Fault -- X -> ran | 9 | 11 | 12 | 11 | 0 | 9 | 3 |
| 9.3** | Path Delay -- Robust -- X -> 0 | 3 | 6 | 8 | 7 | 0 | 3 | 5 |
| 9.4** | Path Delay -- Robust -- X -> ran | 3 | 7 | 8 | 8 | 0 | 3 | 5 |
| 9.5** | Path Delay -- Robust Test | 3 | 6 | 7 | 7 | 0 | 3 | 4 |
| 9.6** | Path Delay -- Non-Robust A | 8 | 10 | 12 | 12 | 0 | 8 | 4 |
| 9.7** | Path Delay -- Non-Robust B | 3 | 7 | 6 | 8 | 0 | 3 | 3 |
| 13.1** | At-Speed Test A | 3 | 7 | 6 | 9 | 0 | 3 | 3 |
| 13.2** | At-Speed Test B | 4 | 7 | 6 | 9 | 0 | 4 | 2 |
| 13.3** | At-Speed Test C | 4 | 7 | 7 | 8 | 0 | 4 | 3 |

* 82 defective CUTs (SQR, ELM, STD, ROB)
** 63 defective CUTs (ELM, STD, ROB)

Table 8 Test escapes of two-pattern test sets with different wait time

| Test set | Clocking mode / Wait time | DI 3Tc | DI Tc | 3Tc-only | Both | Tc-only |
|---|---|---|---|---|---|---|
| | | | | Test escapes distribution | | |
| 7.1 | Transition Fault, ATPG Tool 5 | 11 | 11 | 0 | 11 | 0 |
| 8.1* | Gate Delay Fault -- X-> 0 | 14 | 13 | 1 | 13 | 0 |
| 8.2* | Gate Delay Fault -- X -> ran | 12 | 12 | 0 | 12 | 0 |
| 9.3 | Path Delay – Robust – X-> 0 | 8 | 7 | 1 | 7 | 0 |
| 9.4** | Path Delay – Robust -- X -> ran | 8 | 7 | 1 | 7 | 0 |
| 9.5** | Path Delay – Robust Test | 7 | 5 | 2 | 5 | 0 |

* 82 defective CUTs (SQR, ELM, STD, ROB)
** 63 defective CUTs (ELM, STD, ROB)

Based on the results in Fig. 5, we made the following observations:

**a.** Six out of these eight CUTs failed all the tests at 1.7V. This indicates that the effects of some timing-dependent defects are more visible at very low voltage.

**b.** Four out of these eight CUTs exhibited TIC defects at 1.7V. i.e., the defects that caused timing failures at nominal supply voltage can become TIC defects when tested at very low voltage.

**c.** Two out of these eight CUTs had test escapes at 1.7V. Some defects that caused timing failures at the nominal supply voltage had no faulty effects at very low voltage.

## 6. MULTIPLE-DETECT SSF TEST SETS

We collected multiple-detect SSF test sets with more resolution for the retest. They include 1-detect, 2-detect, 3-detect, 4-detect, 5-detect, 7-detect, 10-detect, 12-detect, and 15-detect SSF test sets.

Table 9 lists the total test length of each multiple-detect SSF test set. We fault graded these multiple-detect SSF test sets using transition fault model. The average fault coverage for the five CUTs are calculated and shown in the same table. Test escapes at rated timing for both PU and DI clocking mode are also listed.

There are 120 CUTs used in this section. They include the 117 CUTs that failed the same CUT(s) for some Boolean tests at nominal supply voltage for both the wafer probe and retest and the other three CUTs that passed all the tests in the wafer probe but failed some Boolean tests at nominal supply voltage in the retest.

Based on this table, we made the following observations:

**a.** Although multiple-detect SSF test sets do not target transition faults, they have very high transition fault coverage.

**b.** Mostly, test escapes improve or remain the same when the number of detects for each fault increases.

**c.** The test escapes for pulse-width generated clocking mode is in general better than those for direct-clocking mode**.**

## 7. DEFECT DISTRIBUTION

Figure 6 shows the wafer map notation used in this paper. "X" represents a gross failure. "." represents a die that passed both stage 1 and stage 2 tests. "F" represents a die that failed at least one CUT test at nominal voltage. "T" represents a die with TIC defects. "V" represents a die that passed all the tests at the nominal supply voltage but failed some tests at 1.7V. "D" represents a die with non-TIC defects. "I" represents a die whose maximum IDDQ measurement is over the current limit.

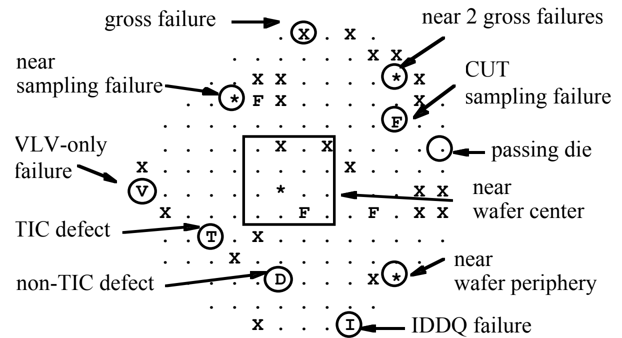


Figure 6 Classification for die location

We classified die locations into the following 4 categories:

**a.** near gross failures: one or more of the eight surrounding dies have gross failures.

Table 9 Test length, coverage, and test escapes of each multiple-detect SSF test sets

| Test set | | Test length* | Transition fault coverage* | Test escapes (rated timing) | |
|---|---|---|---|---|---|
| | | | | PU | DI |
| 7.1 | Transition Fault, ATPG Tool 5 | 1,444 | 91.64% | 6 | 11 |
| 2.6 | SSF Tool 4 (100%, gate faults) | 547 | 89.11% | 4 | 8 |
| 2.12 | SSF Tool 4 -- Min 5 Det/Fault | 2,398 | 98.00% | 3 | 7 |
| 2.13 | SSF Tool 4 -- Min 15 Det/Fault | 7,181 | 98.86% | 3 | 6 |
| 11.1 | SSF Tool 11 (100%, gate faults) | 313 | 85.78% | 6 | 8 |
| 11.2 | SSF Tool 11 -- Min 2 Det/Fault | 671 | 94.00% | 5 | 8 |
| 11.3 | SSF Tool 11 -- Min 3 Det/Fault | 981 | 95.96% | 3 | 8 |
| 11.4 | SSF Tool 11 -- Min 4 Det/Fault | 1,292 | 97.31% | 3 | 8 |
| 11.5 | SSF Tool 11 -- Min 5 Det/Fault | 1,605 | 97.56% | 3 | 7 |
| 11.6 | SSF Tool 11 -- Min 7 Det/Fault | 2,203 | 98.16% | 4 | 7 |
| 11.7 | SSF Tool 11 -- Min 10 Det/Fault | 3,022 | 98.02% | 3 | 7 |
| 11.8 | SSF Tool 11 -- Min 12 Det/Fault | 3,578 | 98.02% | 3 | 7 |
| 11.9 | SSF Tool 11 -- Min 15 Det/Fault | 4,396 | 98.20% | 3 | 7 |

* Please see appendix (Tables A-1 and A-2) for the detailed numbers for each CUT

**b.** near wafer edges: a die that is located next to the wafer periphery.

**c.** near wafer center: a die that is among the center 16 dies on a wafer.

**d.** near sampling failures: a die that is next to one or more dies that had CUT sampling failures at normal voltage.

If a die location belongs to any of the 4 categories, it is a *classified die location*. Otherwise, it is a *non-classified die location*. We focus on the die locations of the following defects: TIC defects, non-TIC defects, SSF TIC defects, non-SSF TIC defects, VLV-only failures and IDDQ failures.

Table 10 lists the statistics of the distribution of TIC, non-TIC, SSF TIC, non-SSF TIC, and VLV-only failures. Table 11 shows the statistics of the die location of IDDQ failures with 3 different current limits. The current limits used include 3μA, 20μA, and 100μA.

Based on the results in Tables 10 and 11, we make the following observations.

**a.** 88.8% of the dies that had CUT sampling failures at nominal operating voltage are either close to dies with gross failures or next to the wafer periphery.

**b.** 91.1% of the dies that had non-TIC defects are either close to dies with gross failures or next to the wafer periphery.

**c.** All the dies with VLV-only failures are either close to dies with gross failures or next to the wafer periphery, i.e., all VLV-only failures have classified die locations.

**d.** The percentage of dies with classified die locations is slightly low for non-SSF TIC defects compared to the other defect classes.

**e.** 89.6% of dies whose maximum IDDQ measurements exceeded 20 μA are either close to dies with gross failures or next to the wafer periphery.

**f.** The percentage of the dies that are close to either gross failures or the wafer periphery for IDDQ failures remains almost the same for three different current limits.

In general, a high percentage of the defects that behave as TIC, non-TIC, VLV-only failures, or IDDQ failures are located either near to dies with gross failures or next to the wafer periphery.

## 8. CONCLUSIONS

We have presented the test results for pattern-dependent failures, timing-dependent failures, multiple-detect SSF test sets, and defect distribution based on the retest results in a test chip experiment.

Some pattern-dependent failures can become test escapes if the test sets were reordered or modified. Some timing-dependent failures can become TIC-defects at very low voltage. However, we also found that some timing-dependent failures may become test escapes for VLV tests.

We compared two clocking modes: direct clocking mode and pulse-width clocking mode. More defective CUTs were detected in the pulse-width clocking mode than in the at-speed clocking mode. However, there were some unique detects in the at-speed clocking mode. For two-pattern test, we compared two different wait time: three cycle times and one cycle time. The results showed little difference.

Table 10 Statistics of defect distribution for each defect class

| Defect type | Defect location | | | | | |
|---|---|---|---|---|---|---|
| | Number of dies | Near gross failures | Near wafer periphery | Near either gross failures or wafer periphery | Near wafer center | Others |
| TIC | 69 | 58 (84.1%) | 15 (21.7%) | 60 (87.0%) | 9 (13.0%) | 7 (10.1%) |
| Non-TIC | 56 | 49 (87.5%) | 11 (19.6%) | 51 (91.1%) | 10 (17.9%) | 4 (7.1%) |
| SSF TIC | 39 | 35 (89.7%) | 11 (28.2%) | 36 (92.3%) | 5 (12.8%) | 2 (5.1%) |
| non-SSF TIC | 30 | 23 (76.7%) | 4 (13.3%) | 24 (80.0%) | 4 (13.3%) | 5 (16.7%) |
| VLV-only | 23 | 18 (78.3%) | 14 (60.9%) | 23 (100%) | 2*(8.7%) | 0 (0%) |
| TIC+non-TIC | 125 | 107 (85.6%) | 26 (20.8%) | 111 (88.8%) | 19 (15.2%) | 11 (8.8%) |

* near gross failures too

Table 11 Defect location for dies whose IDDQ measurements exceeded the limit

| | Defect location | | | | | |
|---|---|---|---|---|---|---|
| IDDQ measurement limit | Number of dies | Near gross failures | Near wafer periphery | Near either gross failures or wafer periphery | Near wafer center | Others |
| 3 μA | 111 | 95 (85.6%) | 28 (25.2%) | 100 (90.1%) | 16 (14.4%) | 9 (8.1%) |
| 20 μA | 106 | 90 (84.9%) | 28 (26.4%) | 95 (89.6%) | 14 (13.2%) | 9 (8.5%) |
| 100 μA | 92 | 79 (85.9%) | 23 (25%) | 82 (89.1%) | 12 (13.0%) | 9 (9.8%) |

We applied multiple-detect SSF test sets generated by an ATPG. The new test sets have more resolution than the ones used in the wafer probe. Mostly, the test escapes always improve or at least remain the same when the number of detects for each fault increases. We found that multiple-detect SSF test sets have very high transition fault coverage

We also presented the defect distributions on wafers for different defect classes. Most dies that had TIC or non-TIC defects were close to gross failures or next to the wafer periphery. All dies that had VLV-only failures in this experiment were close to gross failures or next to the wafer periphery.

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## APPENDIX

Table A-1 lists the test length of the multiple-detect SSF test sets for each CUT. SSF Tool 4 is the same tool as shown in [3-4]. SSF Tool 11 was an ATPG tool that aims at generating multiple-detect SSF test sets. As shown in the table, the test length of any multiple-detect SSF test sets generated by using SSF Tool 11 is much shorter than the one generated by SSF Tool 4. Table A-2 lists the transition fault coverage of the multiple-detect SSF test sets for each CUT. Table A-3 lists the detailed behavior of each CUT with very-slow-timing escape at nominal voltage.

Table A-1 Test length of multiple-detect SSF test sets for each CUT

| Test set | | Test length | | | | |
|---|---|---|---|---|---|---|
| | | ROB | STD | ELM | MUL | SQR |
| 7.1 | Transition Fault, ATPG Tool 5 | 796 | 222 | 256 | 84 | 86 |
| 2.6 | SSF Tool 4 (100%, gate faults) | 275 | 71 | 93 | 68 | 39 |
| 2.12 | SSF Tool 4 -- Min 5 Det/Fault | 1,235 | 339 | 397 | 258 | 168 |
| 2.13 | SSF Tool 4 -- Min 15 Det/Fault | 3,745 | 1,046 | 1,163 | 754 | 473 |
| 11.1 | SSF Tool 11 (100%, gate faults) | 167 | 38 | 49 | 33 | 26 |
| 11.2 | SSF Tool 11 -- Min 2 Det/Fault | 346 | 83 | 102 | 79 | 61 |
| 11.3 | SSF Tool 11 -- Min 3 Det/Fault | 519 | 124 | 150 | 105 | 83 |
| 11.4 | SSF Tool 11 -- Min 4 Det/Fault | 692 | 161 | 197 | 136 | 106 |
| 11.5 | SSF Tool 11 -- Min 5 Det/Fault | 859 | 201 | 244 | 170 | 131 |
| 11.6 | SSF Tool 11 -- Min 7 Det/Fault | 1,194 | 275 | 339 | 234 | 161 |
| 11.7 | SSF Tool 11 -- Min 10 Det/Fault | 1,633 | 380 | 478 | 324 | 207 |
| 11.8 | SSF Tool 11 -- Min 12 Det/Fault | 1,933 | 452 | 564 | 379 | 250 |
| 11.9 | SSF Tool 11 -- Min 15 Det/Fault | 2,350 | 561 | 706 | 466 | 313 |

Table A-2 Transition fault coverage of multiple-detect SSF test sets for each CUT

| Test set | | Fault coverage | | | | |
|---|---|---|---|---|---|---|
| | | ROB | STD | ELM | MUL | SQR |
| 7.1 | Transition Fault, ATPG Tool 5 | 98.90% | 99.66% | 100.00% | 85.31% | 83.03% |
| 2.6 | SSF Tool 4 (100%, gate faults) | 84.53% | 87.61% | 87.50% | 94.04% | 87.70% |
| 2.12 | SSF Tool 4 -- Min 5 Det/Fault | 98.26% | 99.60% | 99.24% | 98.64% | 94.17% |
| 2.13 | SSF Tool 4 -- Min 15 Det/Fault | 99.80% | 100.00% | 100.00% | 99.18% | 94.77% |
| 11.1 | SSF Tool 11 (100%, gate faults) | 84.88% | 84.63% | 89.26% | 88.08% | 80.38% |
| 11.2 | SSF Tool 11 -- Min 2 Det/Fault | 94.11% | 94.78% | 95.95% | 95.44% | 88.56% |
| 11.3 | SSF Tool 11 -- Min 3 Det/Fault | 96.17% | 96.79% | 97.48% | 97.26% | 90.92% |
| 11.4 | SSF Tool 11 -- Min 4 Det/Fault | 97.85% | 97.42% | 98.42% | 98.25% | 93.23% |
| 11.5 | SSF Tool 11 -- Min 5 Det/Fault | 97.85% | 98.57% | 98.83% | 98.43% | 93.44% |
| 11.6 | SSF Tool 11 -- Min 7 Det/Fault | 98.85% | 99.60% | 99.53% | 98.69% | 93.79% |
| 11.7 | SSF Tool 11 -- Min 10 Det/Fault | 97.77% | 99.89% | 99.88% | 98.95% | 93.87% |
| 11.8 | SSF Tool 11 -- Min 12 Det/Fault | 97.65% | 99.77% | 99.82% | 99.09% | 93.87% |
| 11.9 | SSF Tool 11 -- Min 15 Det/Fault | 97.91% | 99.89% | 99.82% | 99.18% | 94.26% |

Table A-3 Characteristics of dies that had test escapes at very slow timing in the retest

| CUT | 5V | 2.5V | 1.7V |
|---|---|---|---|
| 1 (#93 in [3]) | failed only exhaustive tests at rated timing and both pulse-width generated and at-speed clocking modes; passed all the tests at both slow and very slow timing; max. IDDQ = 153.2μA | failed only the exhaustive test at rated timing; passed all the tests at very slow timing | failed all the tests at rated timing; passed all the tests at very slow timing |
| 2 (#63 in [3]) | failed only the exhaustive test at rated timing and at-speed clocking mode; passed all the tests at both slow and very slow timing; max. IDDQ = 477.2 μA | failed only the exhaustive test at rated timing; passed all the tests at very slow timing | failed all the tests at both rated and very slow timing; 53 out of 54 test sets had the same failure counts for both timing. |
| 3 (#96 in [3]) | failed some tests at rated and slow timing; passed all the tests at very slow timing; max. IDDQ = 9 μA | failed all the tests; behaved as having TIC defects | failed all the tests; behaved as having TIC defects |
| 4 (#79 in [3]) | failed some tests at rated and slow timing; passed all the tests at very slow timing; max. IDDQ > 800 μA | behaved as having TIC defects | behaved as having TIC defects |
| 5 (no # in [3]) | failed all tests at rated timing; failed some tests at slow timing; passed all the tests at very slow timing; max. IDDQ = 563.8 μA | failed all the tests; behaved as having TIC defects | failed all the tests; behaved as having TIC defects |
| 6 (#98 in [3]) | failed some tests at rated and slow timing; passed all the tests at very slow timing; max. IDDQ > 800 μA | passed all the tests | passed all the tests |
| 7 (#76 in [3]) | failed some tests at rated timing, passed all the tests at slow and very slow timing; max. IDDQ = 1.8 μA | passed all the tests | passed all the tests |
| 8 (#1 in [3]) | passed some tests that failed at rated timing when tested at slow and very slow timing; max. IDDQ = 39.2 μA | failed all the tests; behaved as having TIC defects | failed all the tests; behaved as having TIC defects |