ANALYSIS OF POCKET DOUBLE GATE TUNNEL FET FOR LOW STAND BY POWER LOGIC CIRCUITS

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ABSTRACT

For low power circuits downscaling of MOSFET has a major issue of scaling of voltage which has ceased after 1V. This paper highlights comparative study and analysis of pocket double gate tunnel FET (DGTFET) with MOSFET for low standby power logic circuits. The leakage current of pocket DGTFET and MOSFET have been studied and the analysis results shows that the pocket DGTFET gives the lower leakage current than the MOSFET. Further a pocket DGTFET inverter circuit is design in 32 nm technology node at V_{DD} =0.6 V. The pocket DGTFET inverter shows the significant improvement on the leakage power than multi-threshold CMOS (MTCMOS) inverter. The leakage power of pocket DGFET and MTCMOS inverter are 0.116 pW and 1.83 pW respectively. It is found that, the pocket DGTFET can replace the MOSFET for low standby power circuits.

KEYWORDS

Pocket DGTFET, Band to Band Tunneling (BTBT), Leakage Current, MTCMOS Inverter

1. INTRODUCTION

With the scaling down of MOSFET, the voltage which can be applied to the gate must be reduced to maintain reliability. At the same time to maintain reliability, threshold voltage of the MOSFET has to be reduced. When gate oxide thickness reduces to about 1.2 nm or less, the electron tunneling occurs abruptly between gate and channel due high electric field. Power consumption goes high because of increase in sub-threshold leakage current [1-4]. To reduce leakage current alternatives were seeking, double gate MOSFET, tri gate and gate all around [5-10]**.** For the past few years TFET is promising candidate to overcome the issue related with MOSFET, because of less sub threshold slope (SS), lower leakage current and scaled supply voltage made this device suitable for low power applications. DGTFET shows improved characteristics including higher drive current and 57mV/dec sub-threshold slope then single gate TFET [11-19]. Low stand by power (LSTP) devices place the accent on low voltage and low leakage devices for their operation. This application requires devices which can minimize their leakage current during sleep mode. This is also an issue with other high performance (HP) and low operating power (LOP) circuits, because sleep mode leakage power contributes to total power consumption. Conventionally the low standby power (LSTP) circuits are designed using technique of power gating in which sleep circuit is added to reduce standby leakage current by shutting off the flow of current to blocks of the circuit that are not currently in use [20]**.** In the present work, the design and implementation of pocket DGTFET at device as well as circuit level is carried out through the simulations and compared to the CMOS counterpart.

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2. DEVICE STRUCTURE AND SIMULATION

The device structure of pocket DGTFET is shown in Fig. 1, Two-dimensional device simulations are performed for the device structure using the Version 5.11.24.C ATLAS device simulator [21]. The trivalent doping of 1×10^{20} /cm^3 for source and pentavalent doping of 1×10^{20} /cm^3 for drain are used. HfO_2 is used as high-k dielectric (having ε=29) equivalent oxide thickness 2 nm. Gate leakage is enabled in our simulations because of very thin gate oxide layer.

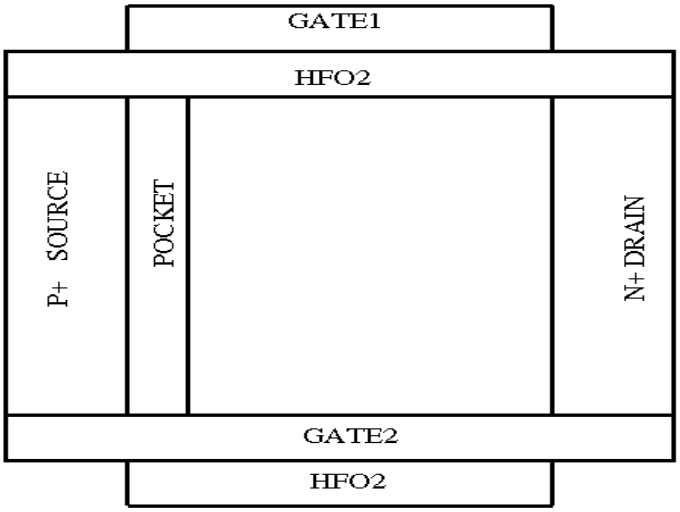

Figure 1 Device structure of pocket DGTFET.

Contacts are made of aluminum, and for gate contact, work function is set to be 4.1 eV. We have used nonlocal band to band tunneling (BTBT) model combined with a band gap narrowing model, trap assisted tunneling, shirata, mobility, quantum density-gradient and oxide tunneling model for present simulations.

3. RESULTS AND DISCUSSIONS

3.1. Leakage Current of Pocket DGTFET and MOSFET

The impact on leakage current, due to the mode of operations of both pocket MOSFET and DGTFET can be understand with energy band diagrams as shown in Fig. 2 and Fig. 3. The TFET works on the principle of band to band tunneling rather than thermionic injections of charge carriers than MOSFET counterpart. Because of BTBT in pocket DGTFET low leakage current exits as shown in Fig. 4. Applying a negative gate voltage pulls the energy bands up. A conductive channel opens as soon as the channel valence band has been lifted above the source conduction band because carriers can now tunnel into empty states of the channel.

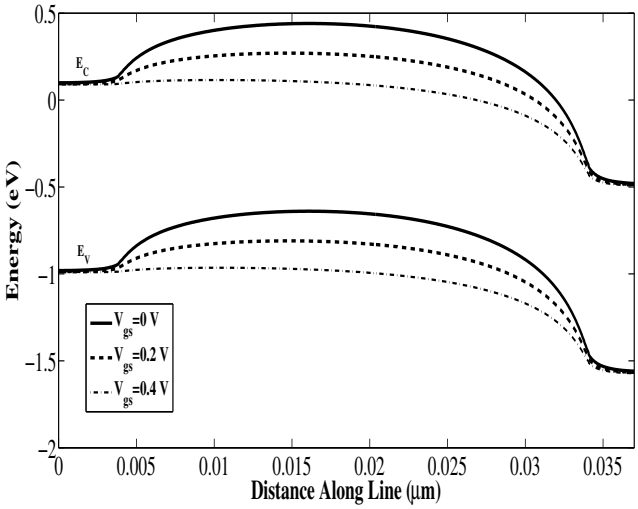

Fig. 2 Energy band diagrams of MOSFET

Because only carriers in the energy window can tunnel into the channel, the energy distribution of carriers from the source is limited; the high-energy part of the source Fermi distribution is effectively cut off. When the gate voltage exceeds the threshold voltage, the potential barrier between the channel and the source becomes narrow enough to allow a significant tunneling current, which is called ON state.

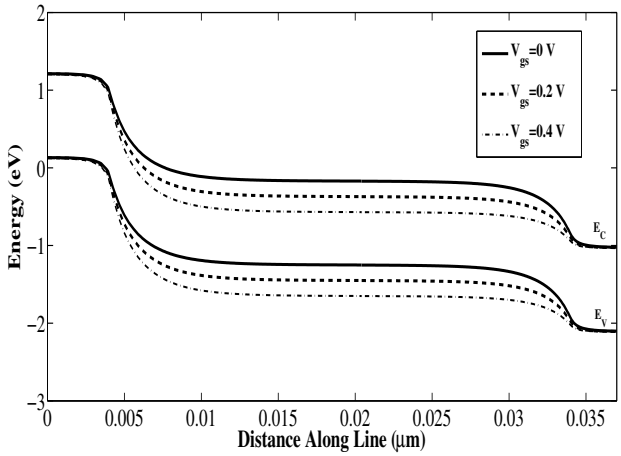

Fig.3 Energy band diagrams of pocket DGTFET

When pocket DGTFET is in its OFF state, the valence band edge of the channel is located below the conduction band edge of the source, leading to very small OFF-state currents. That are dictated by the reverse-biased p-i-n diode a given gate voltage swing compared to the MOSFETs, making the pocket DGTFET architecture an attractive to low supply voltage (V_{DD}) digital logic circuits.

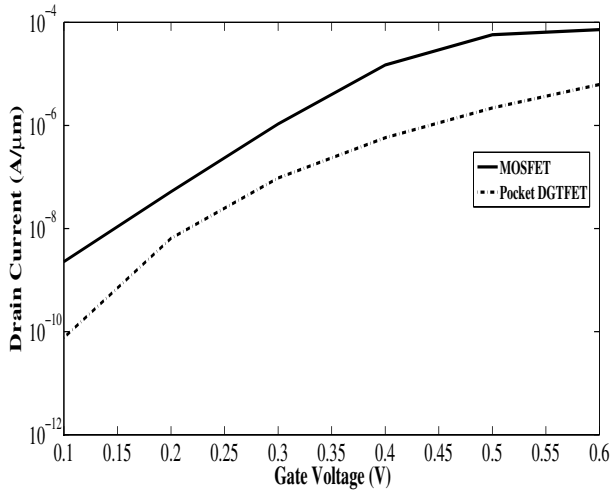

Fig. 4 Transfer characteristics (log scale) of Pocket DGTFET and MOSFET

3.2. Design of Low leakage MTCMOS Inverter

The leakage current is dominant factor for performance degradation of CMOS circuits. To improve the performance of CMOS circuits power gating techniques are used i.e. MTCMOS. The symbol and transient response of MTCMOS inverter are shown in Fig. 5 and Fig. 6 respectively. We have used 32nm technology node for SPICE simulations at V_{DD}=0.6 V. When sleep signal is not enabling, logic circuit will be its normal mode of operations according to input signal. As sleep signal goes high, logic block will be disconnected from power supply and data is retain their previous value because of virtual V_{DD}. In CMOS circuits sleep device is added to reduce the leakage current of circuit in OFF state. The MTCMOS inverter shows good agreement with leakage current reduction for CMOS circuits at the cost of extra circuit overhead.

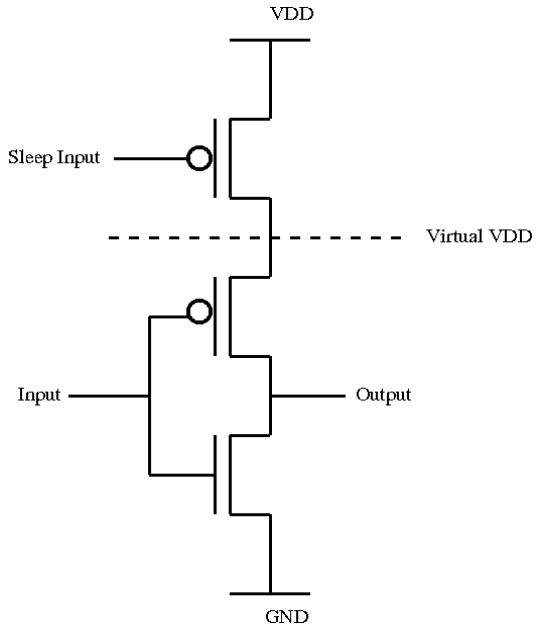

Fig. 5 MTCMOS inverter symbol

The leakage current and leakage power of active mode of MTCMOS inverter are 1.25 pA and 0.75 pW respectively. During standby mode of MTCMOS inverter the leakage current and leakage power is 1.8 pA and 3.05 pW have been observed.

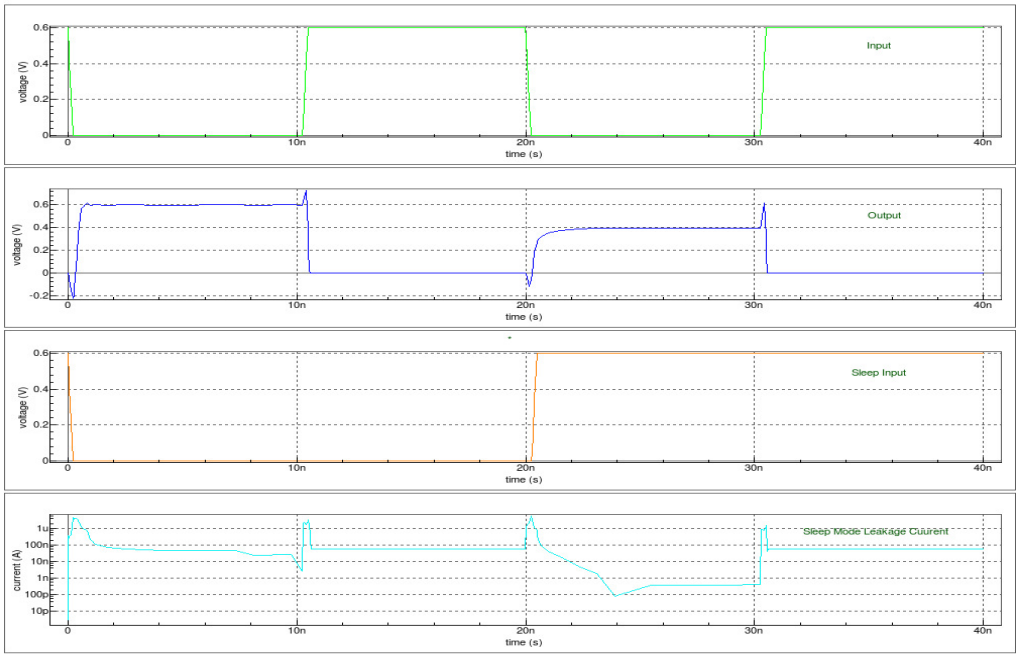

Fig. 6 Transient Response of MTCMOS inverter

It is clear from the transient response of MTCMOS inverter that, there are spikes at the output waveforms (voltage and current waveforms) during low to high or high to low transitions of input waveform. This is because of ground bounce noise i.e. when transition occurs; it takes finite time to switch from one level to other level of transition.

3.3. Design of Low leakage Pocket DGTFET Inverter

In order to designing a device one should have a basic idea of the parameters affecting the device and thus choose the appropriate parameters so to get the desired output and to implement the device in the required circuits. As for devices working at sub-threshold voltage region requires a sufficient amount of ON current (~10^{-6} amp) with a minimum leakage current (~ 10^{-13} amp). The ON state current of conventional TFET is not sufficient to drive the circuits, to fulfil this requirement of conventional TFET, pocket DGTFET devices are used to making the circuits. In pocket DGTFET, due to heavily doped pocket, bands are much closer at tunneling junction (i.e. reduced tunneling width). The effective tunneling area gets increased resulting higher ON current in pocket DGTFET than MOSFET counterpart. Since compact models of TFET are not available, therefore simulations are carried out using device-circuit co-design approach [21]. The symbol and transient response of Pocket DGTFET inverter are shown in Fig. 7 and Fig. 8 respectively.

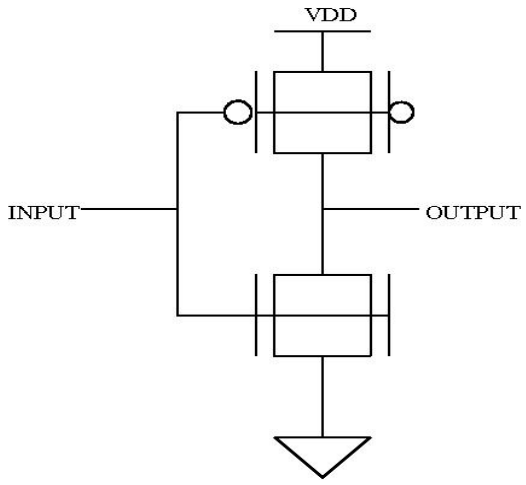

Fig. 7 Pocket DGTFET inverter symbol

The performance of pocket DGTFET inverter is compared with MTCMOS inverter and it is noticed that pocket DGTFET inverter drain less leakage current than MTCMOS counterpart.
The leakage current and leakage power of pocket DGTFET inverter are 194.4 fA and 0.116 pW respectively. As shown in transient analysis of pocket DGTFET, the voltage overshoot, which is expected in conventional TFET, similar behaviour is observed in pocket DGTFET. The voltage overshoot in pocket DGTFET is the consequence of larger Miller capacitance. The gate to drain capacitance (C_{gd}) is the main dominating component of Miller capacitance in case of pocket DGTFET. However in case of MTCMOS inverter (clearly shown in Fig. 8) suffers from voltage overshoot because of ground bounce noise rather than Miller capacitance discussed above section.

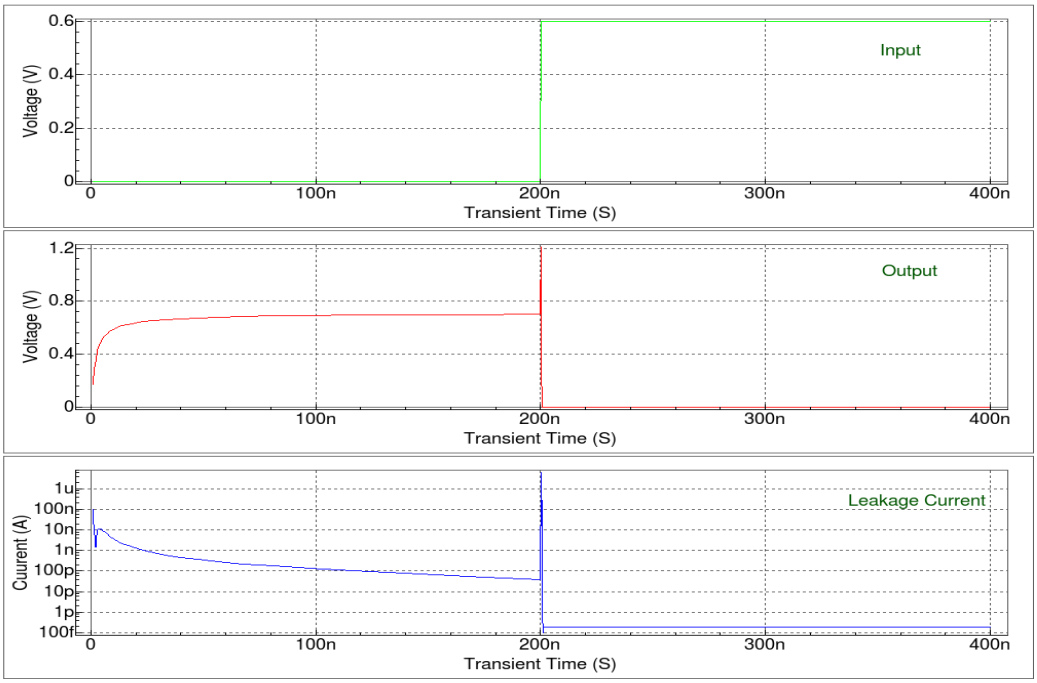

Fig. 8 Transient Response of pocket DGTFET

4. CONCLUSIONS

Present work focuses the performance comparisons of pocket DGTFET for low standby power circuits. The leakage current of pocket DGTFET and MOSFET have been studied and the analysis results shows that the pocket DGTFET gives the lower leakage current than the MOSFET. Further design of Inverter circuit using pocket DGTFET and MTCMOS inverter has been discussed. The leakage current and leakage power of both pocket DGTFET and MTCMOS inverter are 194.4 fA, 1.8 pA and 0.116 pW, 3.05 pW respectively. Based on simulation results and analysis it is found that leakage power is more in MTCMOS inverter than pocket DGTFET inverter. Pocket DGTFET exhibit high performance to design low leakage logic circuits

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