Analysis of Power Consumption and Linearity in Capacitive Digital-to-Analog Converters Used in Successive Approximation ADCs

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***Abstract*—Successive-approximation analog-to-digital converters (SA-ADCs) are widely used in ultra-low-power applications. In this paper, the power consumption and the linearity of capacitive-array digital-to-analog converters (DACs) employed in SA-ADCs are analyzed. Specifically, closed-form formulas for the power consumption as well as the standard deviation of INL and DNL for three commonly-used radix-2 architectures including the effect of parasitic capacitances are presented and the structures are compared. The proposed analysis can be employed in choosing the best architecture and optimizing it in both hand calculations and computer-aided-design tools. Measurement results of previously published works as well as simulation results of a 10-bit 10 kS/s SA-ADC confirm the accuracy of the proposed equations. It will be shown that, in spite of what commonly is assumed, although the total capacitance and the power consumption of those architectures employing attenuating capacitors seem to be smaller than conventional binary-weighted structures, the linearity requirements impose much larger unit capacitance to the structure such that the entire power consumption is larger.**

***Index Terms*—Capacitor-based DAC, capacitor matching, DNL, INL, power dissipation, successive approximation ADC.**

I. Introduction

SUCCESSIVE approximation analog-to-digital converters (SA-ADCs) have recently become very attractive in low-power moderate-resolution/moderate-speed applications such as wireless sensor nodes or implantable biomedical devices due to their minimal active analog circuit requirements and low power consumption [1]–[7]. The conventional structure of an SA-ADC, as shown in Fig. 1, consists of a sample-and-hold (S/H) circuit, a comparator, a successive approximation register (SAR), and a digital-to- analog converter (DAC). The operation of the SA-ADC is as follows. In the sampling phase, the analog input signal is sampled by the S/H circuit (producing $\mathrm{V_H}$) and does not change during the conversion phase. During the conversion phase, the SAR and control logic perform a binary search algorithm, which constructs the binary word. This binary word is fed through the DAC (producing $\mathrm{V_{DAC}}$) and compared with the sampled analog input signal $(\mathrm{V_H})$. In other words, during the first clock cycle in the conversion phase the comparator defines whether the analog sampled voltage $(\mathrm{V_H})$ is smaller or greater than $\mathrm{V_{DAC}} = \mathrm{V_{ref}}/2$. Based on this result the most significant bit (MSB) is determined and stored in the SAR. In the second clock cycle, the output of the DAC is increased or decreased by $\mathrm{V_{ref}}/4$ according to the result of the first clock cycle and the second significant bit is found. During the next clock cycles $\mathrm{V_{DAC}}$ tracks $\mathrm{V_H}$ until the difference between them becomes less than $1\mathrm{V_{LSB}}$ where $\mathrm{V_{LSB}}$ is the value of the least-significant-bit voltage. Therefore, after N clock cycles in the conversion phase, all N bits of the digital word will be ready. It should be noted that in many recent architectures the S/H function is realized by the capacitive DAC itself [5]–[8]. In other words, the capacitive array used in the DAC part also serves as the S/H capacitor.

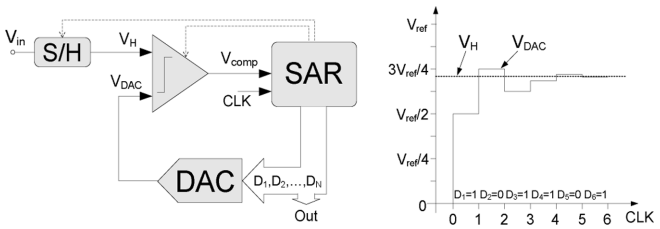

Fig. 1. Principle of SA-ADC operation.

In an SA-ADC the power is mainly consumed in the DAC, the comparator, the reference buffers and the digital circuits. One of the most important building blocks that determine the accuracy and conversion speed of the converter and also consume most of the overall power dissipation of the SA-ADC, is the DAC [5]. The DAC required in the SA-ADC can be realized in various ways; e.g., capacitor-based DAC [8]–[32], switched-current DAC [33]–[35] or R-2R ladder DAC [36]–[39]. Among these architectures, the capacitor-based DAC has become more popular because of its zero quiescent current. Furthermore, in most technologies resistor mismatch and tolerance are greater than capacitor mismatch and tolerance.

Several structures have been proposed to implement capacitor-based DACs for SA-ADCs for both radix-2 [8]–[25] and non-radix-2 architectures [26]–[28]. In radix-2 capacitive-array DACs, the digital circuit is simple, yet the matching of capacitors in the array is essential; on the other hand, in non-radix-2 architectures, the matching requirement in the capacitive array can be more relaxed but the digital circuit has a larger complexity [28]. Several methods have

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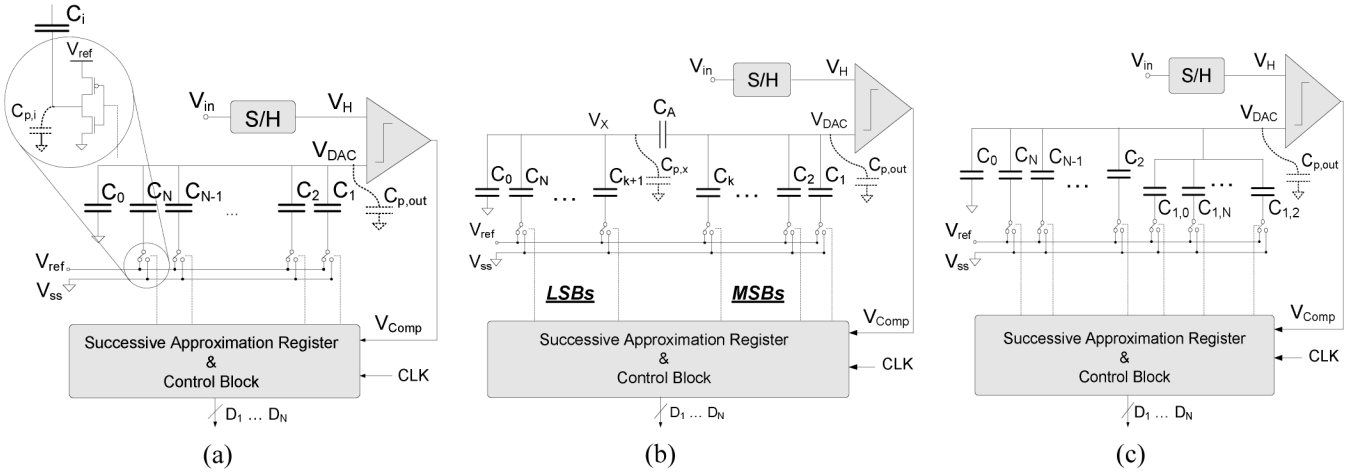

Fig. 2. Schematic of an SA-ADC with (a) a CBW DAC (b) a BWA DAC (c) a SBW DAC.

been proposed in literature for implementation of radix-2 capacitive-array DACs, such as conventional binary-weighted capacitive-array DAC [4]–[11], binary-weighted capacitive-array DAC with attenuation capacitor [12]–[15], split binary-weighted capacitive-array DAC [15]–[17], SA-ADC with dual binary-weighted capacitive-array DAC [18], [19] and C-2C capacitive-array DAC [20]–[23]. All of these radix-2 capacitor-array architectures are based on three fundamental structures, i.e., conventional binary-weighted (CBW) capacitive array, binary-weighted capacitive array with attenuation capacitor (BWA) and split binary-weighted (SBW) capacitive-array DAC, as depicted in Fig. 2. The operation of these architectures will be explained in Section II.

As the energy consumed in charging the capacitors of these capacitor-based DACs is one of the main sources of energy consumption in the ADC and even it determines the lower bound on the ADC energy consumption [5], the main purpose of this paper is to present a comprehensive yet accurate analysis about the power consumption of the capacitive-array DACs due to capacitor switching supplied by the reference voltage source. In order to be able to analyze the power consumption of these structures, one should note that the capacitor switching power consumption is directly proportional to the size of the unit capacitor in the capacitive array [10], [17], [18]. In practice, the smallest possible value for unit capacitor is determined by one of the followings: kT/C noise requirement, capacitor matching, design rules and the size of the parasitic capacitances [10]. The capacitor matching and parasitic capacitances which directly affect non-linearity parameters of the ADC such as integral non-linearity (INL) and differential non-linearity (DNL) are the dominant factors for medium resolutions. Therefore, any comparison between different architectures from power consumption viewpoint cannot be fairly accomplished without comparing their linearity performances. The standard deviations of the INL and the DNL determine the parameters of INL-yield and DNL-yield, important in many applications.

In literature, several useful discussions and analyses have been presented about the power consumption of the capacitive DACs used in SA-ADCs [10], [16], [17], [24]. In [16] and [17] a modified structure and switching algorithm (called as SBW in this paper) has been proposed. Only using a comparative discussion, it has been shown that the power consumption in the SBW architecture is smaller compared to CBW architecture; however, the power consumption of the entire DAC has not been calculated. For the CBW structure, a formula is presented in [10] for a special case of 8 bits with some limiting approximations. But there have not been any attempts to analyze the capacitor switching power consumption for the BWA structure. This paper presents a comprehensive and accurate analysis for the power consumption of the CBW structure and also for the BWA and SBW structures. These calculations have been done for both structures with and without explicit use of S/H circuits.

As for the linearity (i.e., INL/DNL) of the capacitive-array DACs, some useful discussions have been presented as well [16], [25]. In [16] an interesting approach for calculating the standard deviation of the INL and DNL of the CBW and SBW structures has been presented. But there have not been any attempts to analyze the linearity behavior for the BWA structures.

As discussed in this paper it will be shown that if the linearity performance is also considered, the BWA structure is inferior compared to the CBW and SBW structures from the power consumption viewpoint. This fact that is usually overlooked by circuit designers is due to the reduced size of the capacitors in this structure. In addition, presented closed-form formulas for the power consumption and the linearity can be employed in both hand calculations and computer-aided-design tools to optimize the structure and the capacitor values of capacitive DACs. Furthermore, in this paper the effect of the parasitic capacitances on the power consumption and the linearity performance is analyzed and discussed.

The rest of this paper is organized as follows. In Section II the power consumption of the capacitor-based DAC due to capacitor switching will be analyzed. Section III presents a statistical comparative analysis for INL and DNL characteristics of SA-ADCs employing the capacitive-array DACs. Section IV presents the simulation results of our design as well as measurement and simulation results of other published works which verify the accuracy of the proposed closed-form equations. In addition, in this section a comprehensive comparison between

three commonly-used architectures will be presented. Finally the paper is concluded in Section V.

II. Power Consumption of Capacitive-Array DAC Due to Capacitor Switching

In this section, the power consumption of the DAC part of an SA-ADC with a radix-2 capacitive-array structure due to capacitor switching, supplied by the reference voltage ($\mathrm{V_{ref}}$), will be calculated. These calculations will be performed for the three different architectures depicted in Fig. 2 being CBW, BWA, and SBW structures. Although many recent structures of SA-ADCs have realized the S/H circuit by capacitive-array DAC, for simplicity in calculations, in subsections A-C the structures with an additional S/H circuit are analyzed. Then in subsection D, it will be shown that both structures, with and without additional S/H circuit, consume the same amount of switching power. Note that the effect of parasitic capacitors is excluded from the analysis in subsections A-C. It will be addressed in subsection E.

A. Conventional Binary-Weighted Capacitive Array (CBW)

The conventional structure of an SA-ADC with a binary-weighted capacitive-array DAC, as shown in Fig. 2(a), consists of a S/H circuit, a comparator, an SAR, and a binary-weighted capacitive-array DAC [8]–[11]. In the sampling phase, the analog input signal is fed through a S/H circuit, so that the sampled voltage does not change during the entire conversion phase. In the conversion phase, during the first clock cycle, the MSB capacitor ($\mathrm{C_1}$) is connected to $\mathrm{V_{ref}}$ with the remaining capacitors connected to ground. The comparator determines if the sampled voltage ($\mathrm{V_H}$) is larger or smaller than the output voltage of the capacitive-array DAC (i.e., $\mathrm{V_{DAC}}$ that equals $0.5\mathrm{V_{ref}}$ in this clock cycle). Therefore, the MSB bit ($\mathrm{D_1}$) is determined and stored in the SAR. During the second clock cycle, $\mathrm{C_2}$ is connected to $\mathrm{V_{ref}}$, $\mathrm{C_1}$ is connected to $\mathrm{D_1V_{ref}}$ ($\mathrm{C_1}$ connected to ground if $\mathrm{D_1} = 0$, else $\mathrm{C_1}$ remains connected to $\mathrm{V_{ref}}$) and the remaining capacitors will be connected to ground. Therefore, $\mathrm{V_H}$ is compared with $\mathrm{V_{DAC}} = 0.25\,\mathrm{V_{ref}}$ (if $\mathrm{D_1} = 0$) or $\mathrm{V_{DAC}} = 0.75\,\mathrm{V_{ref}}$ (if $\mathrm{D_1} = 1$) and the second significant bit ($\mathrm{D_2}$) is determined. This procedure is repeated until all N bits are found.

The power consumption of the reference voltage supply ($\mathrm{V_{ref}}$) due to capacitor switching for an N-bit SA-ADC can be calculated according to [10]

$$P_{V_{\mathrm{ref}}} = \frac{V_{\mathrm{ref}}}{T_s}\sum_{i=1}^{N} Q_i \tag{1}$$

where $\mathrm{T_s}$ represents the time period during which a sample is converted and $\mathrm{Q_i}$ is the total charge that $\mathrm{V_{ref}}$ supplies to the capacitive-array DAC during the ith clock cycle in the conversion phase. In most structures, one clock cycle is allocated for the sampling phase and N clock cycles for the conversion phase. Thus, $\mathrm{T_s} = (\mathrm{N}+1)/\mathrm{f_{clk}}$ where $\mathrm{f_{clk}}$ is the clock frequency of the SA-ADC. According to the above discussion on the CBW structure operation, $\mathrm{Q_i}$ can be calculated at each clock cycle according to

$$\begin{aligned}
Q_1 &= C_1[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_1}) - (0-0)]\\
Q_2 &= C_2[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_2}) - (0 - V_{\mathrm{DAC}_1})]\\
&\quad + C_1D_1[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_2}) - (V_{\mathrm{ref}} - V_{\mathrm{DAC}_1})]\\
Q_3 &= C_3[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_3}) - (0 - V_{\mathrm{DAC}_2})]\\
&\quad + (C_1D_1 + C_2D_2)\\
&\quad \times [(V_{\mathrm{ref}} - V_{\mathrm{DAC}_3}) - (V_{\mathrm{ref}} - V_{\mathrm{DAC}_2})]
\end{aligned} \tag{2}$$

Similar deduction leads to a more general expression for the ith clock cycle as

$$\begin{aligned}
Q_i &= C_i[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_i}) - (0 - V_{\mathrm{DAC}_{i-1}})]\\
&\quad + \left(\sum_{j=1}^{i-1} C_jD_j\right)[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_i})\\
&\quad - (V_{\mathrm{ref}} - V_{\mathrm{DAC}_{i-1}})]\\
&= C_iV_{\mathrm{ref}} + \left(C_i + \sum_{j=1}^{i-1} C_jD_j\right)(V_{\mathrm{DAC}_{i-1}} - V_{\mathrm{DAC}_i})\\
&\qquad\qquad i \geq 2
\end{aligned} \tag{3}$$

where the value of $\mathrm{V_{DAC,i}}$ and $\mathrm{C_i}$ are given by

$$C_i = 2^{N-i}C_0, \quad C_{\mathrm{total}} = C_0 + \sum_{i=1}^{N} C_i \tag{4}$$

$$V_{\mathrm{DAC}_i} = \frac{C_i + \sum_{j=1}^{i-1} C_jD_j}{C_{\mathrm{total}}}V_{\mathrm{ref}} \tag{5}$$

where $\mathrm{C_0}$ is the capacitance of the unit capacitor.

By combining (5) and (4) with (3), $\mathrm{Q_i}$ can be rewritten as

$$\begin{aligned}
Q_i &= 2^NC_0V_{\mathrm{ref}}\\
&\quad \times \left\{\frac{1}{2^i} + \frac{2^NC_0}{C_{\mathrm{total}}}\left(\frac{1}{2^i} + \sum_{j=1}^{i-1}\frac{D_j}{2^j}\right)\left(\frac{1}{2^i} - \frac{D_{i-1}}{2^{i-1}}\right)\right\}
\end{aligned} \tag{6}$$

and the total charge that $\mathrm{V_{ref}}$ supplies to the capacitive-array DAC can be calculated from

$$\begin{aligned}
&\sum_{i=1}^{N} Q_i\\
&\quad = Q_1 + \sum_{i=2}^{N} Q_i\\
&\quad = 2^NC_0V_{\mathrm{ref}}\left(\frac{1}{2}\right) + 2^NC_0V_{\mathrm{ref}}\\
&\qquad \times \left\{\begin{array}{l}\displaystyle\sum_{i=2}^{N}\frac{1}{2^i} + \sum_{i=2}^{N}\frac{1}{2^{2i}} + \sum_{i=2}^{N}\left(\frac{1}{2^i}\sum_{j=1}^{i-1}\frac{D_j}{2^j}\right)\\ \displaystyle -\sum_{i=2}^{N}\left(\frac{D_{i-1}}{2^{i-1}}\sum_{j=1}^{i-1}\frac{D_j}{2^j}\right) - \sum_{i=2}^{N}\left(\frac{1}{2^i}\frac{D_{i-1}}{2^{i-1}}\right)\end{array}\right\}.
\end{aligned} \tag{7}$$

In the above equation, the first term is related to Q_1 (i.e., the charge consumed in the first clock cycle) calculated from (2).

In order to simplify (7), the following relations can be used

$$\sum_{i=2}^{N}\left(\frac{1}{2^i}\sum_{j=1}^{i-1}\frac{D_j}{2^j}\right)=\sum_{i=1}^{N-1}\left(\frac{D_i}{2^i}\right)^2-\left(\frac{1}{2}\right)^N\sum_{i=1}^{N-1}\frac{D_i}{2^i}$$
$$\sum_{i=2}^{N}\left(\frac{1}{2^i}\frac{D_{i-1}}{2^{i-1}}\right)=\frac{1}{2}\sum_{i=1}^{N-1}\left(\frac{D_i}{2^i}\right)^2$$
$$\sum_{i=2}^{N}\left(\frac{D_{i-1}}{2^{i-1}}\sum_{j=1}^{i-1}\frac{D_j}{2^j}\right)=\frac{1}{2}\left(\sum_{i=1}^{N-1}\frac{D_i}{2^i}\right)^2+\frac{1}{2}\sum_{i=1}^{N-1}\left(\frac{D_i}{2^i}\right)^2. \tag{8}$$

Using (8) and (7) in (1) and after simplification, it can be concluded that the power that the reference voltage source ($\mathrm{V_{ref}}$) supplies to the capacitive-array DAC, denoted by $P_{V_{\mathrm{ref}}}$ is

$$P_{V_{\mathrm{ref}}}\approx\frac{2^N f_{\mathrm{clk}}C_0}{N+1}\times\left\{\left(\frac{5}{6}-\left(\frac{1}{2}\right)^N-\frac{1}{3}\left(\frac{1}{2}\right)^{2N}\right)V_{\mathrm{ref}}^2-\frac{1}{2}V_{\mathrm{in}}^2-\left(\frac{1}{2}\right)^N V_{\mathrm{in}}V_{\mathrm{ref}}\right\}. \tag{9}$$

where $V_{\mathrm{in}}=\sum_{i=1}^{N}(D_i)/(2^i)V_{\mathrm{ref}}$ is the equivalent analog voltage of the corresponding digital word. The accuracy of this equation will be verified in Section IV.

B. Binary-Weighted Capacitive Array With Attenuation Capacitor (BWA)

As demonstrated in the previous section, the power consumption of an SA-ADC due to capacitor switching is proportional to the total capacitance of the capacitive-array DAC. In addition, the major speed limitation of an SA-ADC is often related to the *RC* time constant composed by the value of the capacitance of the capacitor array and the resistance of the reference ladder and switches. On the other hand, in the CBW structure, the total capacitance rises exponentially with the ADC resolution leading to an exponential increase in the power consumption and *RC* time constant.

In literature, several attempts have been made to solve this problem. One of the most popular solutions is to employ an attenuating capacitor in the binary-weighted capacitor array [12]–[15] to split the capacitor array into k MSBs and $m=N-k$ LSBs as shown in Fig. 2(b). Therefore, the values of the capacitors related to the MSBs are decreased by a factor of 2^{m} in comparison to the conventional architecture. Thus, the power consumption and the *RC* time constant of DAC will be decreased. Note that the switching sequence of this architecture is similar to that of the CBW structure. The value of each capacitor is given by

$$C_i=\begin{cases}2^{k-i}C_0 & 1\le i\le k\\ 2^{N-i}C_0 & k+1\le i\le N\end{cases}$$
$$C_A=\frac{2^m}{(2^m-1)}C_0 \tag{10}$$

and also

$$C_{k_{\mathrm{total}}}=\sum_{i=1}^{k}C_i=(2^k-1)C_0$$
$$C_{m_{\mathrm{total}}}=C_0+\sum_{i=k+1}^{N}C_i=2^mC_0. \tag{11}$$

In order to calculate the overall power consumption of this structure due to capacitor switching, the total charge that $\mathrm{V_{ref}}$ supplies to the capacitive-array DAC during the k-bit MSB and m-bit LSB conversions will be calculated separately and then used in (1).

As is clear from Fig. 2(b), all capacitors related to the m-bit LSBs are connected to ground during the k-bit MSB conversions. Therefore, the equivalent capacitance of the series combination of $\mathrm{C_A}$ and the LSB capacitors is equal to a unit capacitor ($\mathrm{C_0}$) and the power calculation is the same as a k-bit CBW structure with a unit capacitor of $\mathrm{C_0}$. Hence, from (9) it follows that

$$\sum_{i=1}^{k}Q_i=2^kC_0V_{\mathrm{ref}}\times\left\{\frac{5}{6}-\left(\frac{1}{2}\right)^k-\frac{1}{3}\left(\frac{1}{4}\right)^k-\frac{1}{2}\left(\sum_{i=1}^{k-1}\frac{D_i}{2^i}\right)^2-\left(\frac{1}{2}\right)^k\sum_{i=1}^{k-1}\frac{D_i}{2^i}\right\}. \tag{12}$$

For calculating the total charge consumption during the m-bit LSB conversions, one must consider that each of the k-bit MSB capacitors is connected to either $\mathrm{V_{ref}}$ or ground based on the value of $\mathrm{D_i}$ (i.e., the corresponding ith digital bit ($1\le \mathrm{i}\le \mathrm{k}$)) already determined during the previous clock cycles. Similarly for a conventional structure, the charge consumption in each clock cycle is obtained from

$$Q_i=C_iV_{\mathrm{ref}}+\left(C_i+\sum_{j=k+1}^{i-1}C_jD_j\right)(V_{X_{i-1}}-V_{X_i})+\left(\sum_{j=1}^{k}C_jD_j\right)(V_{\mathrm{DAC}_{i-1}}-V_{\mathrm{DAC}_i}),\quad i\ge k+1 \tag{13}$$

where $\mathrm{V_{X,i}}$ and $\mathrm{V_{DAC,i}}$, (node voltages annotated in Fig. 2(b)) are given by

$$V_{X_i}=\left(\frac{C_i+\sum_{j=k+1}^{i-1}C_jD_j}{C_{m_{\mathrm{total}}}+C_A\|C_{k_{\mathrm{total}}}}+\frac{\sum_{j=1}^{k}C_jD_j}{C_{k_{\mathrm{total}}}+C_A\|C_{m_{\mathrm{total}}}}\times\frac{C_A}{C_A+C_{m_{\mathrm{total}}}}\right)V_{\mathrm{ref}} \tag{14}$$

and

$$V_{\mathrm{DAC}_i}=\left(\frac{C_i+\sum_{j=k+1}^{i-1}C_jD_j}{C_{m_{\mathrm{total}}}+C_A\|C_{k_{\mathrm{total}}}}\times\frac{C_A}{C_A+C_{k_{\mathrm{total}}}}+\frac{\sum_{j=1}^{k}C_jD_j}{C_{k_{\mathrm{total}}}+C_A\|C_{m_{\mathrm{total}}}}\right)V_{\mathrm{ref}}. \tag{15}$$

Substituting (14) and (15) in (13) and following a similar procedure as for the CBW structure, the total charge consumption during the m-bit LSB conversions can be also obtained. Thus, it can be shown that the overall capacitor switching power consumption can be calculated from (16), shown at the bottom of the page. As discussed later in Section IV, it can be shown that the power consumption is minimal if $\mathrm{m} = \mathrm{k} = \mathrm{N}/2$ (assuming N is even). For this case and for large values of N, (16) can be simplified to

$$P_{V_{\mathrm{ref}}} \approx \frac{2^{\frac{N}{2}} f_{\mathrm{clk}} C_0 V_{\mathrm{ref}}^2}{N+1} \times \left\{ \frac{10}{6} - \frac{1}{2}\left(\sum_{i=1}^{\frac{N}{2}-1} \frac{D_i}{2^i}\right)^2 - \frac{1}{2}\left(\sum_{i=1}^{\frac{N}{2}-1} \frac{D_{\frac{N}{2}+i}}{2^i}\right)^2 \right\}. \quad (17)$$

Simulations show that the approximation error of (17) compared to (16) for $\mathrm{N} \geq 8$ and for a sinusoidal input is less than 4%.

C. Split Binary-Weighted Capacitive Array (SBW)

Another structure and switching sequence has been proposed for the capacitive-array DAC to reduce the power consumption due to capacitor switching in [16], [17]. The structure is a split binary-weighted (SBW) capacitive-array DAC as depicted in Fig. 2(c). In this structure, the MSB capacitor (C_1) of the CBW architecture has been realized as a capacitive binary-weighted sub-array (to be called MSB sub-array) exactly similar to the rest of the main array. Hence, the capacitor values of these two arrays are calculated from

$$C_i = C_{1,i} = 2^{N-i} C_0 \quad 2 \leq i \leq N \quad (18)$$

The switching algorithm of this structure is modified as follows. In the first clock cycle of the conversion phase, all capacitors of the MSB sub-array $(\mathrm{C}_{1,2} \ldots \mathrm{C}_{1,\mathrm{N}}, \mathrm{C}_{1,0})$ are connected to $\mathrm{V}_{\mathrm{ref}}$ and the other capacitors are connected to ground. Hence, the input sampled signal $(\mathrm{V}_{\mathrm{H}})$ is compared with $\mathrm{V}_{\mathrm{DAC}} = 0.5\,\mathrm{V}_{\mathrm{ref}}$ and the result is stored in the SAR (D_1). In the second clock cycle, based on D_1, the output of the DAC $(\mathrm{V}_{\mathrm{DAC}})$ must be increased to 0.75 $\mathrm{V}_{\mathrm{ref}}$ if $\mathrm{D}_1 = 1$ (up transition) or decreased to 0.25 $\mathrm{V}_{\mathrm{ref}}$ if $\mathrm{D}_1 = 0$ (down transition). In the up transition, similarly as for the CBW structure, the main sub-array remains connected to $\mathrm{V}_{\mathrm{ref}}$ and also C_2 is connected to $\mathrm{V}_{\mathrm{ref}}$. But the difference in the switching sequence appears in the down transition where, in the CBW structure, all capacitors of main sub-array or C_1 are discharged to ground and C_2 is connected to $\mathrm{V}_{\mathrm{ref}}$ but in this modified structure, half of the MSB sub-array capacitors $(\mathrm{C}_{1,2})$ are connected back to ground leaving other capacitors of the MSB sub-array connected to $\mathrm{V}_{\mathrm{ref}}$ and the rest unchanged. And this procedure is repeated until all N bits are found. In other words, in each clock cycle if a "down" transition is required, only some of the MSB sub-array capacitors already connected to $\mathrm{V}_{\mathrm{ref}}$ are discharged to ground while all other capacitors remain unchanged. This algorithm will therefore lead to considerable power saving.

In order to calculate the power consumption of this structure due to capacitor switching, the charge consumed from $\mathrm{V}_{\mathrm{ref}}$ in each clock-cycle Q_{i} can be found as

$$\begin{aligned}
Q_1 &= (C_{1,2} + C_{1,3} + \cdots + C_{1,N} \\
&\quad + C_{1,0})[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_1}) - (0 - 0)] \\
Q_2 &= (C_{1,3} + \cdots + C_{1,N} + C_{1,0})[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_2}) \\
&\quad - (V_{\mathrm{ref}} - V_{\mathrm{DAC}_1})] \\
&\quad + D_1 \begin{pmatrix} C_2[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_2}) - (0 - V_{\mathrm{DAC}_1})] \\ +C_{1,2}[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_2}) - (V_{\mathrm{ref}} - V_{\mathrm{DAC}_1})] \end{pmatrix} \\
Q_3 &= (C_{1,4} + \cdots + C_{1,N} + C_{1,0})[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_3}) \\
&\quad - (V_{\mathrm{ref}} - V_{\mathrm{DAC}_2})] \\
&\quad + D_1((C_2 + C_{1,2})[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_3}) \\
&\quad - (V_{\mathrm{ref}} - V_{\mathrm{DAC}_2})]) \\
&\quad + D_2 \begin{pmatrix} C_3[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_3}) - (0 - V_{\mathrm{DAC}_2})] \\ +C_{1,3}[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_3}) - (V_{\mathrm{ref}} - V_{\mathrm{DAC}_2})] \end{pmatrix}
\end{aligned} \quad (19)$$

Similar deduction leads to a more general expression for the ith clock cycle as

$$Q_i = \left(\sum_{j=1}^{i-1} D_j(C_{j+1} + C_{1,j+1}) + \sum_{j=i+1}^{N} C_{1,j} + C_{1,0}\right) \times (V_{\mathrm{DAC}_{i-1}} - V_{\mathrm{DAC}_i}) + D_{i-1} C_i V_{\mathrm{ref}}, \quad i \geq 2 \quad (20)$$

where $\mathrm{V}_{\mathrm{DAC,i}}$ is the output of DAC at ith clock-cycle and is obtained from (5). Also from (5) it is clear that

$$V_{\mathrm{DAC}_{i-1}} - V_{\mathrm{DAC}_i} = \left(\frac{1}{2^i} - \frac{D_{i-1}}{2^{i-1}}\right) V_{\mathrm{ref}}. \quad (21)$$

Now, similarly as for the conventional structure and using (8), it can be shown that $P_{V_{\mathrm{ref}}}$ is obtained from

$$P_{V_{\mathrm{ref}}} \approx \frac{f_{\mathrm{clk}} 2^N C_0}{N+1} \times \left\{ \left(\frac{1}{3} - \frac{1}{3}\left(\frac{1}{4}\right)^N\right) V_{\mathrm{ref}}^2 - \frac{1}{2} V_{\mathrm{in}}^2 + \left(\frac{1}{2} - \left(\frac{1}{2}\right)^N\right) V_{\mathrm{in}} V_{\mathrm{ref}} \right\} \quad (22)$$

The accuracy of this equation will be verified in Section IV as well.

$$P_{V_{\mathrm{ref}}} = \frac{f_{\mathrm{clk}} C_0 V_{\mathrm{ref}}^2}{N+1} \left(\begin{array}{l} 2^k \left\{ \frac{5}{6} - \left(\frac{1}{2}\right)^k - \frac{1}{3}\left(\frac{1}{4}\right)^k - \frac{1}{2}\left(\sum_{i=1}^{k-1} \frac{D_i}{2^i}\right)^2 - \left(\frac{1}{2}\right)^k \sum_{i=1}^{k-1} \frac{D_i}{2^i} \right\} \\ +2^m \left\{ 1 - \left(\frac{1}{2}\right)^m + \frac{2^m C_0}{C_{m_{\mathrm{total}}} + C_A \| C_{k_{\mathrm{total}}}} \left(\frac{1}{12} - \frac{1}{3}\left(\frac{1}{4}\right)^m - \frac{1}{2}\left(\sum_{i=1}^{m-1} \frac{D_{k+i}}{2^i}\right)^2 - \left(\frac{1}{2}\right)^m \sum_{i=1}^{m-1} \frac{D_{k+i}}{2^i} \right) \right. \\ \left. +2^{-m} \left(\sum_{j=1}^{k} \frac{D_j}{2^j}\right) \left(\frac{1}{2} - \left(\frac{1}{2}\right)^m - \sum_{i=1}^{m-1} \frac{D_{k+i}}{2^i} \right) + \frac{1}{2} \left(\frac{1 - D_k}{2^k} \left(\frac{C_A}{C_A + C_{m_{\mathrm{total}}}} \right) - \frac{2^{m-1} C_0}{C_{m_{\mathrm{total}}} + C_A \| C_{k_{\mathrm{total}}}} \right) \right\} \end{array} \right) \quad (16)$$

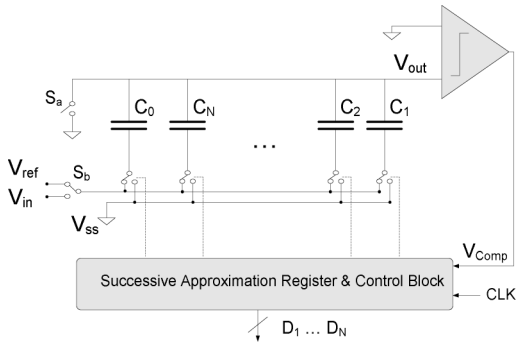

Fig. 3. Conventional SA-ADC without additional S/H circuit.

D. Structures Without an Explicit S/H Circuit

The structures discussed above have employed an additional S/H circuit. However, all three structures mentioned above (i.e., CBW, BWA and SBW) can be used without an additional S/H circuit as shown in Fig. 3 [5]–[8], [13]–[17]. In other words, the S/H function can be realized by the capacitive DAC itself. The operation of these architectures is as follows. In the sampling phase, switch $\mathrm{S_a}$ is closed and $\mathrm{S_b}$ is connected to the input voltage so that the input voltage is sampled on all the capacitors. In the conversion phase, $\mathrm{S_a}$ is opened and $\mathrm{S_b}$ is connected to $\mathrm{V_{ref}}$ and the switching sequence of the capacitors is exactly the same as their counterparts in Fig. 2. In each clock cycle the subtraction of the DAC voltage from the input voltage is compared with zero as

$$V_{\mathrm{out}} = -V_{\mathrm{in}} + V_{\mathrm{DAC}} \tag{23}$$

where $\mathrm{V_{DAC}}$ is obtained from (5).

In these structures since the switching point of the comparator is independent of the input signal, there is no need for a rail-to-rail input common-mode range of the comparator thus avoiding the problem caused by variation of the comparator offset with the input level. On the other side, the input capacitance of the ADC is determined by the entire capacitive array (which can be larger than the previous architectures for matching-limited cases).

The power consumed by the capacitor switching of these structures where the S/H function is performed by the capacitive matrix, will be shown to be similar to their counterparts with explicit S/H circuits, even if the initial charge of the capacitive matrix provided by the input signal is not ignored. This is due to the fact that although the initial charge is different, the voltage changes across the capacitors are the same for two different cases. For example, in the CBW structure and for instance for the first two cycles, the required charge supplied by the reference voltage source is obtained from

$$\begin{aligned} Q_1 &= C_1[(V_{\mathrm{ref}} - (-V_{\mathrm{in}} + V_{\mathrm{DAC}_1})) - (0 - (-V_{\mathrm{in}}))] \\ &= C_1[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_1})] \\ Q_2 &= C_2[(V_{\mathrm{ref}} - (-V_{\mathrm{in}} + V_{\mathrm{DAC}_2})) \\ &\quad - (0 - (-V_{\mathrm{in}} + V_{\mathrm{DAC}_1}))] \\ &\quad + C_1 D_1[(V_{\mathrm{ref}} - (-V_{\mathrm{in}} + V_{\mathrm{DAC}_2})) \\ &\quad - (V_{\mathrm{ref}} - (-V_{\mathrm{in}} + V_{\mathrm{DAC}_1}))] \\ &= C_2[(V_{\mathrm{ref}} + V_{\mathrm{DAC}_2}) - (0 - V_{\mathrm{DAC}_1})] \\ &\quad + C_1 D_1[(V_{\mathrm{ref}} - V_{\mathrm{DAC}_2}) - (V_{\mathrm{ref}} + V_{\mathrm{DAC}_1})]. \end{aligned} \tag{24}$$

As can be seen, there is no difference between (24) and (2).

Similarly, it can be shown that the required power consumption of the BWA and SBW structures with and without additional S/H circuit consume the same amount of power for charging the capacitors.

E. Effect of Parasitic Capacitances on the Power Consumption

In this section the power consumed from the reference voltage due to parasitic capacitances (shown in Fig. 2) in the capacitive-array DACs mentioned above will be discussed. In Fig. 2, $\mathrm{C_{p,out}}$ consists of the entire top-plate parasitic capacitances of the array capacitors, the input parasitic capacitor of the comparator and the parasitic capacitors due to routing metals. On the other hand, there is a parasitic capacitor at the bottom plate of each capacitor, denoted by $\mathrm{C_{p,i}}$ which consists the bottom-plate parasitic capacitance of the main capacitor, the switch and routing parasitic capacitances. In Fig. 2(b) (i.e., BWA) there is another parasitic capacitance at node x denoted by $\mathrm{C_{p,x}}$ consisting of the top-plate capacitors of the capacitor array, the parasitic routing capacitances and the top-plate parasitic capacitance of the attenuation capacitor.

In order to include the effect of $\mathrm{C_{p,out}}$ in the power consumption in the CBW structure, we only have to replace (5) with the following equation

$$V_{\mathrm{DAC}_i} = \frac{C_i + \sum_{j=1}^{i-1} C_j D_j}{C_{\mathrm{total}} + C_{p,\mathrm{out}}} V_{\mathrm{ref}}. \tag{25}$$

By a process similar to what has been done in Sub-section A, the overall power consumed when $\mathrm{C_{p,out}}$ exists can be calculated. Subtracting the result from (9), the contribution of $\mathrm{C_{p,out}}$ to the power consumption becomes

$$\begin{aligned} &P_{\mathrm{Parasitic1}} \\ &\quad \approx \frac{2^N f_{\mathrm{clk}} C_0}{N+1}(\varepsilon) \times \left\{ \left(\frac{1}{6} + \frac{1}{3}\left(\frac{1}{2}\right)^{2N} \right) V_{\mathrm{ref}}^2 \right. \\ &\qquad \left. + \frac{1}{2} V_{\mathrm{in}}^2 + \left(\frac{1}{2}\right)^N V_{\mathrm{in}} V_{\mathrm{ref}} \right\} \end{aligned} \tag{26}$$

where $\varepsilon = \mathrm{C_{p,out}}/\mathrm{C_{total}}$.

In order to consider the power consumed by $\mathrm{C_{p,1}}$ to $\mathrm{C_{p,N}}$, in this structure, it should be noted that all switches related to the bottom-plate nodes of the capacitors will be turned on only once during the conversion phase. Thus, the power consumption due to these parasitic capacitances can be calculated from

$$P_{\mathrm{Parasitic2}} \approx \frac{f_{\mathrm{clk}} V_{\mathrm{ref}}^2}{N+1}(C_{p,1} + C_{p,2} + \cdots + C_{P,N}) \tag{27}$$

Since $\mathrm{C_{p,out}}$ is usually much smaller than $\mathrm{C_{total}}$, the excess power consumption due to $\mathrm{C_{p,out}}$ can be neglected. Therefore, the additional power consumption due to parasitic capacitances is dominated by bottom-plate capacitors (i.e., $\mathrm{C_{p,1}}$-$\mathrm{C_{p,N}}$) and obtained from

$$P_{\mathrm{Parasitic}} = P_{\mathrm{parasitic1}} + P_{\mathrm{parasitic2}} \approx \frac{f_{\mathrm{clk}} V_{\mathrm{ref}}^2}{N+1} 2^N \beta C_0 \tag{28}$$

where β is the ratio of the bottom-plate parasitic capacitance to the main capacitance of each capacitor. By similar deduction, it can be shown that the power consumption overhead due to

$C_{p,out}$ and $C_{p,x}$ in the other two structures (Fig. 2(b) and (c)) is not considerable. Thus, the power consumed by the parasitic capacitors in the capacitive array with attenuation capacitor can be calculated from (27). For the SBW structure, all switches related to the MSB sub-array capacitors (i.e., $C_{p1,2}$ to $C_{p1,N}$) will be turned on at the beginning of the conversion phase and remain on or change back to off according to the mentioned algorithm. Thus, all parasitic capacitances related to these nodes will be charged during the conversion phase only once. But the switches related to the main sub-array capacitors ($C_{p,2}$ to $C_{p,N}$) may become turned on or remain off according to the algorithm. Hence, the power consumed by parasitic capacitances in this structure can be calculated as

$$P_{\text{Parasitic}} \approx \frac{f_{\text{clk}} V_{\text{ref}}^2}{N+1} \times \left(C_{p1,0} + \sum_{i=2}^{N} C_{p1,i} + \sum_{i=2}^{N} C_{p,i} D_{i-1} \right). \quad (29)$$

In summary, it can be concluded (as confirmed by simulations) that the contribution of the parasitic capacitors at moderate speed (with small switches) in the entire power consumption of the capacitive DACs will not be considerable for small values of β (e.g., if $\beta < 5\%$, then the excess power consumed due to the parasitic capacitances would be less than 7%).

III. Static Linearity Behavior of the SA-ADCs

According to the presented equations in Section II, the power consumption of capacitive-array DACs is directly proportional to the size of the unit capacitor (C_0) in the capacitive array. In practice, the smallest possible value for C_0 is determined either by the kT/C noise requirement, the required capacitor matching, parasitic capacitance or design rules of the technology. The matching properties of the capacitors as well as the parasitic capacitances which affect the linearity characteristics of the converter such as INL and DNL are dominant factors for medium-resolution ADCs. Therefore, in this section, first a comparative analysis of the linearity of an SA-ADC employing the mentioned DACs due to capacitor mismatch will be presented and the standard deviation of the INL and DNL will be calculated. Then, the effect of parasitic capacitances on the linearity behavior of the structures will be discussed.

A. INL/DNL Performance of the ADC

In order to analyze the statistical behavior of the linearity metrics (INL and DNL) of the SA-ADC employing capacitive-array DAC structures, each of the capacitors is modeled as the sum of the nominal capacitance value and an error term [16], [25]. Therefore, for the CBW architecture, each capacitor is obtained from

$$C_i = 2^{N-i} C_0 + \delta_i, \quad \sigma_i^2 = E\left[\delta_i^2\right] = 2^{N-i}\sigma_0^2 \quad (30)$$

where C_0 is the unit capacitance, δ_i is a random variable with a zero mean and a variance of σ_i^2 and σ_0 is the standard deviation of the unit capacitance.

Now, the variance of the INL and DNL of SA-ADC with the CBW and SBW capacitive DAC neglecting the gain error can be calculated from [16]

$$\begin{aligned} \sigma_{\text{INL,CBW}}^2 &\approx 2^N \left(\frac{\sigma_0}{C_0}\right)^2 \left(\frac{V_{\text{in}}}{V_{\text{ref}}}\right) \text{LSB}^2 \\ \sigma_{\text{DNL,CBW}}^2 &\approx 2^N \left(\frac{\sigma_0}{C_0}\right)^2 \text{LSB}^2 \\ \sigma_{\text{INL,SBW}}^2 &\approx 2^N \left(\frac{\sigma_0}{C_0}\right)^2 \left(\frac{V_{\text{in}}}{V_{\text{ref}}}\right) \text{LSB}^2 \\ \sigma_{\text{DNL,SBW}}^2 &\approx \frac{2^N}{2} \left(\frac{\sigma_0}{C_0}\right)^2 \text{LSB}^2. \end{aligned} \quad (31)$$

Using the above method and utilizing (15), one can show that for the SA-ADC with BWA capacitive DAC, the variance of the INL and DNL can be calculated from

$$\begin{aligned} \sigma_{\text{INL,BWA}}^2 &\approx \left(\frac{\sigma_0}{C_0}\right)^2 \frac{V_{\text{ref}}^2}{2^{\frac{N}{2}}} \left\{ \sum_{i=1}^{\frac{N}{2}} \frac{D_i}{2^i} + \frac{1}{2^{\frac{N}{2}}} \sum_{i=1}^{\frac{N}{2}} \frac{D_{\frac{N}{2}+i}}{2^i} \right\} \\ &= 2^{\frac{3N}{2}} \left(\frac{\sigma_0}{C_0}\right)^2 \left(\frac{V_{\text{in}}}{V_{\text{ref}}}\right) \text{LSB}^2 \\ \sigma_{\text{DNL,BWA}}^2 &\approx \left(\frac{2^{N/2-1}\sigma_0^2 + \sum_{i=1}^{N/2} 2^{N/2-i}\sigma_0^2}{2^N C_0^2} + \frac{\sum_{i=2}^{N/2} 2^{N/2-i}\sigma_0^2}{2^N C_0^2} \times \frac{1}{2^{N/2}} \right) V_{\text{ref}} \\ &= 2^{\frac{3N}{2}} \left(\frac{\sigma_0}{C_0}\right)^2 \text{LSB}^2 \end{aligned} \quad (32)$$

It must be noted that in the BWA structure, it has been assumed that $k = m = N/2$ and also C_A and $C_A || (\sum_{i=1}^{N/2} C_i)$ are both approximated by C_0.

To summarize, it can be concluded that the CBW and SBW structures have the same standard deviation of INL (denoted by σ_{INL}) and $2^{N/4}$ times smaller than that of the BWA structure. On the other side, the standard deviation of DNL (denoted by σ_{DNL}) for the SBW array is smaller by a factor of $\sqrt{2}$ in comparison with the CBW structure. However, σ_{DNL} for the BWA architecture is $2^{N/4}$ times larger than that of the CBW structure. This fact that is usually overlooked by circuit designers is due to the reduced size of the capacitors in this structure.

B. The Effect of Parasitic Capacitances on the Linearity Characteristics

In order to investigate the effect of the parasitic capacitances on the linearity characteristics of the capacitive-array DACs, we assume that there is no mismatch between the main capacitors

but the parasitic capacitors exist. It should be noted that the parasitic capacitances related to the bottom-plate node of the capacitors do not affect the linearity behavior of the ADC. This is true due to the fact that the bottom plates of the main capacitors are connected to either $\mathrm{V_{ref}}$ or $\mathrm{V_{ss}}$ and do not affect the charge distribution of the main capacitors. On the other hand, other parasitic capacitances related to the top-plate node of the capacitors ($\mathrm{C_{p,out}}$ and $\mathrm{C_{p,x}}$) can affect the linearity characteristics of the converter.

For the CBW structure, including the effect of the parasitic capacitors, the analog output voltage of the DAC ($\mathrm{V_{DAC}}$) corresponding to the given digital input word of the DAC (i.e., X), is obtained from

$$V_{\mathrm{DAC}}(X) = \frac{\sum_{i=1}^{N} C_i D_i}{C_{p,\mathrm{out}} + C_0 + \sum_{i=1}^{N} C_i} V_{\mathrm{ref}} = \left(\frac{1}{1+\varepsilon_1}\right) \sum_{i=1}^{N} \frac{D_i}{2^i} V_{\mathrm{ref}}. \quad (33)$$

Similarly, for the BWA structure (and the case where $\mathrm{k} = \mathrm{m} = \mathrm{N}/2$), the output voltage of the DAC is obtained from

$$V_{\mathrm{DAC}}(X) = \left(\frac{1}{1+\varepsilon_{21}}\right) \sum_{i=1}^{N/2} \frac{D_i}{2^i} V_{\mathrm{ref}} + \left(\frac{1}{1+\varepsilon_{22}}\right) \sum_{i=N/2+1}^{N} \frac{D_i}{2^i} V_{\mathrm{ref}} \quad (34)$$

and for the SBW structure this voltage will become

$$V_{\mathrm{DAC}}(X) = \left(\frac{1}{1+\varepsilon_3}\right) \sum_{i=1}^{N} \frac{D_i}{2^i} V_{\mathrm{ref}}. \quad (35)$$

In (33), (34) and (35),

$$\varepsilon_1 = \varepsilon_3 = \frac{C_{p,\mathrm{out}}}{C_{\mathrm{total}}} = \frac{C_{p,\mathrm{out}}}{2^N C_0}$$
$$\varepsilon_{12} \simeq \frac{C_{p,\mathrm{out}}}{2^{N/2} C_0} + \frac{C_{p,x}}{2^N C_0}$$
$$\varepsilon_{22} \simeq \frac{C_{p,\mathrm{out}} + C_{p,x}}{2^{N/2} C_0} + \frac{C_{p,x} + C_{p,\mathrm{out}} + C_{p,x} C_{p,\mathrm{out}}}{2^N C_0} \quad (36)$$

According to the above equations it can be concluded that in both the CBW and SBW structures, if the values of the parasitic capacitances are assumed to be constant and independent of the DAC voltage, they will only cause a gain error without affecting the linearity performance. But in the BWA structure, the parasitic capacitors degrade the linearity performance of the converter, even if constant. This is true due the fact that the effect of the parasitic capacitances on the value of the DAC voltage is not constant for different input voltages, as estimated by (34). It should be noted in all three structures that since $\mathrm{C_{p,out}}$ consists of the input parasitic capacitance of the comparator which is dependent on its input voltage, it degrades the linearity performance of the converters.

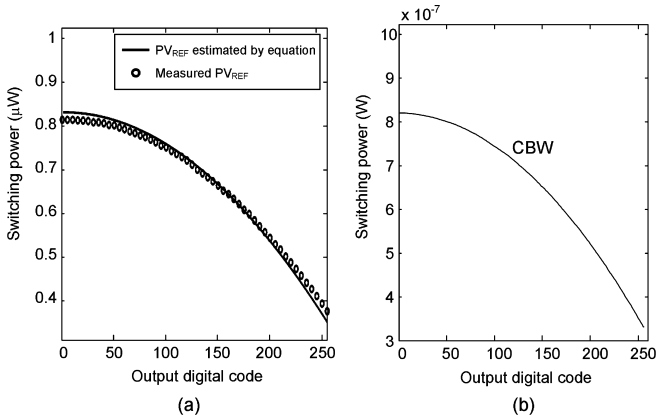

Fig. 4. Switching power consumption of the CBW structure; (a) calculation and measurement results reported in [10] (extracted from Fig. 13 in [10]) and (b) what predicted by (9) in this paper for an 8-bit ADC.

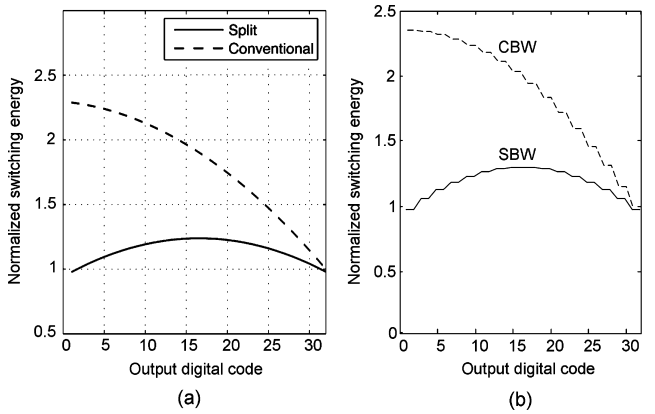

Fig. 5. Normalized switching energy consumptions of the CBW and SBW structures (a) reported in [16] (extracted from Fig. 8 in [16]) and (b) those predicted by the proposed equations in this paper (i.e., (9) and (22)).

IV. Simulation Results and Comparison Between the Structures

In order to verify the accuracy of the proposed equations, transistor-level simulations have been done. In this section, first measurement and simulation results of previously published works will be compared with the values obtained from the equations proposed in this work. Then, the results of the simulations performed to verify the accuracy of the proposed equations will be presented. Finally, different architectures are compared from power-consumption and linearity viewpoints.

A. Measurement and Simulation Results of Previously Published Works

In [10], the measured power consumption of a CBW structure has been shown versus the output code of the ADC. Fig. 4 compares the values predicted by our equations with those presented in [10] and the measurement results with very good agreement. Nevertheless, the equations proposed in this paper are more general than those presented in [10] for an 8-bit example.

Furthermore, simulation results presented in [16], [18], [19] and [24] have been compared with the results predicted by the equations proposed in this paper in Figs. 5, 6, 7 and 8, respectively. Very good agreement can be observed in all cases.

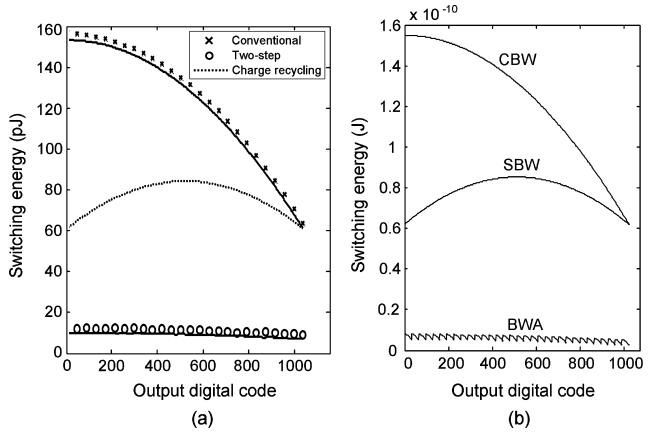

Fig. 6. Switching energy consumptions of the CBW, SBW and BWA structures (a) reported in [18] (extracted from Fig. 5 in [18]), and (b) those predicted by the proposed equations in this paper (i.e., (9), (16) and (22)). Note that the two-step architecture presented in [18] is not exactly the same as the BWA architecture but the other two are exactly the same.

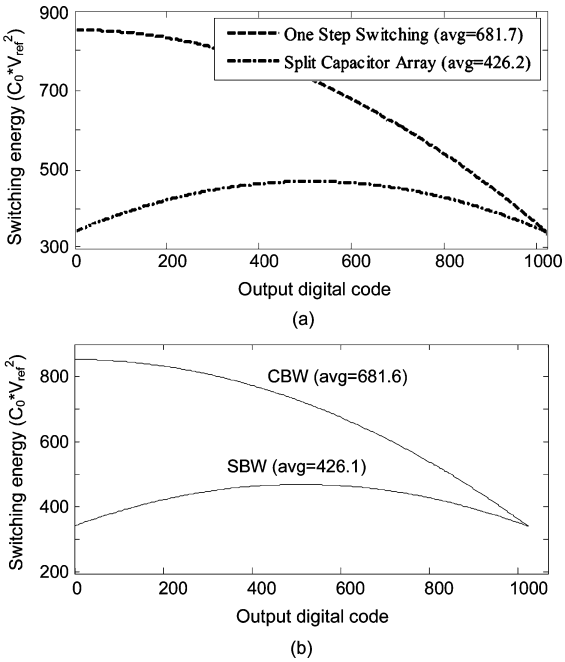

Fig. 7. Switching energy consumption of the CBW and SBW structures normalized to $C_0V_{ref}^2$ (a) reported in [19] (extracted from Fig. 4 in [19]) and (b) what predicted by the proposed equations in this paper (i.e., (9) and (22)).

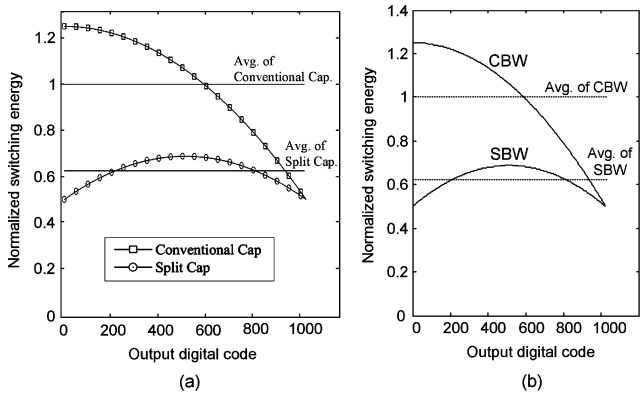

Fig. 8. Switching energy consumption of the CBW and SBW structures normalized to the average energy consumption of the CBW structure (a) reported in [24] (extracted from Fig. 8 in [24]) and (b) what predicted by the proposed equations in this paper (i.e., (9) and (22)).

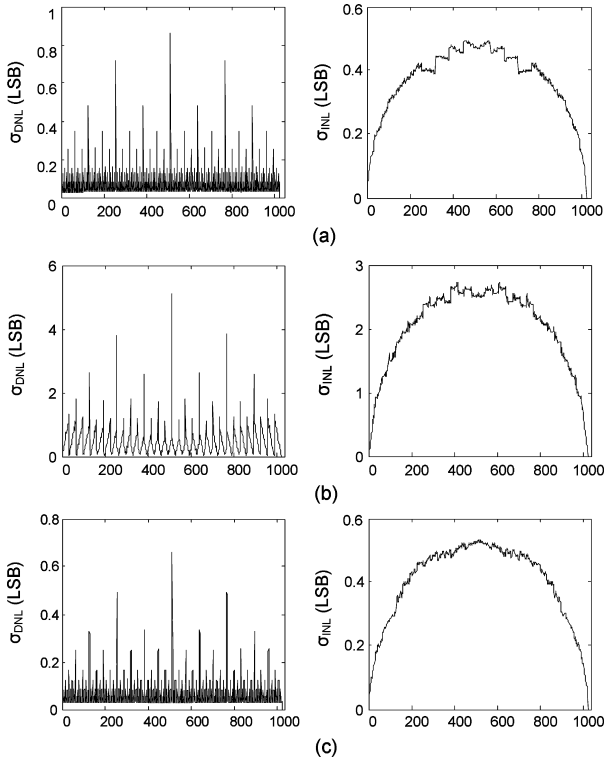

Fig. 9. Simulation results for linearity of an SA-ADC employing (a) a CBW structure, (b) a BWA structure, (c) a SBW array DAC. 300 Monte Carlo runs were performed with independent identically-distributed Gaussian errors in the unit capacitors ($\sigma_0/C_0 = 3\%$). The standard deviation of the DNL and INL are plotted.

B. Simulation Results

We have also designed and simulated the above-mentioned architectures (i.e., the CBW, BWA and SBW architectures) using a 0.18-μm CMOS technology with a metal-insulator-metal- (MIM-) capacitor option. For all cases, a 1-V, 10-bit, 10 kS/s SA-ADC with $C_0 = 50$ fF has been simulated.

Fig. 9 shows the results of 300 Monte Carlo simulation runs where the standard deviation of INL and DNL are depicted versus the output digital code of the SA-ADC for the three mentioned structures. In all cases, the value of the unit capacitors is taken to be independent identically-distributed Gaussian random variables with a standard deviation of 3% (i.e., $(\sigma_0/C_0) = 0.03$). A very good agreement between the maximum values of the σ_{INL} and σ_{DNL} for all three structures and those predicted by (31) and (32) can be observed.

In order to be able to compare the structures from a power consumption viewpoint, one should note that the power consumption is directly proportional to the value of the unit capacitor. Assuming identical values for the unit capacitor in the three structures, simulated values of the power drawn from the reference supply voltage (i.e., P_{Vref}) versus the digital output codes of the ADC are compared with the values predicted by the equations presented in this paper (i.e., (9), (16) and (22))

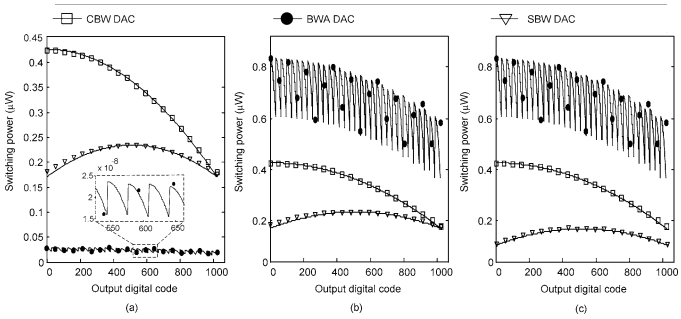

Fig. 10. Estimated values of the power consumption of the DAC ($\mathrm{P_{Vref}}$) in a 10-bit SA-ADC based on the proposed equations (solid lines) and the circuit-level simulation results (signs); (a) with similar unit capacitors, (b) with similar INL behavior, and (c) with similar DNL behavior for all structures.

in Fig. 10(a). A very good agreement can be observed. As expected, assuming similar unit capacitors, the power consumption of the BWA structure is the least.

On the other hand, in many applications, the value of the unit capacitor is determined by the required value for σ_{INL} and/or σ_{DNL}. In such cases, one should note that if the capacitor mismatch is dominated by oxide variation, it can be written as [40]

$$\frac{\sigma_0}{C_0} = \frac{\alpha_0}{\sqrt{C_0}} \tag{37}$$

where α_0 is a technology-dependent coefficient. Therefore, according to (31) and (32), it can be concluded that for similar values of σ_{INL}, the unit capacitor of the BWA structure should be chosen $2^{\mathrm{N}/2}$ times larger than its counterparts in the CBW and SBW structures. Similarly, for identical values of σ_{DNL}, the unit capacitor of the BWA structure should be chosen $2^{\mathrm{N}/2}$ times larger than that of the CBW structure and the unit capacitor of the SBW structure is half of that in the CBW architecture. Simulated values of $\mathrm{P_{Vref}}$ are compared once assuming a similar standard deviation of the INL for the structures in Fig. 10(b) and then with a similar standard deviation of the DNL in Fig. 10(c). A very good agreement can be observed between the simulation results and those predicted by the proposed equations. It should be noted that in the design of the BWA, the number of LSBs and MSBs has been taken equal to $\mathrm{k} = \mathrm{m} = \mathrm{N}/2$. This is because the capacitor switching power consumption would be minimal for this case. This can be observed in Fig. 11 where the power consumption of the BWA structure is shown versus the digital output codes for different values of k and m.

For a better comparison between the structures, based on (9), (16) and (22), it can be shown that the average power consumption of the capacitive array for an input signal with a uniform probability for all codes, can be estimated from

$$P_{\mathrm{avg,CBW}} \approx K_1 2^N \left(\frac{f_{\mathrm{clk}} C_0 V_{\mathrm{ref}}^2}{N+1}\right) \tag{38}$$

$$P_{\mathrm{avg,BWA}} \approx K_2 2^{\frac{N}{2}} \left(\frac{f_{\mathrm{clk}} C_0 V_{\mathrm{ref}}^2}{N+1}\right) \tag{39}$$

$$P_{\mathrm{avg,SBW}} \approx K_3 2^N \left(\frac{f_{\mathrm{clk}} C_0 V_{\mathrm{ref}}^2}{N+1}\right) \tag{40}$$

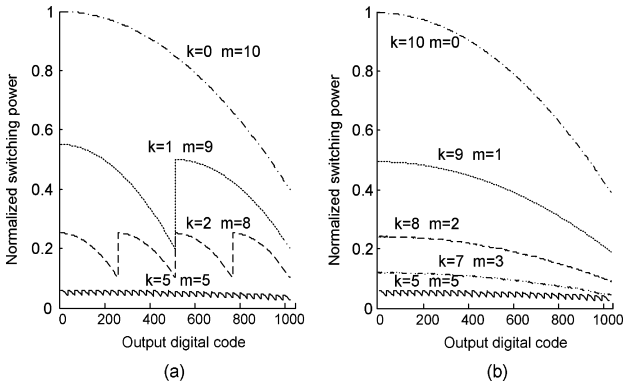

Fig. 11. Normalized switching power consumption of the BWA DAC versus output digital code for various distributions of k and m values for a 10-bit SA-ADC estimated by (16) (k and m are the number of MSBs and LSBs respectively): (a) $\mathrm{k} \leq \mathrm{m}$, (b) $\mathrm{k} \geq \mathrm{m}$.

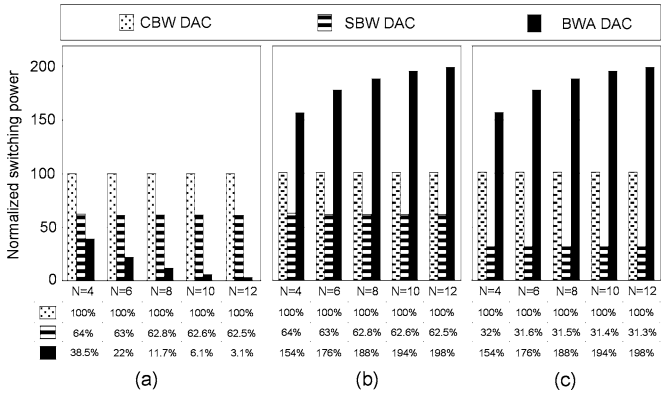

Fig. 12. Comparison of the normalized switching power consumption of the capacitive-array DACs in different architectures for different resolutions, (a) with identical unit capacitors, (b) with similar INL performance, and (c) with similar DNL performance.

where $\mathrm{K_1} = 0.66$, $\mathrm{K_3} = 0.41$ and $\mathrm{K_2}$ depending on the converter resolution varies between 1.1 to 1.3. In the following comparisons, $\mathrm{K_2}$ has been assumed equal to 1.25.

Fig. 12 depicts the values of the power consumption for a full-scale sinusoidal input signal normalized to the power consumption of the CBW structure for different converter resolutions once with identical unit capacitors (in Fig. 12(a)), then with a similar σ_{INL} (in Fig. 12(b)) and finally with similar σ_{DNL} (in Fig. 12(c)). It can be observed that if the size of the unit capacitor is dictated by capacitor mismatch for similar INL and DNL, the switching power consumption of the SBW structure is the least.

The effect of the parasitic capacitances on the capacitor switching power consumption of the ADC is shown in Fig. 13 for different values of β (i.e., the ratio of the bottom-plate parasitic capacitance to the main capacitance of each capacitor). In Figs. 13(a), 10(a) has been redrawn including the effect of parasitic capacitances. In Fig. 13(b), the simulated and calculated values of the excess power consumed due to the bottom-plate parasitic capacitances are compared versus the value of β for the CBW structure. A very good agreement can be observed

TABLE I
COMPARISON OF THE CAPACITIVE-ARRAY DACS

	Average power (W)	Standard deviation of INL (LSB)	Standard deviation of DNL (LSB)	Total required capacitance
CBW	$0.66\times 2^N\left(\frac{f_{clk}C_0V_{ref}^2}{N+1}\right)$	$2^{\frac{N}{2}-1}\left(\frac{\sigma_0}{C_0}\right)$	$2^{\frac{N}{2}}\left(\frac{\sigma_0}{C_0}\right)$	$2^N C_0$
BWA	$\approx 1.25\times 2^{\frac{N}{2}}\left(\frac{f_{clk}C_0V_{ref}^2}{N+1}\right)$	$2^{\frac{3N}{4}-1}\left(\frac{\sigma_0}{C_0}\right)$	$2^{\frac{3N}{4}}\left(\frac{\sigma_0}{C_0}\right)$	$2\times 2^{\frac{N}{2}} C_0$
SBW	$0.41\times 2^N\left(\frac{f_{clk}C_0V_{ref}^2}{N+1}\right)$	$2^{\frac{N}{2}-1}\left(\frac{\sigma_0}{C_0}\right)$	$\frac{2^{\frac{N}{2}}}{\sqrt{2}}\left(\frac{\sigma_0}{C_0}\right)$	$2^N C_0$

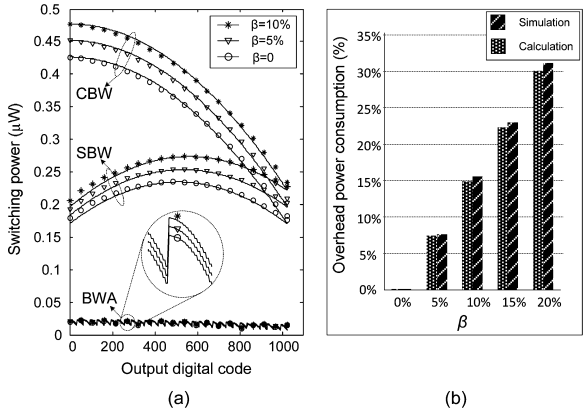

Fig. 13. Effect of the parasitic capacitances on the switching power consumption in a 10-bit SA-ADC (a) Estimated values of P_{Vref} including the effect of parasitic capacitances based on the proposed equations (solid lines) and the circuit-level simulation results (signs) for different values of β; (b) Extra power consumption due to the parasitic capacitances for different values of β in the CBW structure.

between the simulation results and those estimated by (28) and (29), too.

C. Comparison Between the Structures

In order to have a better comparison between the structures, the value of the average power consumption, maximum standard deviations of the INL and DNL, and the total required capacitance of the each structure are summarized in Table I. It is clear that with similar values for the sampling frequency, resolution, reference voltage and specifically the size of the unit capacitor, the average reference power consumption (P_{avg}) of the BWA array is around $(190\times 2^{-N/2})\%$ of the CBW structure and that of the SBW array is around 62% of the CBW structure. But the standard deviation of INL for the BWA structure is $2^{N/4}$ times larger than that of both the CBW and SBW structures. As for the standard deviation of the DNL, the performance of the CBW and the SBW structures are $2^{N/4}$ and $\sqrt{2}\times 2^{N/4}$ times smaller than that of the BWA structure, respectively. Thus, in order to have similar INL characteristics in these three structures with the same sampling frequency, resolution and reference voltage, the average power consumption of the BWA array and the SBW array is around 190% and 62% of that of the CBW structure, respectively. Similarly, it can be concluded that for identical DNL performances, the average power consumption of the BWA array and the SBW array is around 190% and 31% of that of the CBW structure, respectively. Comparison of the chip areas of the structures for similar values of the σ_{INL} is also instructive. For the BWA structure, since the size of each capacitor should be increased by a factor of $2^{N/2}$ compared to the CBW structure, the area occupied by the capacitors will be almost twice (i.e., $2\times 2^{N/2}\times 2^{N/2}C_0$). On the other hand, the SBW capacitors occupy almost the same area. However, for identical values of σ_{DNL}, the total capacitance of the BWA and the SBW DACs is twice and half of the CBW structure, respectively. While the logic circuit is exactly the same for CBW and BWA ADCs, the SBW ADC suffers from a power and area overhead for more complexity of the digital circuit.

As discussed in Section III, the linearity performance of the BWA structure is degraded by the parasitic capacitances; while in the CBW and SBW structures the linearity is affected mainly by the non-linearity behavior of the input parasitic capacitance of the comparator. Obviously, even for the binary-weighted SA-ADCs, the structures of the capacitive DACs are not limited to the main three already discussed in this paper. For instance, a C-2C structure has been employed in [20]–[23] and an SA-ADC with dual capacitive-array DAC in [18], [19]. Deducing from what has been developed for the BWA structure, it can be shown that the total capacitance of the capacitive array and the power consumption due to capacitor switching in the C-2C architecture increase linearly with the resolution in the number of bits. However, this structure severely suffers from parasitic capacitances [20], [23] and even worse from capacitor mismatch. It can be shown that the capacitor switching power consumption and the linearity behavior of the SA-ADC with a dual capacitive array is almost the same as of the BWA structure.

V. CONCLUSION

The power consumed by switching the capacitors of a capacitive-array DAC employed in successive-approximation ADCs and its linearity behavior have been analyzed and verified by simulations for three commonly-used architectures i.e., the CBW, BWA and SBW structures. The proposed equations provide closed-form relations between the power consumption of the DAC as well as its INL and DNL metrics versus the size of the unit capacitor, the converter resolution, the clock frequency and the reference voltage. The effect of the parasitic

capacitances on the power consumption and the linearity of the converters has also been analyzed. The presented equations can be used not only in choosing the best architecture for the capacitive-array DAC and optimizing the chosen architecture but also in estimating the power consumption of the DAC in both hand calculations and computer-aided-design tools. It has been shown that for identical DNL performances, the capacitor switching power consumption of the SBW structure is almost 1/3 of the CBW structure and 1/6 of the BWA structure. Furthermore, in spite of what commonly assumed, the switching power consumption as well as the total capacitance of the BWA structure is larger than that of the CBW structure if similar INL/DNL performances are required. It has also been demonstrated that the capacitor switching power consumption of the structures with and without explicit S/H circuits is the same.

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