Analysis of Process-Geometry Modulations Through 3D TCAD

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Abstract

In this work we present a study of the combined effects of the variation of process parameters and geometry in a 65 nm technology through consistent three-dimensional TCAD process and device simulations. Channel lengths and widths together with two critical process parameters obtained through a screening experiment are examined in a 3-level full-factorial design of experiments. The results show an increased impact of process variations for short and narrow structures.

1   Introduction

For the 65 nm technology node and beyond, process tolerances increasingly impact the final device characteristics and therefore the final circuit yield, leading to additional manufacturability problems. The use of TCAD to analyze and quantify process variations is well established in the industry. The common approach is to use two-dimensional simulations to avoid the problems of complexity, cost, and accuracy that arise with three-dimensional simulations [1, 2] . However, modern VLSI circuits use transistors that have not only a short channel, but are also narrow. Three-dimensional effects due to the presence of shallow trench isolation (STI) in the third dimension [3, 4] are no more negligible in the determination of device behavior; they need to be properly addressed. The interaction of process variability with the topographical features of a MOS transistor is non trivial, and is the scope of this work.

2   Device creation and simulation setup

Process simulation is performed with a highly realistic transistor shape (Figure 1). Three different gate lengths and channel widths are investigated, while the features of the STI are kept constant. The influence of the divot over-etch on the electrical characteristics of a device is already well known [3], therefore we focus on parametric process variability. The shallow trench used for isolation in this 65 nm process is 0.3 μm deep with a 6 nm divot. The silicon corner radius is 4 nm. In order to save computational time and gain accuracy, the process simulation up to gate stack formation is performed in two dimensions on a cut along the width direction, and subsequently extruded and reinterpolated on the 3D structure. This approximation is permissible as long as the influence of the STI on the source/drain side is not considered.
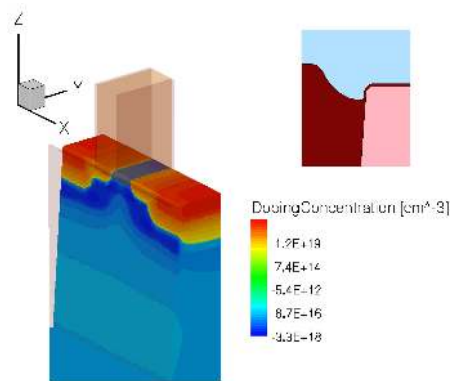
Figure 1: Final device after process simulation. In the inset, particular of the 6 nm deep oxide over-etch in the device corner.
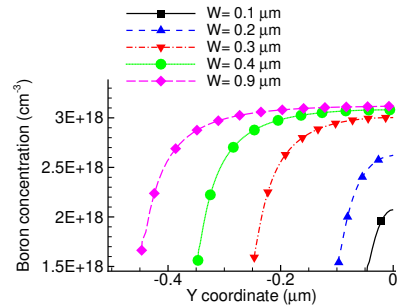

Figure 2: Boron concentration 1 $\mathring{A}$ under the gate, along the width of the device. The 3D effect increases for narrow devices.

Three-dimensional process simulation is used from polysilicon deposition to the end of the process. In particular, 3D analytical implantation is performed using calibrated dual-Pearson functions. For the dopant diffusion, a three-stream model has been adopted, and interstitial clustering is also taken into account in order to properly reproduce transient enhanced diffusion (TED). Segregation of dopant into the oxide and release from it are included through the use of the three-phase segregation model [5]. The large Si/SiO$_2$ interface of the shallow trench isolation strongly affects the doping concentration in the channel of the device for narrow structures because of TED. There is a strong difference in the surface concentration of devices with different widths as can be seen from Figure 2. Note that in our simulation the doping concentration in the center of the channel approaches that from standard two-dimensional simulations only for devices wider than 0.9 μm. For wide devices, an excellent agreement with 2D calibrated boron profiles is obtained as reported in Figure 3. The depletion of boron on the surface is partially compensated by a slightly higher doping in the depth direction for small widths, therefore there are no dramatic variations of threshold voltage due to 3D process effects. Two process parameters have been selected through a screening experiment as the ones having the highest impact on device characteristics: halo tilt angle and halo dose. A three-level full factorial design of experiment (DOE) has been then performed on the main transistor dimensions (L: 65, 130, 250 nm, W: 0.1, 0.2, 0.5 μm) and on these process variations (Halo tilt: 30° ±5°, Halo dose: 4.9e13 ±0.3e13 cm^{-2}).

In device simulation, Poisson and drift-diffusion equations are solved. The modified local density approximation is used to account for quantum confinement of electrons in the channel [6]. Figure 4 shows the roll-off curves for three device widths, compared to the 2D counterpart. Stress effects are not included in the simulations in order to properly separate process effects from stress-derived ones.
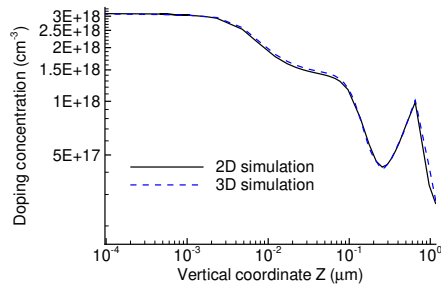
Figure 3: Vertical boron profile in the center of a 1.2 μm wide 3D device structure compared with the 2D device.
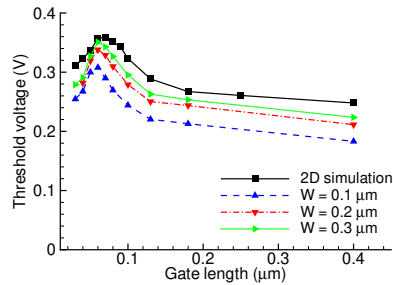

Figure 4: Roll-off curves for 3D structures of different widths compared to 2D roll-off curve.

3   Results and discussion

Figures 5 and 6 show the threshold voltage as a function of geometry and process variations. The surfaces represent different process conditions. Threshold voltage increases for small gate length due to the reverse short channel effect, while it decreases for small transistor widths due to the reverse narrow channel effect. A larger halo dose implies a higher threshold voltage and therefore lower saturation current. An increase in the halo implantation angle also leads to a higher threshold voltage, due to the larger pile up of boron in the center of the channel.

Although the dependency on the geometry of the transistors shows the same trends for different process conditions, it is interesting to highlight the impact on the different geometries. Threshold voltage variation due to a 6% halo dose variation is approximately 2.5% for wide structures (W=0.5 μm), while it is 4% for narrow ones. The impact of halo tilt variation ($\pm 5°$) is stronger, and we observe a 3% threshold voltage variation for wide structures and a much larger 7% variation for narrow ones. A similar increased sensitivity is observed for currents (Figures 7, 8). These variations are not dramatic
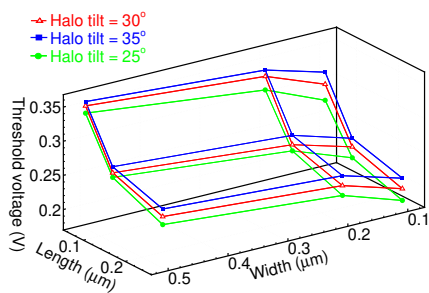

Figure 5: Dependence of threshold voltage on halo tilt variations for the different geometries. Halo dose is 4.9e13 cm^{-2} for all the structures.
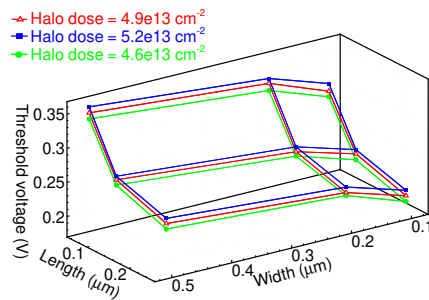

Figure 6: Dependence of threshold voltage on halo dose variations for the different geometries. Halo tilt is 30° for all the structures.
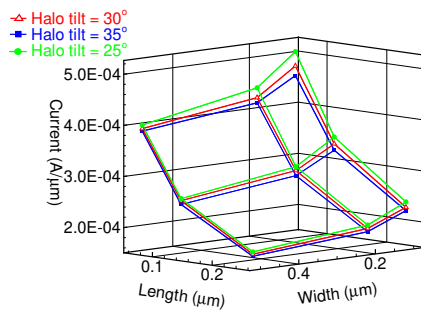
Figure 7: Dependence of saturation current on halo tilt variations for the different geometries. Halo dose is 4.9e13 cm^{-2} for all the structures.
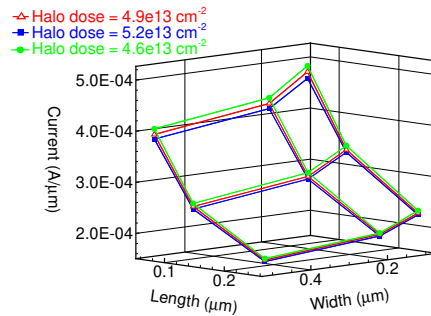
Figure 8: Dependence of saturation current on halo dose variations for the different geometries. Halo tilt is 30° for all the structures.

in absolute value, but they clearly show how the dimensions of a device influence the effects of process variations.

4   Conclusions

We have studied the interaction of process variability with the geometry of a device through 3D TCAD simulations. A careful simulation setup and meshing strategy allow to achieve consistent quantitative results across all 3D simulations. An excellent agreement with 2D calibrated simulations is achieved for large devices.

Results of a 3-level full-factorial DOE on two process variables and different transistor dimensions show a considerably higher impact of process variations for short and narrow devices, as they are typical in the latest technologies. Therefore a study of parametric variability effects performed with standard two-dimensional simulation approach can underestimate the impact of process variability on narrow structures.

References

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