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Analysis of proton irradiated n- and p-type strained FinFETs at low temperatures down to 100 K

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Abstract

This paper studies the main low temperature electrical parameters of SOI n- and p-type FinFETs, standard and strained devices, submitted to proton irradiation. The study covers the range from room temperature down to 100 K, focusing on the threshold voltage (V_{TH}), subthreshold swing (SS), the Early voltage V_{EA}, transistor efficiency and the intrinsic gain voltage (A_V) for 3 different channel widths. The p-channel devices showed a greater immunity to radiation than the n-channel ones, when considering the basic parameters thanks to the back conduction turn-off tendency, while from the analog parameters point of view, both transistor types presented a similar response to proton radiation at strong inversion.

Keywords: strained devices, proton radiation, low temperature, FinFETs

(Some figures may appear in colour only in the online journal)

1. Introduction

Silicon-on-insulator (SOI) technology has shown an improved performance in special applications that may involve harsh environments such as radiation and high temperatures. The presence of a buried oxide beneath the thin silicon active region allows for a higher tolerance to transient radiation effects, mainly for fully depleted SOI devices, which have better electrostatic coupling than bulk devices [1]. However, the buried oxide is usually thick and makes the device more susceptible to total ionization dose (TID) effects, mainly due to positive charge buildup [2]. The radiation effects in MOS oxides was extensively studied and it is reported in [3].

In the challenge of device downscaling, SOI is also a prominent technology. To overcome short-channel effects and other parasitics that may arise from reducing the physical size, the semiconductor industry has developed new techniques, i.e., strain engineering, high-κ dielectrics and novel architectures, such as non-planar (three-dimensional -3D) and multiple gate structures.

A vertical triple gate transistor (FinFET) is one of the candidates for commercial and special applications where fitting these scaling requirements are necessary. Its structure aims for the improvement of electrostatic coupling and better control of short-channel effects (SCE) than traditional planar devices. By using narrow-fin devices a high radiation tolerance can be achieved [4].

Considering that the effects of low temperature on strained FinFET devices are not fully explored yet, and also that there are some applications where transistors are submitted to radiation, such as for aerospace and medical equipment, this work aims to evaluate the low temperature impact on the main electrical parameters of strained FinFETs submitted to proton radiation.

2. Device characteristics

The triple gate SOI FinFETs analyzed in this work were fabricated at imec, Belgium, on SOI substrates with a 150 nm

thick SiO_2 layer (BOX). The gate dielectric is composed by a 2 nm HfSiON layer over a 1 nm SiO_2 interfacial layer, resulting in a 1.5 nm equivalent oxide thickness (EOT). The midgap gate is composed of 10 nm of TiN capped by 100 nm of poly-silicon. All devices have a fin height of 65 nm and the source and drain series resistance were reduced by selective epitaxial regrowth. A schematic lay-out of the studied FinFETs is shown in figure 1.

In this work, two different channel lengths (L_G), 150 nm and 900 nm have been considered and three different fin widths (W_{Fin}), 20 nm, 120 nm and 370 nm. More process details can be found in [5].

Additionally two different splits were analyzed: an unstrained split that was taken as a reference and a strained one. In the last case, the strained split combines biaxial (sSOI substrates) and uniaxial stress (dual contact etch stop layer—dCESL). The dCESL technique consists of a deposition of an SiN_x cap over the gate stack, which can result in a compressive or tensile strain in the channel, depending on the amount of hydrogen and some processing parameters [6]. Since both p and n-type devices are evaluated, the dCESL is appropriate because while compressive strain enhances the hole mobility, tensile strain benefits the electron mobility.

The devices were irradiated at the Cyclone facility in Louvain-la-Neuve (Belgium), using 60 MeV beam energy, with a fluence of 10^{12} p/cm^2 at room temperature. No bias was applied during irradiation and the contacts were kept floating.

3. Analysis and discussion

3.1. Basic parameters

Figure 2 shows the experimental threshold voltage (V_{TH}) for a temperature range from room temperature down to 100 K, for both n-type (figure A) and p-type transistors (figure B), before and after proton radiation and for 3 different channel widths (W_{Fin}).

Considering that for 3D devices, not only the channel length but the W/L ratio is important when the SCE are taken into account, for the widest studied transistor (W_{Fin} =370 nm) a long channel device was also evaluated, aiming to minimize the SCE and to better understand the proton irradiation influence on the FinFET behavior.

Both types of transistors (nMOS and pMOS) presented a V_{TH} absolute value increase as the temperature decreases. One can notice that this V_{TH} increase is almost linear with the temperature reduction and can be explained by the Fermi level potential shift towards the majority carrier band edge upon cooling. Another general evaluation is the comparison between strained and unstrained devices. Strained devices present smaller V_{TH} values compared with their counterparts, since the mechanical stress causes a valence and conduction band offset, resulting in a bandgap narrowing and, consequently, a V_{TH} reduction.

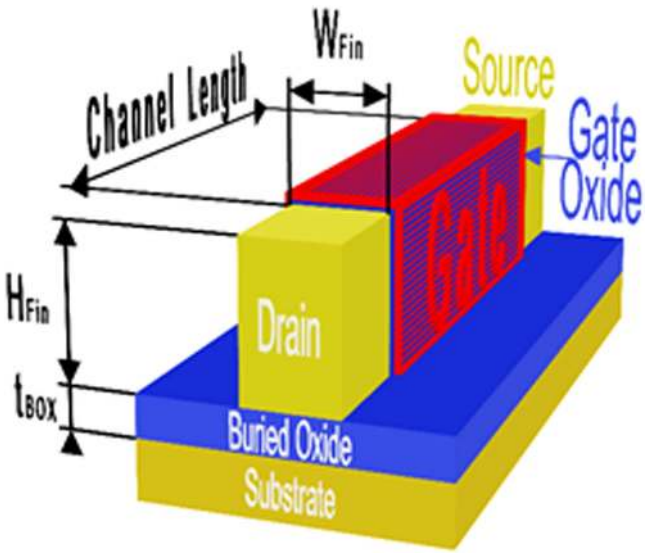

Figure 1. FinFET structure.

However, when the focus is on the proton radiation effects, it is possible to observe that it affects the n-type and p-type transistors in a different way. When nFinFETs were irradiated, positive charges build up in the oxides. Considering the thickness of the buried oxide, it causes a negative V_{TH} shift at the back interface resulting in a parasitic back conduction. It is equivalent to the application of a positive back-gate bias, inverting the back interface. On the other hand, for the pFinFETs, the effect of the radiation induced positive charges in the buried oxide on V_{TH} (negative shift) which turns off the back interface parasitic current, thus improving the device characteristic [7].

When the results were evaluated for low temperatures, the effectiveness of stress should be taken into account, because while for MOSFET technology the modulus of V_{TH} increases at low temperatures, the strain effectiveness also increases reducing the V_{TH} value. In addition, the higher the strain effectiveness, the higher the interface charges even before radiation. As a result, it is possible to observe that for strained devices the V_{TH} is slightly less affected by radiation as the temperature goes down.

The same V_{TH} trend was obtained for both channel lengths (150 nm and 900 nm) after radiation.

The same analysis was performed for the subthreshold swing (SS) as a function of temperature (figure 3). For both types of transistors (n and p) the devices with a narrow fin (W_{Fin} = 20 nm) showed to be tolerant to radiation, presenting almost no variation independent of the mechanical stress and temperature. Wider FinFETs however, are more affected by radiation since there is a lower electrostatic coupling between the sidewall gates and the back channel. As explained before, these buried charges created by the radiation cause a back conduction for n-channel devices and turns off this parasitic current for p-channel ones. This opposite behavior of the back conduction results in an

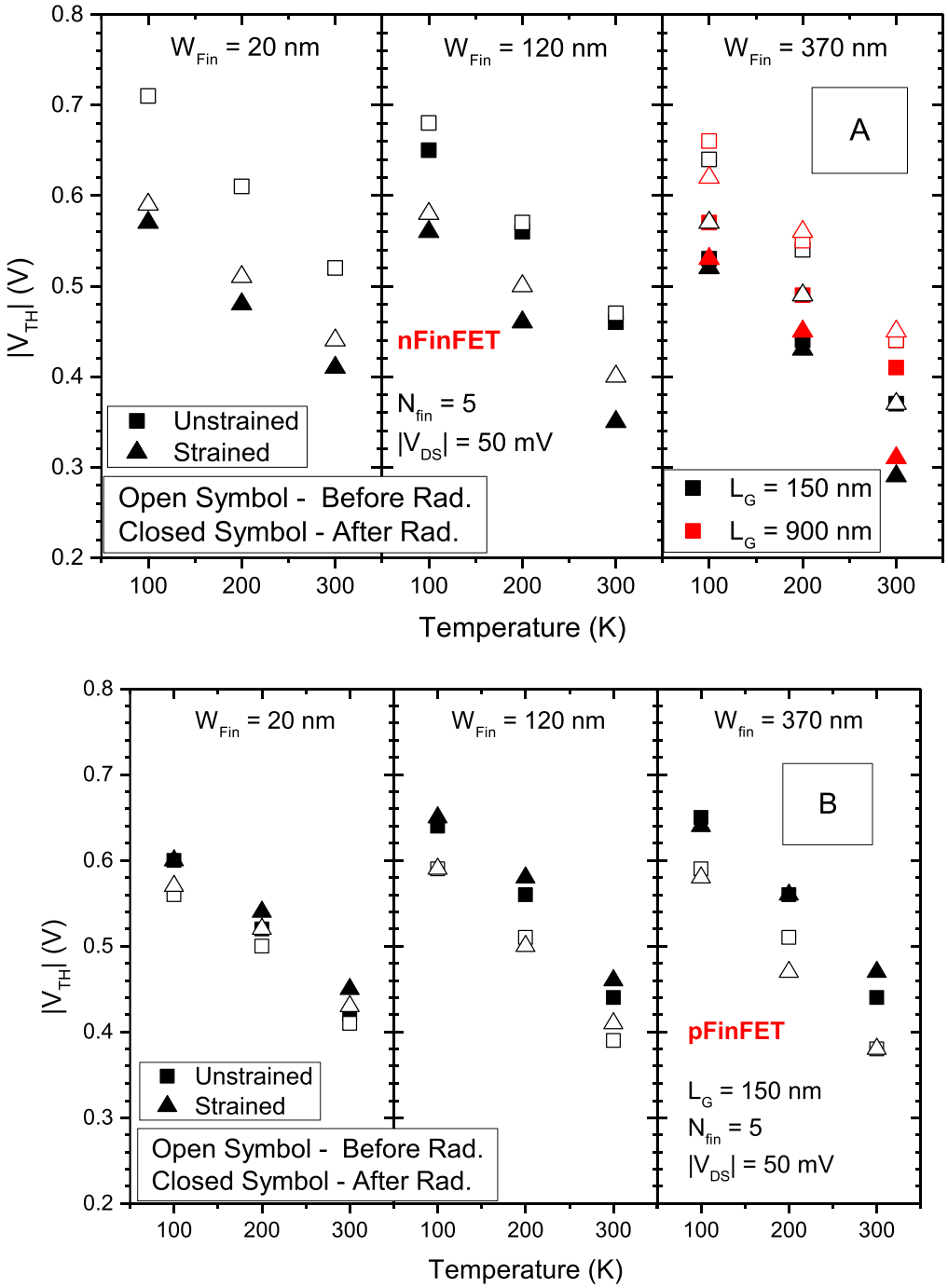

Figure 2. Experimental threshold voltage as a function of temperature for strained and unstrained devices, before and after radiation for nFinFETs (A) and pFinFETs (B). In case of nFinFET with $W_{Fin} = 370$ nm, two L_G values are analyzed.

opposite trend of SS comparing p and n transistors. While the radiation degrades the SS behavior for nFinFETs, it reduces the p-type transistor off current [7, 8].

Analyzing the temperature influence on SS for unstrained devices, the reduction of SS with temperature is almost linear as expected [9], but it is non-linear for both types of strained FinFETs. This is explained as follows: although the mechanical stress improves the ON current, it results in a high interface trap density (N_{it}) [10] that tends to degrade the SS values. Then, for strained devices both effects (N_{it} and V_{TH} variation) should be taken into account. Considering that at low temperatures the V_{TH} is less affected by irradiation and N_{it} has a higher impact on SS, a non-linear SS reduction with temperature was obtained for strained transistors.

For p-type devices, when the temperature goes down, the increase of V_{TH} results in a suppression of the back parasitic conduction. Since the radiation effects on V_{TH} follow the same trend, it is possible to conclude that the best behavior of

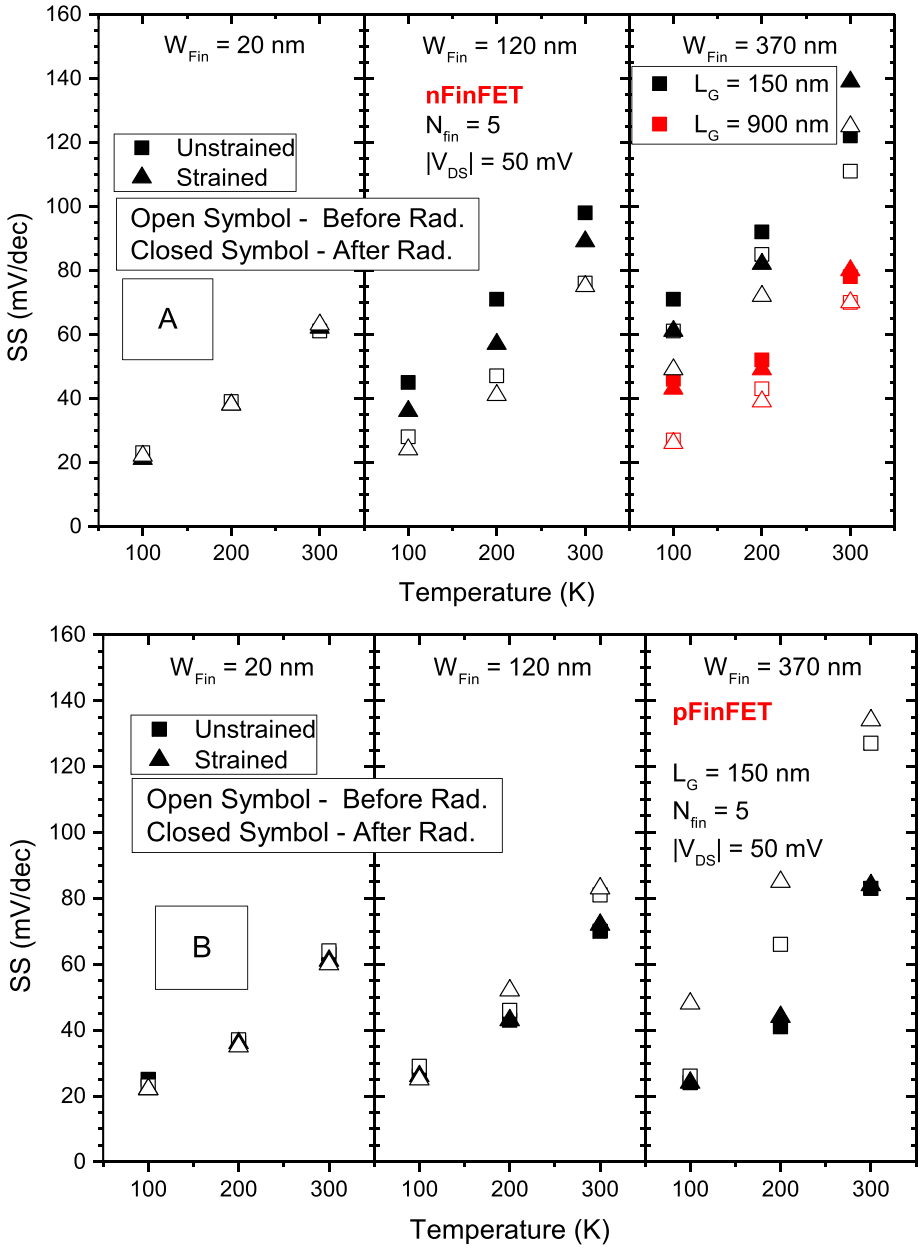

Figure 3. Experimental subthreshold swing as a function of temperature for strained and unstrained devices, before and after radiation for nFinFETs (A) and pFinFETs (B). In case of nFinFET with $W_{Fin} = 370$ nm, two L_G values are analyzed.

the back interface (in the studied temperature range) occurs at 100 K. Both effects contribute to the SS improvement, which remains near the theoretical value at 100 K (20 mV/dec) independent of W_{Fin}.

Analyzing the transconductance (gm), figure 4 presents the normalized transconductance (gm/W_{eff}) as a function of front gate voltage V_{GS} at room temperature, comparing both splits, before and after proton irradiation.

Considering only the tensile stress effectiveness, it can be noticed that for strained devices a higher transconductance is obtained due to the enhancement of the electron mobility. Adding the radiation effects to this analysis, a gm degradation was observed for irradiated devices, as expected.

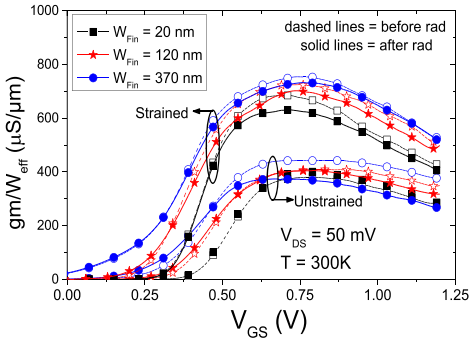

Figure 4. Normalized transconductance as a function of front gate voltage at room temperature; for strained and unstrained devices, before and after radiation for $L_G = 150$ nm.

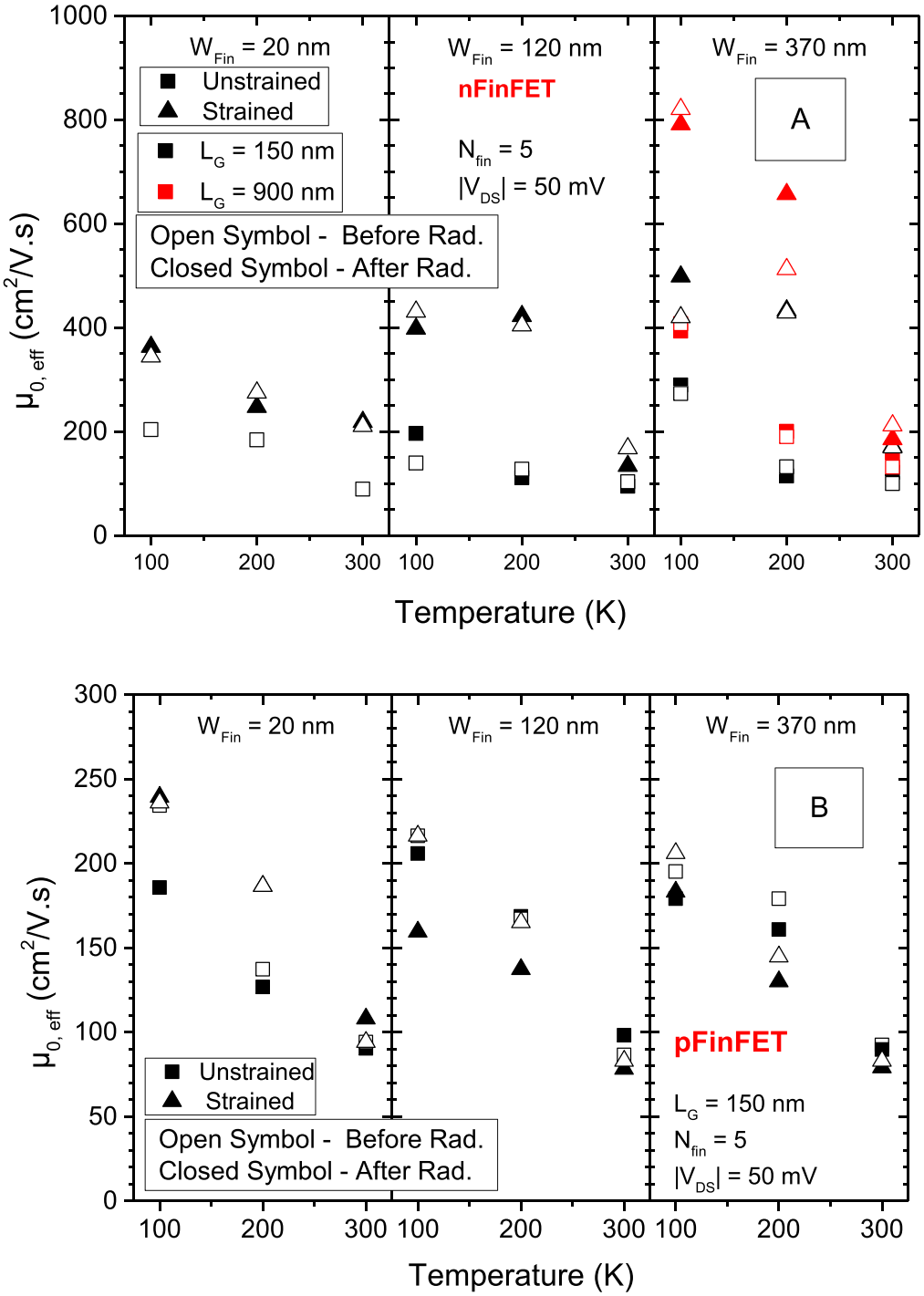

Figure 5. Effective mobility as a function of temperature for different fin widths, for strained and unstrained devices, before and after radiation for nFinFETs (A) and pFinFETs (B).

However, strained transistors, present a higher gm degradation because tensile strain introduces more interface traps, which reduces the electron mobility by Coulomb scattering [11] and the proton irradiation may increase that. In addition, strained narrow-fin devices are more affected by radiation, because their small geometry results in a small effect of biaxial strain and the lattice defects and traps may be more significant.

Another observation is that wider fin devices present higher gm due to the different electron mobility at each interface caused by a different crystallographic orientation. The top interface is (100) and in this plane electrons have higher mobility than in the side interfaces, which are (110) [12].

Since the carrier mobility changes with crystallographic orientation, the fin geometry plays an important role in the effective mobility. Thus, for wide FinFETs, the top mobility (μ_{top}) is more important, while for narrow-fin devices, the sidewall mobility (μ_{side}) has a higher influence on μ_{eff}. Another important consideration is that in the (100) plane the

electron mobility is higher, while it is better in the (110) sidewalls for the hole mobility. Putting all these elements together, one can understand why for n-type transistors a higher effective mobility is obtained for wide FinFETs and for p-type devices the better results were obtained for narrow devices (figure 5).

The transconductance analyses also pointed out the radiation and low temperature effects on the effective mobility (μ_{eff}), a parameter extracted by the Y-function method [13], for all measured devices, and presented in figure 5.

Focusing on the temperature influence on mobility, an improvement of the mobility when the temperature decreases for both types of transistors is observed, as expected [14]. However, the radiation effect degrades this parameter due to the increase of the lattice defects, it is possible to observe a smaller mobility increase as temperature goes down, showing a higher radiation influence on $\mu_{0,\ eff}$ at 100 K.

Only for wider and strained n-type FinFETs at 100 K the obtained mobility after radiation seems to be higher than before. This unexpected result can be explained by the back conduction that is high enough to cause a gm ramp (figure 6) due to a different mobility of the front and back interfaces [15] and when it occurs the Y function method is no longer valid.

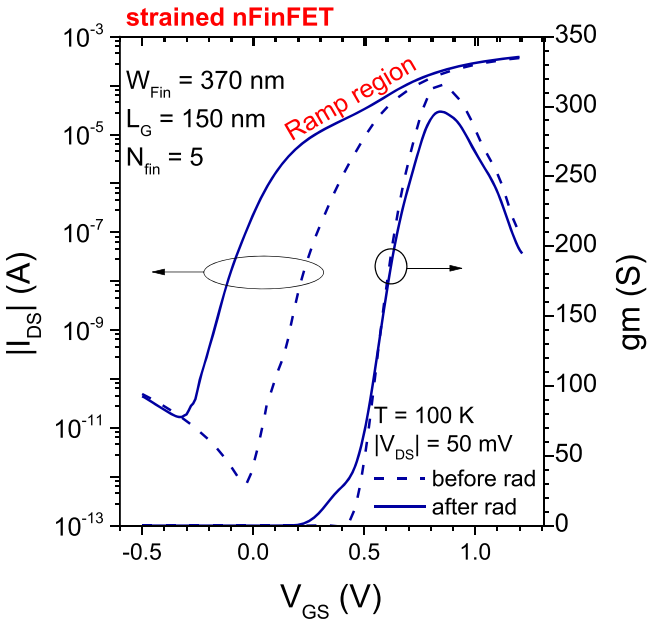

Figure 6. Experimental drain current and transconductance as a function of gate bias for strained nFinFET.

3.2. Analog parameters

The analog analysis is based on the intrinsic voltage gain (A_V), the transistor efficiency (gm/I_{DS}), the early voltage (V_{EA}) and the output conductance (g_D). The intrinsic voltage gain is calculated by equation (1).

$$|A_V| = gm/I_{DS} * V_{EA} = gm/g_D \quad (1)$$

Figure 7 presents the temperature and proton radiation influence on the narrow and strained nFinFET efficiency as a function of the inversion coefficient [16]. The narrow and strained device was chosen due to its better basic performance parameters (high mobility and better gate coupling).

Focusing on the low temperature influence on gm/I_{DS}, it is possible to observe an improvement of this parameter at 100 K reaching about 90 V A^{-2} at weak inversion. This is due to the temperature impact on the SS behavior that results in a lower SS value. At strong inversion the same trend was obtained due to the electron mobility enhancement. However, the proton radiation acts in the opposite direction to the temperature. The radiation tends to degrade the gm/I_{DS} in all inversion regimes. At weak inversion the degradation is caused by the interface states that increase the SS value and consequently the transistor efficiency and at strong inversion the main radiation effect is the mobility degradation. The effect of the proton radiation is more significant at weak inversion than at strong one.

The same gm/I_{DS} trend was obtained for pFinFETs.

Figure 8 presents the output conductance (g_D) behavior as a function of temperature for both (p and n) transistors for $|V_{DS}| = 1$ V and $|V_{GT}| = 0.2$ V.

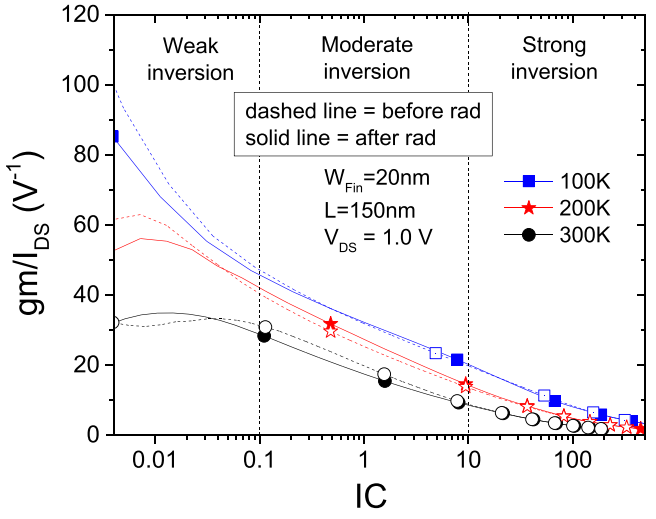

Figure 7. gm/I_{DS} ratio as a function of inversion coefficient for strained nFinFETs, at different temperatures.

Evaluating all fin widths, a g_D increase was obtained reducing the temperature, due to two different mechanisms at low temperatures: the impact ionization rate increase and the higher carrier mobility. However, for devices with a strong coupling between gates (narrow devices) the g_D degradation at low temperatures is smaller, so that the impact ionization rate could be the predominant effect on the g_D behavior. Similar for lowering of the temperature, the use of strain increases g_D due to the enhancement of the electron mobility. It can be noticed that the temperature impact on g_D is predominant compared with radiation and mechanical stress effects.

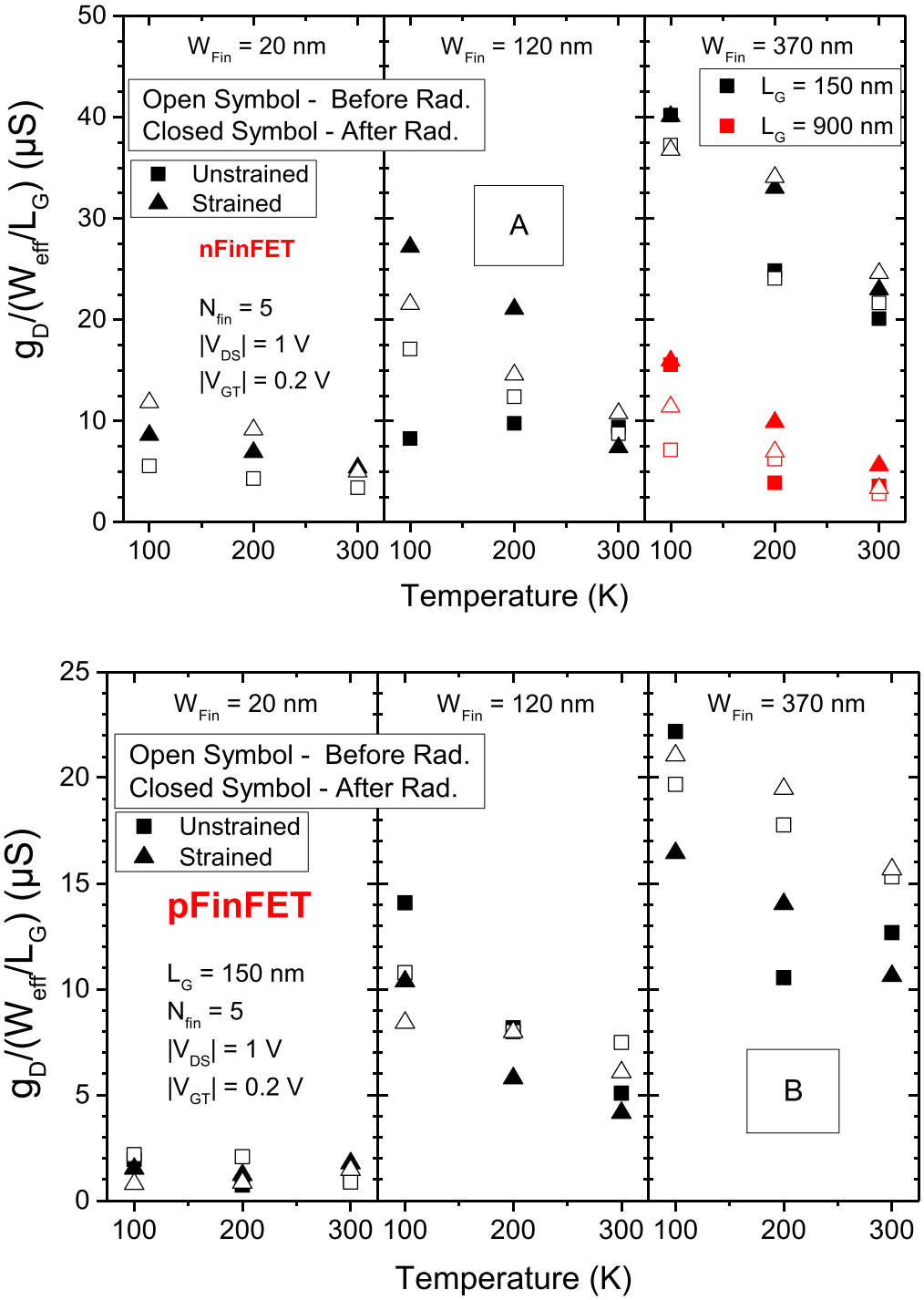

Figure 8. Output characteristic as a function of temperature for different fin widths, for strained and unstrained devices, before and after radiation for nFinFETs (A) and pFinFETs (B).

Although the V_{EA} behavior usually follows the same trend of g_D, analyzing figure 9, one can conclude that the V_{EA} is independent of temperature. Similar to the output conduction, V_{EA} also depends on both mechanisms discussed earlier. However, thinking about the V_{EA} behavior, there is competition between these effects. While the impact ionization rate increase tends to degrade the V_{EA}, the higher carrier mobility results in a higher drain current level, which tends to improve the V_{EA} value. Based on this competition, and on the almost flat V_{EA} behavior, it is possible to conclude that in the studied temperature range both effects have almost the same impact on V_{EA} and cancel each other out. The same behavior was obtained for both types of transistors.

One way of putting together the radiation and temperature effects on the investigated analog parameters is to evaluate the intrinsic voltage gain (A_V) that is presented for

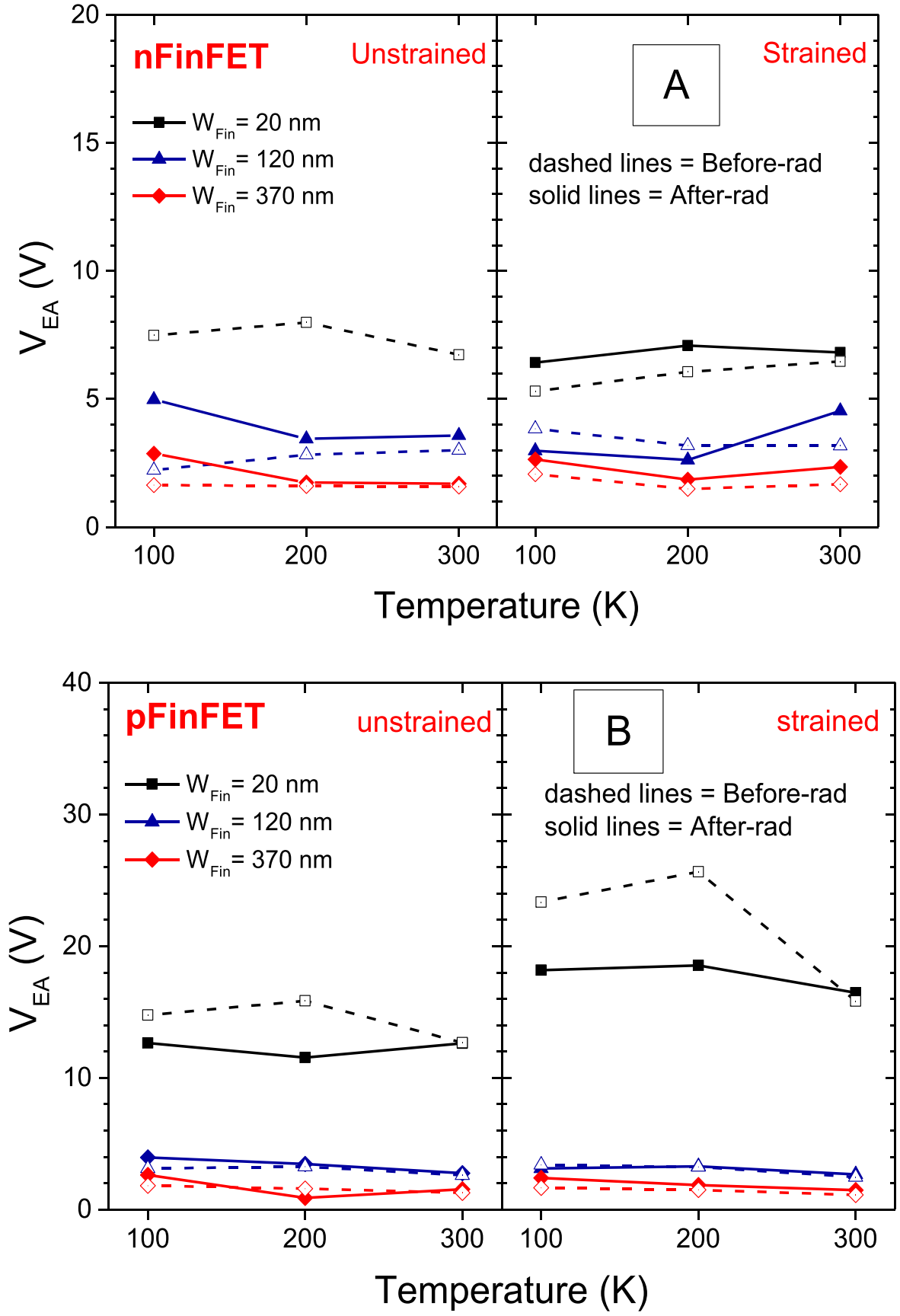

Figure 9. Early voltage behavior at low temperatures for different fin widths, for strained and unstrained devices, before and after radiation for nFinFETs (A) and pFinFETs (B).

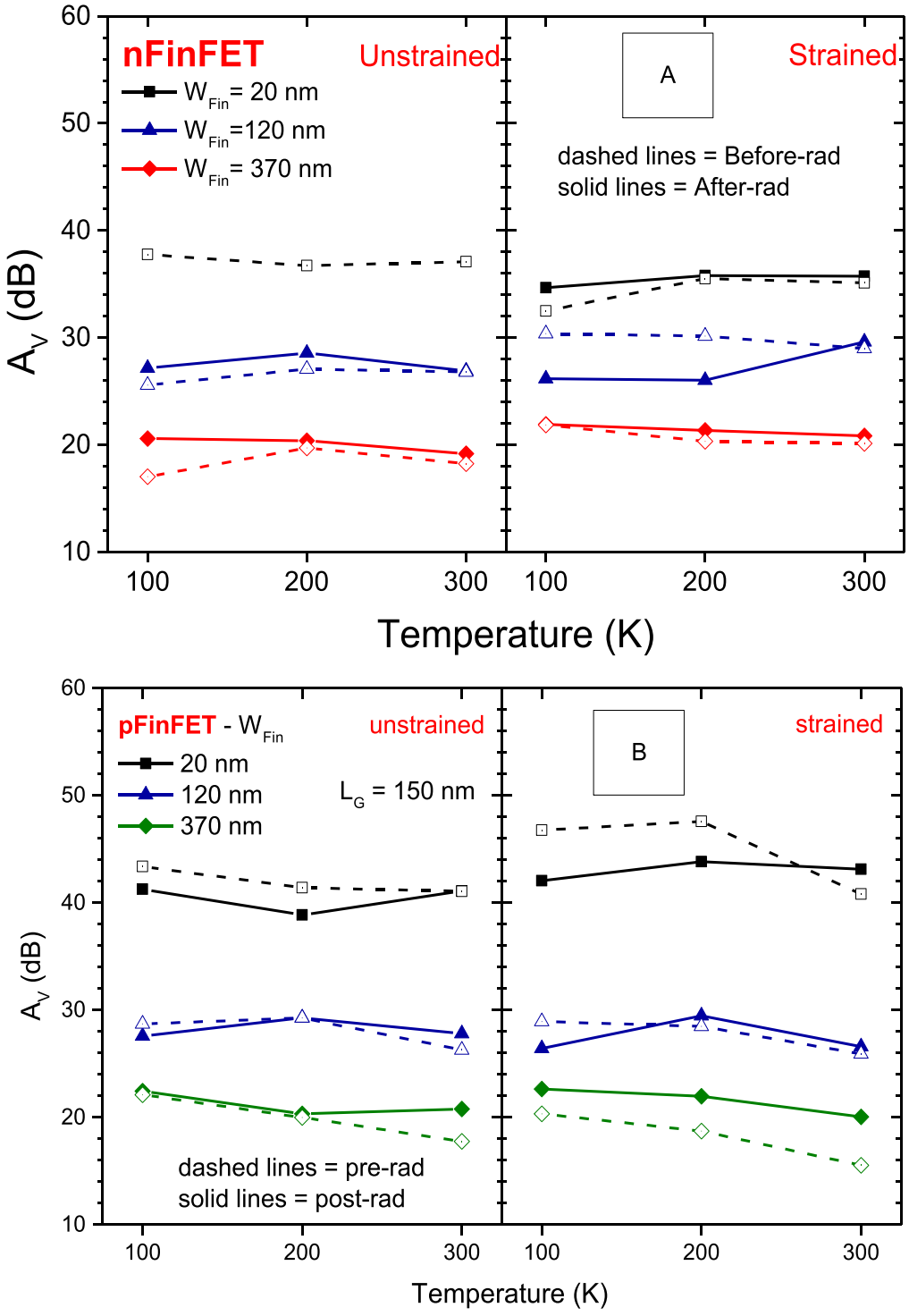

Figure 10. Intrinsic Voltage Gain (A_V) at low temperatures for different fin widths, for strained and unstrained devices, before and after radiation for nFinFETs (A) and pFinFETs (B).

$|V_{DS}| = 1$ V and $|V_{GT}| = 0.2$ V in figure 10. From this figure it is possible to see that A_V at strong inversion is slightly affected by temperature even for irradiated devices.

It can be explained by the fact that at low temperatures, in the strong inversion regime, both the drain current (I_{DS}) and gm increase due to the carrier mobility, results in only a small gm/I_{DS} rate variation. Since the intrinsic gain voltage depends on this ratio and the V_{EA} values, the A_V keeps the same V_{EA} tendency. The same explanation can be used for both nFinFETs and pFinFETs.

In summary, the pFinFETs have a better performance when looking at digital parameters like SS after irradiation, mainly due to the negative shift of V_{TH} caused by the charge buildup in the BOX. However, nFinFETs and pFinFETs

present similar behavior in terms of the analyzed analog parameters at strong inversion.

4. Conclusion

The proton irradiation effects of SOI FinFETs were evaluated from room temperature down to 100 K. Both n-channel and p-channel devices have been studied, with and without channel strain. Narrow fin devices (20 nm) are practically radiation insensitive in all cases. The influence of both temperature and radiation is more noticeable on wider devices, mainly on the strained ones, where the effects of oxide and interface traps turned out to be more significant.

The pFinFET presented an improvement with radiation concerning some basic parameters due to the turn-off of the parasitic back current. On the other hand the nFinFETs degrade due to the presence of the parasitic back current which increases in these transistors. For the analog parameters studied in this paper, both FinFET types present similar results at strong inversion.

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