Analysis of SAR ADC Performance Enhancement utilizing Stochastic Resonance

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***Abstract*—Stochastic resonance (SR) is a phenomenon where the noise of a certain intensity helps to improve the signal-to-noise ratio (SNR) of nonlinear systems. This brief applies this concept to a successive approximation register (SAR) analog-to-digital converter (ADC) to enhance its performance. To improve the effective number of bits of the SAR ADC, some additional comparisons are repeated after the normal binary search. The theoretical analysis of the performance enhancement based on the statistical information provides the optimal number of additional comparisons in terms of the ADC figure-of-merit (FoM). As this scheme allows the use of a high-input-referred-noise but low-power comparator in the SAR ADC, the total power consumption can be reduced even with the additional comparisons.**

***Index Terms*—stochastic resonance, successive approximation register, analog-to-digital converter, signal-to-noise ratio**

I. Introduction

SUCCESSIVE approximation register (SAR) analog-to-digital converter (ADC) is one of the most widely-used ADC architectures, where a comparator makes decisions to quantize the input signal through binary search [1]. In practice, to achieve the target signal-to-noise ratio (SNR) in the ADC, the input-referred noise of the comparator must be minimized well below the 1 least significant bit (LSB) resolution by proper design [2]. Stochastic resonance (SR) is a phenomenon where noise of a certain intensity helps nonlinear systems to improve their performance [3], [4]. SR has been studied in various fields such as optical systems [5], [6], electric and magnetic systems [7], [8] and neuronal systems [9]. A handful of prior works applied this concept to enhance the performance of the ADCs [10]–[12], which demonstrated that the SNR of the ADC is improved by adding proper noise.

A typical N-bit SAR ADC repeats comparisons N times based on binary search. Through the course of comparisons, there always is at least one critical decision, where the voltage difference less than 1 LSB must be resolved. The comparator in the SAR ADC must be designed to have low-enough noise for this critical decision, while in other decisions the noise requirement is not that tight. Though the LSB decision at the end of the SAR conversion is always critical, it is normally difficult to identify in advance where the critical decision occurs at the middle of conversion. Some prior works such as [13] tried to find the location of the critical decision to optimize the comparator operation. It utilizes the comparator decision time to identify the critical decision then switches to the majority voting mode to mitigate the noise contribution. However, a majority voting does not make full use of the statistical information as it simply gives a 0/1 binary decision through multiple comparisons. To make better use of them, [14] proposed to increase the number of output levels by a tri-level voting scheme. In [15], the average of 8 LSB decisions is appended to the binary SAR output to enhance the number of bit resolution. Though these techniques successfully improved the ADC performance, the theoretical analysis to optimize the design has not been provided. In [12], statistical estimation methods such as the Bayes estimator are applied to accurately estimate a conversion residue. [16] utilizes a majority voting with multiple comparisons for each bit decision to effectively realize a noise-tunable comparator using a high-input-referred-noise but low-power comparator multiple times. Though the analytical method proposed in [16] can assign the optimal number of comparisons for each bit decision when the total number of comparisons is given, based on the majority voting this method still can not fully utilize the statistical information from the multiple comparisons.

In this brief, based on the concept of SR, we present a method to enhance the bit resolution of the SAR ADC with simpler additional hardware and operation than those in [13], [15]. By simply repeating the comparisons after the normal SAR binary search, a count of 1 outputs from the comparator is appended to the binary SAR output to increase the effective number of bits. This brief theoretically analyzes the performance of the SAR ADC followed by SR-based multiple comparisons, which is so-called SR SAR ADC. The analysis and simulation results demonstrate that the SNR of the SR SAR ADC depends on the comparator noise and can be optimized with proper noise intensity, which is the benefit of SR. With the relaxed noise requirement of the comparator, we can improve the power efficiency of the SR SAR ADC compared with the typical SAR ADC. In addition, to show the feasibility of the proposed SR SAR ADC, it is compared with the SAR ADC based on majority voting technique [16].

II. Operation of the proposed SR SAR ADC

As shown in Fig. 1, the proposed SR SAR ADC is composed of a sampling switch, a binary-weighted charge-redistribution capacitor digital-to-analog converter (CDAC)

Manuscript received April 19, 2005; revised August 26, 2015.

This work is supported in part by the Institute for AI and Beyond, the University of Tokyo and in part by JST, CREST Grant Number JPMJCR19K2 and KAKENHI Grant Number JP21H03406.

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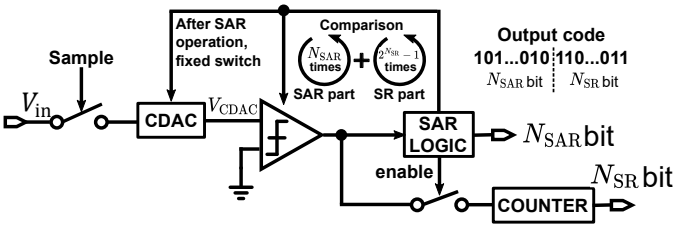

Fig. 1. A conceptual block diagram of the proposed SR SAR ADC.

and a comparator whose output is 0 or 1. It additionally has a counter to count the 1 outputs from the comparator. The output code is divided into N_{SAR}-bit SAR part and N_{SR}-bit SR part. In the first SAR part, the counter is disabled and N_{SAR}-bit A/D conversion is conducted in the same way as in the conventional SAR ADC after the input voltage V_{in} is sampled onto the CDAC. After the decision of N_{SAR}-bit binary output, the counter is enabled and the states of the N_{SAR} switches of the CDAC are fixed. At this time, the residue voltage after the SAR conversion appears at the output of the CDAC. With the CDAC switches fixed, in other words with V_{CDAC} fixed, additional comparisons are repeated $2^{N_{\mathrm{SR}}} - 1$ times and the counter counts the number of 1 outputs from the comparator.

Though ideally the two inputs to the comparator are fixed, the decision threshold of it is fluctuated in reality due to the comparator noise, which mainly comes from the transistors in the comparator [2]. Thus the additional comparison results fluctuate and have statistical information of V_{CDAC}. In the SR part, since the voltage difference between V_{CDAC} and V_{th} is small, the decision time of the comparator tends to be long, which leads to some decision errors due to metastability. We have checked with the behavioral simulations that even with 1 % decision error, its impact on the SNR is negligible.

In the proposed SR SAR ADC, the output of the counter, which is from 0 to $2^{N_{\mathrm{SR}}} - 1$, is simply appended as N_{SR}-bit binary format after the N_{SAR}-bit binary code. Consequently, the output of the proposed SAR ADC is $N = N_{\mathrm{SAR}} + N_{\mathrm{SR}}$ bits. Supposing that the input-referred noise of the comparator has Gaussian distribution, the count number in the SR part usually has nonlinear dependence on the CDAC residue, which may lead to harmonic distortions in the ADC output. As will be demonstrated in section IV, however, the analysis only considering the noise agrees perfectly with the behavioral simulation result including the nonlinearity, which means that the impact of the nonlinearity due to the SR part is negligible. Thus the performance analysis in the next section ignores this nonlinearity and uses SNR as a performance metric.

III. Performance analysis

To calculate the SNR of the proposed SR SAR ADC, we need to obtain the signal power P_{sig} and the noise power P_{noise}. Then the SNR is simply given by $P_{\mathrm{sig}}/P_{\mathrm{noise}}$. With a sinewave input whose amplitude is V_{r}, $P_{\mathrm{sig}} = V_{\mathrm{r}}^2/2$. In the proposed SR SAR ADC, we assume that the input-referred noise of the comparator is dominant, and other noise such as kT/C thermal noise and reference buffer noise is designed to be sufficiently low for the target SNR performance, so that these other noise sources do not limit the final SNR. With this assumption, we can calculate P_{noise} with the statistical variance of the quantization error. In N-bit A/D conversion, when V_{in} is the input value and $V_{\mathrm{out}}(k)$ is the analog output value reconstructed from the digital output code k ranged from 0 to $2^N - 1$, the quantization error E_{q} is described as $E_{\mathrm{q}} = V_{\mathrm{out}}(k) - V_{\mathrm{in}}$. In N-bit ADC where the LSB voltage is denoted as $\Delta = 2V_{\mathrm{r}}/2^N$, which means that the input sinewave is full scale, the relationship between $V_{\mathrm{out}}(k)$ and k is described as follows:

$$V_{\mathrm{out}}(k) = \left(k + 0.5 - 2^{N-1}\right)\Delta. \tag{1}$$

P_{noise} is calculated by multiplying the conditional expectation of E_{q}^2 given V_{in} and the probability distribution function of the input signal $f(V_{\mathrm{in}})$, then integrating the product over the entire input voltage range. Therefore, P_{noise} is given by

$$P_{\mathrm{noise}} = \int_{-V_{\mathrm{r}}}^{V_{\mathrm{r}}} E[E_{\mathrm{q}}^2 \,|\, V_{\mathrm{in}}] \cdot f(V_{\mathrm{in}}) dV_{\mathrm{in}}, \tag{2}$$

where $E[X|Y]$ is the conditional expectation operation of X given Y. $E[E_{\mathrm{q}}^2 \,|\, V_{\mathrm{in}}]$ is calculated by multiplying E_{q}^2 and the probability of having quantization error E_{q}, then summing the products all over the possible output codes. Therefore, $E[E_{\mathrm{q}}^2 \,|\, V_{\mathrm{in}}]$ is given by

$$E[E_{\mathrm{q}}^2 \,|\, V_{\mathrm{in}}] = \sum_{k=0}^{2^N-1} \{V_{\mathrm{out}}(k) - V_{\mathrm{in}}\}^2 \, P(k_{\mathrm{SAR}}, k_{\mathrm{SR}} \,|\, V_{\mathrm{in}}), \tag{3}$$

where $P(k_{\mathrm{SAR}}, k_{\mathrm{SR}} \,|\, V_{\mathrm{in}})$ is the conditional probability of getting the output code k_{SAR} and k_{SR} in the SAR part and SR part respectively when V_{in} is given. k_{SAR} and k_{SR} are respectively given by

$$k_{\mathrm{SAR}} = \sum_{i=1}^{N_{\mathrm{SAR}}} k_{\mathrm{b}}[i] \, 2^{N-i} \quad \text{and} \quad k_{\mathrm{SR}} = \sum_{i=N_{\mathrm{SAR}}+1}^{N} k_{\mathrm{b}}[i] \, 2^{N-i}, \tag{4}$$

where $k = k_{\mathrm{SAR}} + k_{\mathrm{SR}}$. k_{b} is a binary representation of k. Given V_{in}, we describe the conditional probability of k_{SAR} in the SAR part as $P_{\mathrm{SAR}}(k_{\mathrm{SAR}} \,|\, V_{\mathrm{in}})$. Then the conditional probability of k_{SR} in the SR part is described depending on the result of the SAR part as $P_{\mathrm{SR}}(k_{\mathrm{SR}} \,|\, V_{\mathrm{in}}, k_{\mathrm{SAR}})$. Finally, $P(k_{\mathrm{SAR}}, k_{\mathrm{SR}} \,|\, V_{\mathrm{in}})$ is given by

$$P(k_{\mathrm{SAR}}, k_{\mathrm{SR}} \,|\, V_{\mathrm{in}}) = P_{\mathrm{SAR}}(k_{\mathrm{SAR}} \,|\, V_{\mathrm{in}}) \cdot P_{\mathrm{SR}}(k_{\mathrm{SR}} \,|\, V_{\mathrm{in}}, k_{\mathrm{SAR}}). \tag{5}$$

A. The SAR conversion part

In N_{SAR}-bit SAR algorithm, V_{CDAC} is resolved through the N_{SAR}-time binary search while its value is changed in N_{SAR} steps as $V_{\mathrm{CDAC}}[i]$ $(i = 1, 2, ..., N_{\mathrm{SAR}})$, where $V_{\mathrm{CDAC}}[1] = V_{\mathrm{in}}$. $V_{\mathrm{CDAC}}[i]$ for $i \geq 2$ is described as

$$V_{\mathrm{CDAC}}[i] = V_{\mathrm{CDAC}}[1] - \sum_{j=1}^{i-1} (2k_{\mathrm{b}}[j] - 1) \, \frac{V_{\mathrm{r}}}{2^j}. \tag{6}$$

Then, the probability $P_{\mathrm{th}}[i]$ where $V_{\mathrm{CDAC}}[i]$ exceeds the threshold voltage of the comparator V_{th} is described. Here, we assume the input-referred noise from the comparator has Gaussian distribution whose standard deviation is σ. Then $P_{\mathrm{th}}[i]$ is given by

$$P_{\mathrm{th}}[i] = \frac{1}{2}\left\{1 + \mathrm{erf}\left(\frac{V_{\mathrm{CDAC}}[i] - V_{\mathrm{th}}}{\sqrt{2}\sigma}\right)\right\}, \tag{7}$$

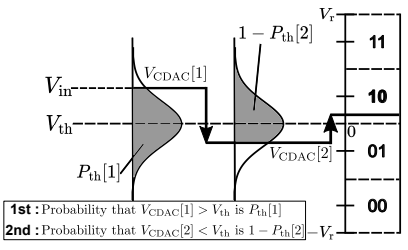

Fig. 2. An example of the probability calculation in a 2-bit SAR operation.

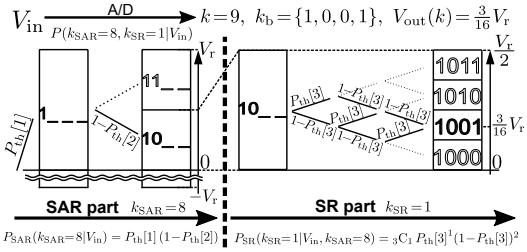

Fig. 3. An example of the decision tree when $k = 9$ and $(N_{\rm SAR}, N_{\rm SR}) = (2, 2)$.

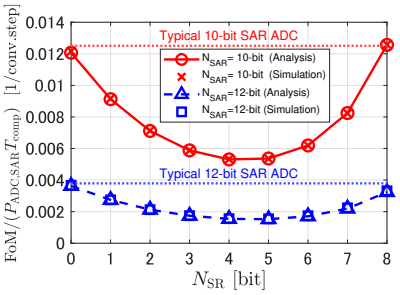

Fig. 4. FoM/$\left(P_{\rm ADC,SAR}T_{\rm comp}\right)$ versus $N_{\rm SR}$ when $N_{\rm SAR} = 10$ and 12 with $a = 0.3$, $b = 2$ and $c = 0.125$.

where

$$\mathrm{erf}(x) \triangleq \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt. \tag{8}$$

The probability where $V_{\rm CDAC}[i]$ is smaller than $V_{\rm th}$ is then $1 - P_{\rm th}[i]$. As shown in Fig. 2, in a 2-bit SAR example, when $k_{\rm SAR}$ is 2 ($k_{\rm b}[1] = 1$ and $k_{\rm b}[2] = 0$), $P_{\rm SAR}(2\,|\,V_{\rm in}) = P_{\rm th}[1]\cdot(1 - P_{\rm th}[2])$. In a general $N_{\rm SAR}$-bit case, $P_{\rm SAR}(k_{\rm SAR}\,|\,V_{\rm in})$ is given by

$$P_{\rm SAR}(k_{\rm SAR}\,|\,V_{\rm in}) = \prod_{i=1}^{N_{\rm SAR}} \{k_{\rm b}[i]P_{\rm th}[i] + (1 - k_{\rm b}[i])\,(1 - P_{\rm th}[i])\}\,. \tag{9}$$

In the above equation, when $k_{\rm b}[i] = 1$ $P_{\rm th}[i]$ is multiplied, while $1 - P_{\rm th}[i]$ is multiplied when $k_{\rm b}[i] = 0$.

B. The SR conversion part

In $N_{\rm SR}$-bit SR part, the proposed SR SAR ADC repeats comparisons $2^{N_{\rm SR}} - 1$ times with the fixed $V_{\rm CDAC}$ and counts the number of 1 outputs from the comparator. $V_{\rm CDAC}$ in the SR part is determined by the conversion result of the SAR part, which is described as $V_{\rm CDAC}[N_{\rm SAR} + 1]$ and is constant throughout the SR part. The operation in the SR part is a random experiment where every outcome is either 0 or 1. The probability of 1 is constant at every comparison. This operation is called as Bernoulli or binomial trial [17]. Therefore the probability $P_{\rm SR}(k_{\rm SR}\,|\,V_{\rm in}, k_{\rm SAR})$ where $V_{\rm CDAC}[N_{\rm SAR}+1]$ exceeds the threshold voltage of the comparator $k_{\rm SR}$ times is given by

$$\begin{aligned} P_{\rm SR}(k_{\rm SR}\,|\,V_{\rm in}, k_{\rm SAR}) = {}_{2^{N_{\rm SR}}-1}{\rm C}_{k_{\rm SR}} P_{\rm th}[N_{\rm SAR}+1]^{k_{\rm SR}} \times \\ (1 - P_{\rm th}[N_{\rm SAR}+1])^{2^{N_{\rm SR}}-1-k_{\rm SR}}\,. \end{aligned} \tag{10}$$

With (5), (9) and (10), $P(k_{\rm SAR}, k_{\rm SR}\,|\,V_{\rm in})$ can be calculated. An example of the decision tree when $k = 9$ and $(N_{\rm SAR}, N_{\rm SR}) = (2, 2)$ is shown in Fig. 3. In this example, the output is 4-bit as $k_{\rm b} = \{1, 0, 0, 1\}$, and $V_{\rm out}$ is calculated by substituting $N = 4$ and $k = 9$ to (1), yielding $V_{\rm out} = V_{\rm r} \times 3/16$. Then $P_{\rm noise}$ is given by using (2) and (3) to calculate the SNR.

C. Extension to Majority-Voting-Based Technique

Since the performance analysis so far does not assume any specific usage of the comparator, it can be straightforwardly extended to analyze the performance of other ADCs using multiple comparisons. In this section, we apply our analysis framework to [16], which employs a majority voting, to demonstrate the feasibility of our analysis. In [16, (3)], the code mean-squared error (MSE) is defined as

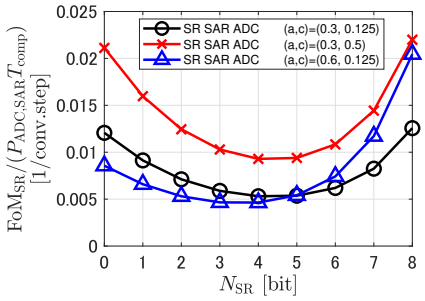

Fig. 5. FoM$_{\rm SR}$/$\left(P_{\rm ADC,SAR}T_{\rm comp}\right)$ versus $N_{\rm SR}$ when $N_{\rm SAR} = 10$ and $b = 2$ with different a and c values.

$$\text{code MSE} = \int_{-V_{\rm r}}^{V_{\rm r}} E\left[(k - \hat{k})^2 | V_{\rm in}\right] f(V_{\rm in}) dV_{\rm in}, \tag{11}$$

where $\hat{k}$ is an ideal output code in the absence of the comparator noise. Though the calculation of $E\left[(k - \hat{k})^2 | V_{\rm in}\right]$ is not explicitly described in [16], based on our analysis framework, we can derive its analytical expression, which is actually given by the same equation as (3), while the probability $P(k_{\rm SAR}, k_{\rm SR}\,|\,V_{\rm in})$ in (3) must be replaced with $P(k\,|\,V_{\rm in})$. Though the calculation of $P(k\,|\,V_{\rm in})$ is different from that in a typical SAR operation due to the majority voting for each bit decision, it is derived in the same manner as for (9). Denoting the probability that majority voting in i-th bit decision results in 1 as $P_{\rm MV}[i]$, $P(k\,|\,V_{\rm in})$ is given by

$$P(k\,|\,V_{\rm in}) = \prod_{i=1}^{N} \{k_{\rm b}[i]P_{\rm MV}[i] + (1 - k_{\rm b}[i])\,(1 - P_{\rm MV}[i])\}\,. \tag{12}$$

When the number of comparisons in i-th decision is N_i, $P_{\rm MV}[i]$ is calculated in the same manner as for [16, (14)], which leads to

$$P_{\rm MV}[i] = \sum_{j=\frac{N_i+1}{2}}^{N_i} {}_{N_i}{\rm C}_j\, P_{\rm th}[i]^j\, (1 - P_{\rm th}[i])^{N_i - j}\,. \tag{13}$$

In [16], the optimal number of comparisons for each bit decision is assigned to $N_i = [1\ 1\ 1\ 3\ 3\ 5\ 7\ 13\ 19\ 29]$ for 10-bit SAR ADC when the comparator noise $\sigma = \Delta$, where Δ is the 1 LSB of a 10-bit ADC, and the total number of comparisons

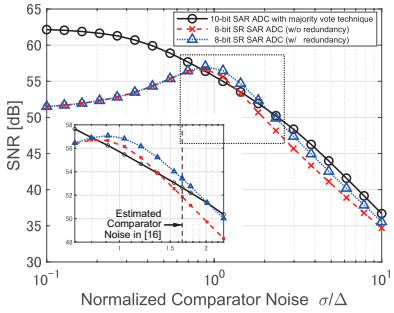

Fig. 6. The SNR of the proposed SR SAR ADC versus the comparator noise normalized by Δ, which is 1 LSB of a 10-bit ADC, when $(N_{\mathrm{SAR}}, N_{\mathrm{SR}}) = (8, 4)$ compared with the SAR ADC based on majority voting [16].

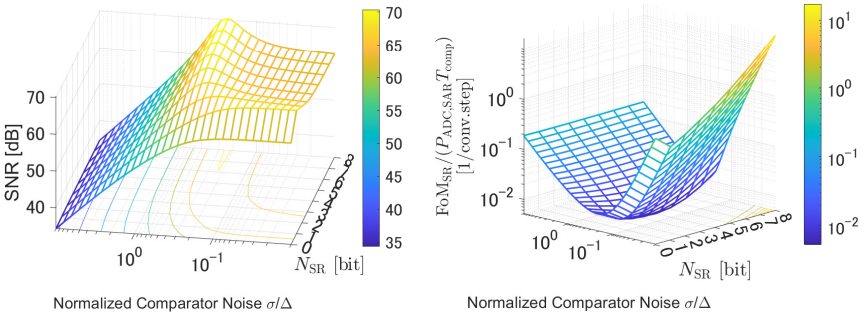

Fig. 7. The analysis results of the proposed SR SAR ADC versus the comparator noise and N_{SR} when N_{SAR} =10; (a) The SNR and (b) $\mathrm{FoM}_{\mathrm{SR}}/(P_{\mathrm{ADC,SAR}}T_{\mathrm{comp}})$ with $a = 0.3$, $b = \sigma/(\Delta/2\sqrt{12})$ and $c = 0.125$.

is restricted to 82. In this case, the code MSE they derived is 0.234, which perfectly agrees with the one derived through our analysis.

IV. Experimental Results

In this section, we compare the proposed SR SAR ADC with a typical SAR ADC in terms of their figure of merit (FoM). Here we use Walden FoM defined as $\mathrm{FoM} = P_{\mathrm{ADC}}/(f_{\mathrm{s}} \cdot 2^{\mathrm{ENOB}})$, where P_{ADC} and f_{s} are the ADC power consumption and the sampling frequency, respectively. ENOB is an effective number of bits. In this brief, it is given by $\mathrm{ENOB} = (\mathrm{SNR[dB]} - 1.76)/6.02$. Here we assume that the sampling period of the N_{SAR}-bit SAR ADC is $T_{\mathrm{SAR}} = 1/f_{\mathrm{SAR}} = T_{\mathrm{S/H}} + N_{\mathrm{SAR}}T_{\mathrm{comp}}$, where $T_{\mathrm{S/H}}$ and T_{comp} are the time to sample-and-hold the input and the time for one comparison, respectively. We also assume that for the SAR ADC the energy consumption for one A/D conversion is given by $E_{\mathrm{SAR}} = P_{\mathrm{ADC,SAR}}T_{\mathrm{SAR}} = E_{\mathrm{other}} + N_{\mathrm{SAR}}E_{\mathrm{comp}}$, where E_{comp} is the energy required for one bit decision in the comparator. E_{other} is the rest energy for one A/D conversion, which is composed mainly of CDAC driver and S/H circuits in the SAR ADC. We suppose that $N_{\mathrm{SAR}}E_{\mathrm{comp}} = aE_{\mathrm{SAR}}$ and $E_{\mathrm{other}} = (1-a)E_{\mathrm{SAR}}$ $(0 < a < 1)$. Assuming $T_{\mathrm{S/H}} = cT_{\mathrm{SAR}}$ $(0 < c < 1)$, for the typical N_{SAR}-bit SAR ADC, the FoM is given by

$$\mathrm{FoM}_{\mathrm{SAR}} = \frac{P_{\mathrm{ADC,SAR}}}{f_{\mathrm{SAR}} \cdot 2^{\mathrm{ENOB}}} = \frac{N_{\mathrm{SAR}}T_{\mathrm{comp}}}{1-c}\frac{P_{\mathrm{ADC,SAR}}}{2^{\mathrm{ENOB}}}. \tag{14}$$

For the proposed SR SAR ADC, on the other hand, the number of comparisons becomes $N_{\mathrm{SAR}} + 2^{N_{\mathrm{SR}}} - 1$. Among these bit decisions, in the SR part the CDAC switches are fixed to have a constant V_{CDAC}. Thus even with the additional SR comparisons, E_{other} is not changed from the typical SAR ADC case, while the comparator consumes more energy for additional comparisons. The energy consumption of the comparator is in a trade-off relationship with its noise. Generally speaking, when we make the input-referred noise of the comparator $\times b\,(b > 0)$, for the same speed, the comparator energy consumption becomes $\times b^{-2}$ according to [2]. In other words, if we want lower noise, we need to consume more energy in the comparator. Thus the total energy consumption of the SR SAR ADC for one A/D conversion is $E_{\mathrm{SR}} = E_{\mathrm{other}} + b^{-2}E_{\mathrm{comp}}(N_{\mathrm{SAR}} + 2^{N_{\mathrm{SR}}} - 1)$. Consequently, the FoM of the proposed SR SAR ADC is given by

$$\begin{aligned}\mathrm{FoM}_{\mathrm{SR}} &= \frac{E_{\mathrm{SR}}}{2^{\mathrm{ENOB}}} \\ &= \frac{N_{\mathrm{SAR}}T_{\mathrm{comp}}}{1-c}\frac{P_{\mathrm{ADC,SAR}}}{2^{\mathrm{ENOB}}}\left\{1 - a + \frac{a}{b^2}\left(1 + \frac{2^{N_{\mathrm{SR}}} - 1}{N_{\mathrm{SAR}}}\right)\right\}.\end{aligned} \tag{15}$$

Here we assume that the power consumed by additional circuit blocks such as a counter is negligible. As a sanity check, when $N_{\mathrm{SR}} = 0$ and $b = 1$, which means that the circuit is operating as a simple SAR ADC, (15) is equivalent to (14). Sweeping N_{SR}, the value $\mathrm{FoM}_{\mathrm{SR}}/\left(P_{\mathrm{ADC,SAR}}T_{\mathrm{comp}}\right)$ of the proposed SR SAR ADC is plotted in Fig. 4 for two cases where $N_{\mathrm{SAR}} = 10$ and $N_{\mathrm{SAR}} = 12$. $\sigma = \Delta/\sqrt{12}$ comparator noise is used for $N_{\mathrm{SAR}} = 10$ and $\sigma = \Delta/(4\sqrt{12})$ is used for $N_{\mathrm{SAR}} = 12$ where Δ is 1 LSB of a 10-bit ADC, so that the original comparator has the input-referred noise comparable to the quantization noise. In the following experiments, we use $b = 2$ to assume the use of a lower-power but larger-input-referred-noise comparator for the proposed SR SAR ADC. $a = 0.3$ and $c = 0.125$ are reasonably assumed with reference to [1], [15]. The ENOB in (15) was obtained with the analysis in Sect. III as well as with behavioral simulations. For behavioral simulations, as the random noise is involved, the average value of 128 simulation results is plotted for each point. Two results perfectly agree with each other in both cases, which proves the feasibility of the analysis. For the typical SAR ADC with $b = 1$ and $N_{\mathrm{SR}} = 0$, the ENOB in (14) was also obtained and $\mathrm{FoM}_{\mathrm{SAR}}/\left(P_{\mathrm{ADC,SAR}}T_{\mathrm{comp}}\right)$ values are indicated with dotted lines on the same graph. The proposed SR SAR ADC achieves the optimum FoM at $N_{\mathrm{SR}} = 4$ when $N_{\mathrm{SAR}} = 10$ and at $N_{\mathrm{SR}} = 5$ when $N_{\mathrm{SAR}} = 12$, which is more power efficient than the SAR ADC without the SR operation. Fig. 5 shows the dependence on the parameters a and c. Supposing that T_{comp} is fixed by the comparator design, the FoM becomes worse when c increases as it simply slows down the sampling rate. When a increases, which means that the comparator power is more dominant in the ADC, the optimum N_{SR} shifts to a lower value.

Fig. 6 plots the SNR versus the standard deviation of the comparator input-referred noise σ normalized by 1 LSB of the 10-bit ADC Δ. The cross marks and triangles show the cases without and with the redundancy[1], respectively. As expected, the SNR changes like a bell-shaped curve [4], which has a peak

when σ is a certain non-zero value. Specifically, the SNR is optimal when σ is close to Δ in both cases.

For the performance comparison, the SNR of the 10-bit SAR ADC using majority voting technique [16] is simulated and plotted with circles on the same graph by sweeping σ. Here, both in our SR SAR and the majority voting SAR ADCs, the total number of comparisons is the same. Based on the measured performance described in [16], the input-referred noise of their comparator is estimated to be $\sigma = 1.65\Delta$. At this design point, the SNR of the proposed SR SAR ADC without redundancy is slightly below the SNR of the majority voting technique, while with redundancy it improves to the better value though it requires one more additional bit decision. In addition, by decreasing the comparator noise with some more power, the proposed SR SAR ADC becomes advantageous at around the peak of the bell-shaped curve. As the proposed SR SAR ADC in this comparison is an 8-bit architecture while the majority voting technique uses a 10-bit one, assuming the same power consumption in the comparator with the same number of total comparisons, the proposed technique is expected to be lower power with better SNR, which leads to better FoM at this design point. Interestingly, in the SR SAR ADC, suppressing the noise too much reduces the SNR, while in the majority voting its SNR monotonically improves with smaller noise. This phenomenon clearly demonstrates the effect of the SR that helps to improve the SNR of a nonlinear system with proper intensity of noise, which does not appear in the majority voting. For both schemes, repeating decisions with a too-low-noise comparator is not an efficient choice, as the lower-noise comparator usually requires more power and the SNR improvement is limited even with additional comparisons.

To find the optimal design point, Fig. 7 plots the analysis results of the SNR and $\mathrm{FoM_{SR}}/(P_{\mathrm{ADC,SAR}}T_{\mathrm{comp}})$ by sweeping N_{SR} and σ for $N_{\mathrm{SAR}} = 10$ as an example. For FoM calculation, $a = 0.3$ and $c = 0.125$ are used as in Fig. 4. To take into account the trade-off between the comparator power and its noise, we change the value of b along with σ based on $b = \sigma/(\Delta/2\sqrt{12})$ where Δ is 1 LSB of a 10-bit ADC. As shown in Fig. 7(a), when σ is close to Δ, the SNR improves along with N_{SR} but the improvement slows down at large N_{SR} where a huge number of comparisons is required. Fig. 7(b) shows that the optimum FoM is achieved at N_{SR} where the ENOB improvement is still significant with reasonable number of additional comparisons. When σ is too small the SNR does not increase with N_{SR}, because here the residue voltage from the CDAC plus the noise can hardly cross the threshold in the SR part. In consequence, as we can not obtain meaningful statistical information, the SR part does not contribute to improve the SNR with too small comparator noise.

V. Conclusion

In this brief, we analyzed the performance enhancement of the SAR ADC by introducing the concept of SR. The results of the analysis and the simulation reveal that with the proposed SR SAR ADC we can achieve better FoM by using a higher-input-referred-noise but lower-power comparator.

[1]To introduce 1-bit redundancy, we used the CDAC weight vector of [127 64 32 16 8 4 2 1 1] for the 8-bit A/D conversion.

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