Analysis of Self-Heating Effects in Ultrathin-Body SOI MOSFETs by Device Simulation

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(Invited Paper)

***Abstract*—This paper discusses self-heating (SHE) effects in silicon-on-insulator (SOI) CMOS technology and applies device simulation to analyze the impact of thermal effects on the operation of nanoscale SOI n-MOSFETs. A 2-D drift-diffusion electrothermal simulation, using an electron transport model calibrated against Monte Carlo simulations at various temperatures, is employed in the analysis. We report the effects of device-structure parameters, such as SOI layer thickness, buried-oxide (BOX) thickness, source/drain (S/D) extension length, and thickness of the elevated S/D region, on the SHE of nanoscale MOSFETs. The SHE effects become significant due to the adoption of thin silicon layers and to the low thermal conductivity of the BOX, leading to the rise of large temperature under nominal operation conditions for high-performance digital circuits. The ac performance of SOI MOSFETs is influenced as well, and in particular, a severe degradation of the cutoff frequency of very short MOSFETs is predicted by numerical electrothermal device simulations. Although the effects of SHE on device performance are found to be somewhat modest and might be mitigated through device design, they may result in a degradation of the long-term reliability.**

***Index Terms*—CMOS, numerical simulation, self-heating, silicon-on-insulator (SOI).**

I. Introduction

THE DEMAND for high circuit performance has been addressed historically by miniaturization of device dimensions and increased device packing densities [1], [2]. The International Technology Roadmap of Semiconductors (ITRS) [3] imposes aggressive scaling trends for the gate length (L_G) and equivalent gate oxide thickness (EOT) to achieve a 17% annual reduction of the intrinsic switching delay (CV/I) for high-performance transistors.

Over time, this strategy has become insufficient because of the degradation of mobility consequent to the increasing channel-doping density. Furthermore, it has become increasingly difficult to control undesired phenomena, such as the leakage current across the gate oxide, short-channel effects causing an excessive OFF current (i.e., the subthreshold current in a transistor that is nominally OFF) and a large dependence of threshold voltage (V_T) on drain bias, and the variability of V_T, due to statistical fluctuations of channel length and of the distribution of the dopant atoms in the channel [4].

Technology scaling also impacts power dissipation. The classic constant-field scaling rule predicts a significant reduction of the dynamic power in a given circuit $(\propto CV_{\rm DD}^2 f)$, whereas the power dissipation per unit area is expected to stay constant. Actual scaling trends have relaxed the reduction of supply voltage in order to comply with the ITRS requirements in terms of gate delay, therefore leading to a steady, although not dramatic, increase of dynamic power density [5]. The power problem has become even worse due to increases in both the subthreshold drain current and the gate leakage current such that the static power density has become comparable with the usually dominant dynamic power contribution [5]–[7].

This increase in power translates into larger heat generation and rising temperatures. Heat dissipation typically occurs through the silicon bulk toward the backside of the die, and thermal energy is ultimately removed by a heat sink.

The relevance of thermal effects in device design increases as a consequence of the large modifications to the basic MOSFET structure that are currently being introduced. In fact, in order to overcome the increasing difficulties in achieving improvements in terms of device and circuit performance, substantial innovations have been introduced or are currently proposed for the near future, including new materials to be adopted for the fabrication of both the wafer and the single device, and modifications to the device architecture. In the short term, adoption of new materials for the realization of the gate stack and the channel of conventional bulk and partially depleted (PD)-SOI MOSFETs is suggested: High-k dielectrics allow the scaling of equivalent oxide thickness that keeps tunneling gate leakage under control [8], whereas new material composition of the channel region can improve channel mobility [9], [10], thus increasing the $I_{\rm ON}/I_{\rm OFF}$ ratio. Additional innovations in

Manuscript received June 11, 2007. This work was supported in part by the Italian MIUR under the PRIN 2006094117 Project and in part by the EU under the PULLNANO IST-026828 Project. The review of this paper was arranged by Editor B. Zhao.

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Digital Object Identifier 10.1109/TED.2007.911354

device architecture are under active scrutiny, with the intention to introduce ultrathin-body (UTB) fully depleted (FD) SOI devices and multiple gate devices, where the short-channel effects are effectively suppressed by scaling down the thickness of the silicon layer [11], [12].

All these innovations must be carefully analyzed from the point of view of the heating effects. The adoption of SiGe alloys or thick buried-oxide (BOX) layers in SOI wafers significantly impacts the thermal properties of the device as these materials possess a much lower thermal conductivity compared with the bulk silicon. In addition, it has been recently pointed out that ultrathin silicon layers with thickness (T_{SI}) on the order of a few tens of nanometers, which are required in order to cope with the short-channel effects in FD single- and double-gate devices, present a degraded thermal conductivity due to phonon boundary scattering that reduces the phonon mean free path significantly [13]–[16].

The impact of self-heating (SHE) in the SOI MOSFETs has been the subject of investigation in the past by both experiments [17]–[20]: 1-D thermal models [21], [22] and 2-D device simulation [23]–[25].

In this paper, we apply a 2-D electrothermal device simulation, with a transport model tuned to the results of Monte Carlo (MC) transport analysis, to investigate the effects of heating on the I–V characteristics of ultrashort MOSFETs and to analyze the impact of available technology options on the SHE occurring in UTB SOI MOSFETs, taking into consideration both digital and analog circuit applications.

This paper is organized as follows. The problem of heat generation and transport through the silicon substrate and interconnects, and the impact of heating on the I–V MOSFET characteristics are reviewed in Section II. The simulation methodology adopted in the applicative part of the work is described in Section III. Section IV is devoted to the analysis of the SHE effects in nanoscale UTB SOI MOSFETs. Finally, conclusion is drawn in Section V.

II. Short Review of Thermal Effects in Nanoscale MOSFETs

A. Heat Generation in Short Devices

Heat generation in MOSFETs occurs through the emission of phonons by carriers heated by the electric field in the channel region. Since the electric field is maximum at the drain end of the channel and the source-to-drain distance is comparable to the mean free path for phonon scattering (on the order of 10 nm), each carrier suffers few scattering events, if not scattering at all, within the intrinsic channel region (quasi-ballistic transport). Hence, most of the heating process takes place inside the drain.

The most common approach for the analysis of heat generation consists of calculating the heating rate per unit volume as the scalar product of the electric field and current-density vectors ($\mathbf{J} \cdot \mathbf{F}$). This approach is strictly local in its nature and fails to take into account the nonlocal characteristics of carrier heating and phonon emission. This local model predicts that the maximum of heat-generation rate takes place where the peak of electric field is located, i.e., at the drain junction; more accurate calculations of phonon emission performed by the MC transport simulations predict a much broader heat-generation region, with a lower peak value, displaced inside the drain junction [26]. Nonlocal effects on carrier heating and phonon emission become more relevant as the device channel length approaches the mean free path for phonon emission. The precise quantification of the impact of the local-heating approximation is still an open issue because the analysis in [26] lacks a detailed treatment of short- and long-range electron–electron interaction that influences the carrier heating and the subsequent cooling process (thermalization) occurring in the drain region; furthermore, the simulations in [26] do not account self-consistently for the impact of heat generation on the transport properties. In spite of its inherent local approximation, the conventional model for Joule heating is still largely adopted in consideration of the ease of implementation in the frame of device simulators, allowing an efficient electrothermal simulation by the self-consistent coupling of carrier transport, heat generation, and heat transport, thus providing the possibility to investigate the impact of technological options on device performance, including the SHE effects [27]. Doubtless to say, more work is needed in order to quantify the effects of nonlocal heat generation and to include them in the electrothermal device simulation.

B. Transport of Heat Generated in Nanoscale Semiconductor Devices

The transport of heat in semiconductors is due to the propagation of lattice vibrations (phonons), whereas the contribution by electrons (dominant in the case of metals) is estimated on the order of 1% even in the case of very large concentrations [28].

Different temperatures at two positions in a semiconductor device imply different distributions of phonons. Since the change in phonon distribution may only occur due to scattering, the temperature may vary only over a length larger than the phonon mean free path.

The simple phenomenological approach based on the Fourier's law of heat diffusion is the most widely adopted one for modeling the heat transport

$$C_S \frac{\partial T}{\partial t} = \nabla \cdot (k_S \nabla T) + H(\vec{r}, t) \tag{1}$$

where C_S and k_S are the heat capacity per unit volume and the thermal conductivity of the semiconductor, respectively, and $H(\vec{r}, t)$ represents the heat-generation rate per unit volume.

The thermal conductivity can be written as

$$k_S = C_S v \Lambda_S / 3 \tag{2}$$

where Λ_S represents the phonon mean free path (approximately 200–300 nm in undoped bulk silicon at 300 K), and v is the average phonon velocity.

When studying the heat transport in nanoscale devices with dimensions on the order of, or smaller than, the phonon mean free path, subcontinuum transport effects occur [29] as follows.

1) Hot-spot ballistic phonon-emission effects: heat generation due to optical phonon emission by heated electrons,

taking place in a region of limited extension (hot spot) compared with the phonon mean free path, leads to higher temperature rise compared with the predictions from diffusion theory based on the Fourier's law because a significant change in temperature may occur only over a distance comparable or larger than the phonon mean free path.

2) Hot spot far from equilibrium effects: SHE occurs mainly through the emission of optical phonons characterized by low propagation velocity. On the other hand, the heat transport involves much faster acoustic phonon modes. Due to the large rate of the optical phonon emission at the drain channel end and to the difference in the propagation velocity of the optical and acoustic phonons, a localized out-of-equilibrium condition is realized, in which the ratio of optical-phonon concentration to acoustic-phonon concentration is much larger than at equilibrium, leading to a reduced heat-spreading capability.
3) Phonon boundary scattering in thin films: thermal conductivity in thin films is substantially reduced with respect to bulk crystals due to the enhanced scattering of phonons with the film boundaries, causing a large reduction of the phonon mean free path.

The first two issues previously listed challenge the continuum diffusion theory of heat transport represented by (1). A higher order treatment of heat transport, which is able to cope with the hot-spot-related issues aforementioned, would require the solution of several phonon Boltzmann transport equations (one for each phonon mode) coupled with each other by the phonon scattering. This approach is difficult due to both the complexity of the solution of the Boltzmann transport equation (BTE) when applied to realistic structures, and the limited knowledge about the selection rules and transition rates for phonon–phonon interactions. Several simplified approaches for the simulation of heat transport based on the phonon BTE have been proposed, and most of them are discussed in [30]. In particular, the split-flux model developed in [31] has been applied in [32] to the analysis of heat transport in short MOSFETs.

The enhanced boundary scattering in thin films leads to a reduced phonon mean free path, thus reducing the effects of hot-spot ballistic phonon emission and making the limitations of (1) less critical. The enhanced scattering can be taken into account in the frame of the simple diffusion theory (1) by appropriately modifying the thermal conductivity in order to account for the enhanced boundary scattering.

In [21], the effect of boundary scattering is included by assuming a boundary-scattering-limited mean free path $\Lambda_{\rm BS} = T_{\rm SI}$. The overall mean free path is then calculated through the Mathiessen rule $\Lambda_S^{-1} = \Lambda_{S-bulk}^{-1} + \Lambda_{\rm BS}^{-1}$, where Λ_{S-bulk} is the mean free path for bulk silicon. The $T_{\rm SI}$-dependent phonon mean free path allows the calculation of the reduced thermal conductivity using (2). In [21], this simple model has been extrapolated to the $T_{\rm SI}$ values down to a few nanometers to analyze scaling issues affecting the UTB SOI MOSFETs with L_G down to 10 nm.

In [15] and [16], experimental data of thermal conductivity in the ultrathin silicon layers are reported, and a physics-based model for the effect of thickness-dependent boundary scattering on the thermal conductivity is proposed. This model, which includes the dependence on temperature, has been validated by comparison with the experimental data for $T_{\rm SI}$ down to 20 nm.

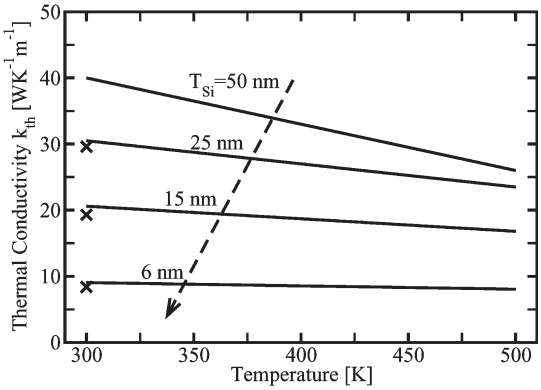

Fig. 1. Thermal conductivity versus temperature in thin silicon layers calculated according to the models in [15] (lines) and [21] (crosses).

The thermal conductivity of thin silicon layers calculated according to the models in [15] (lines) and [21] (crosses) is shown in Fig. 1. The model in [15], which is validated for thicknesses down to 20 nm, is extrapolated in this paper to $T_{\rm SI}$ down to 6 nm and implemented in the thermal-transport module of the electrothermal simulator.

C. Impact of Heating on the I–V Characteristics of Ultrashort MOSFETs

1) Above-Threshold I–V Characteristics: MOSFETs with gate length well below 100 nm feature a quasi-ballistic transport as the carriers that are traveling along the channel can suffer only a very small number of scattering events [33], [34].

A well-accepted compact model for the ON current in the quasi-ballistic regime has been proposed in [35] and [36]

$$I_{\rm DS} = C_G(V_G - V_T)v_{\rm inj}\frac{1-r}{1+r}. \tag{3}$$

Equation (3) expresses the current at the virtual source (VS), i.e., the position of the top of the source-channel potential-energy barrier, where the inversion charge can be effectively approximated by a 1-D analysis. V_T represents the device threshold voltage that depends on the temperature through the intrinsic carrier concentration, which is ultimately related to the carrier energy distribution at equilibrium and to the temperature dependence of the silicon band gap. $v_{\rm inj}$ represents the average velocity of those carriers that cross the barrier with positively directed (source-to-drain) velocity. Under nondegenerate quasi-equilibrium conditions, $v_{\rm inj}$ is well approximated by the thermal velocity of an equilibrium half-Maxwellian electron distribution, and it is an increasing function of the temperature ($v_{\rm inj} \approx v_{\rm th} \propto T^{0.5}$). The parameter r represents the reflection coefficient, i.e., the ratio of the current of carriers injected into the channel at the VS and scattered back into the source to the total current of carriers injected at the VS.

According to Lundstrom and Ren [36], r can be expressed as

$$r = \frac{\lambda}{\lambda + 2L_{k_BT}} \tag{4}$$

where λ represents the carrier mean free path, and L_{k_BT} is the length over which the channel potential energy drops by k_BT/q starting from the VS.

The ballistic ratio defined as $\mathrm{BR} = (1-r)/(1+r)$ represents the ratio of the actual current to the ballistic current, the upper limit for I_{DS}, which is attainable in the absence of scattering in the channel ($r = 0$).

The main temperature dependences of this model are discussed in [37], and the model itself has been applied in [22] to a comprehensive analysis of SHE in the UTB SOI and GOI FETs.

The temperature dependence of the drain current can be expressed, starting from (3), as

$$\frac{\partial I_{\mathrm{DS}}}{\partial T}\frac{1}{I_{\mathrm{DS}}} = \frac{\partial v_{\mathrm{inj}}}{\partial T}\frac{1}{v_{\mathrm{inj}}} + \frac{\partial \mathrm{BR}}{\partial T}\frac{1}{\mathrm{BR}} - \frac{\partial V_T}{\partial T}\frac{1}{V_{\mathrm{GS}} - V_T}. \quad (5)$$

It must be noted that while V_T (decreasing with T) and v_{inj} promote a larger ON current at increasing T, the negative temperature coefficient of the ballistic ratio, due to the increasing phonon scattering at increasing T, turns out to be dominant at large gate overdrive, leading to an overall degradation of I_{ON} at large temperature. On the other hand, as the gate overdrive is reduced, the dependence of threshold voltage on the temperature becomes more and more relevant, and the degradation of the current is therefore expected to be reduced substantially until a critical gate voltage is reached, corresponding to a zero-temperature-coefficient condition. Below such critical value, due to the temperature dependence of V_T and v_{inj}, the current is expected to rise due to SHE [20].

2) Subthreshold I–V Characteristics and Leakage Currents: The leakage currents in MOSFETs include the subthreshold drain current I_{OFF} determined by diffusion above the potential energy barrier located at the source channel end, band-to-band tunneling at the drain-substrate junction and gate tunneling current across the gate dielectric.

In the recent years, the gate leakage and subthreshold currents have largely increased as a consequence of the following:

1) reduction of the threshold voltage due to both the scaling strategies and the drain-induced barrier lowering (DIBL);
2) degradation of the subthreshold swing due to the short-channel effects and the increase of the channel doping concentration that enhances the depletion capacitance;
3) dramatic increase of the direct tunneling gate leakage current as a consequence of the scaling of the oxide thickness.

As a consequence, the static power consumption that is used to be negligible in CMOS logic circuits has progressively increased [5], [6], and between the 130- and 65-nm technology nodes, it has reached levels that are comparable with those of the active power dissipation associated to the switching activity in high-performance logic integrated circuits (ICs) [7]. This represents a particularly critical issue not only because the power consumption increases but also because of the positive temperature coefficient of the subthreshold drain current: If a condition is realized under which I_{OFF} provides the dominant contribution to the dissipated power, a positive feedback is set, and a thermal runaway may occur [38].

In this section, we will focus on the temperature-dependent subthreshold current. Both the band-to-band junction leakage current and the gate direct tunneling leakage current, although relevant, do not significantly depend on the temperature. Additional leakage associated to defects in the gate dielectric may present large temperature dependence (e.g., Poole–Frenkel conduction) and play a significant role in the temperature-accelerated degradation of the gate dielectric.

The subthreshold drain leakage current ($V_{\mathrm{GS}} = 0$ V) can be modeled as [39]

$$I_{\mathrm{OFF}} = \frac{W}{L}\mu C_G(m-1)\left(\frac{k_BT}{q}\right)^2 \exp\left(-\frac{qV_T}{mk_BT}\right) \quad (6)$$

where m represents the ideality factor which can be expressed as

$$m = 1 + \gamma\frac{C'}{C_G} \quad (7)$$

where C_G is the gate-to-channel capacitance, C' represents the channel-to-bulk capacitance (C_{DEPL} in the case of bulk MOSFET; $C_{\mathrm{SOI}}C_{\mathrm{BOX}}/(C_{\mathrm{SOI}} + C_{\mathrm{BOX}})$ for the FD SOI MOSFET), and $\gamma(\geq 1)$ accounts for the degradation of the subthreshold swing due to the short-channel effects ($\gamma = 1$ for the long-channel devices).

Starting from (6), the temperature dependence of the subthreshold current can be expressed as

$$\frac{\partial I_{\mathrm{DS-leak}}}{\partial T}\frac{1}{I_{\mathrm{DS-leak}}} = \frac{\partial \mu}{\partial T}\frac{1}{\mu} + \frac{2}{T} - \frac{q}{mk_BT}\frac{\partial V_T}{\partial T} + \frac{qV_T}{mk_BT^2}. \quad (8)$$

Note that $I_{\mathrm{DS-leak}}$ increases with temperature due to the T^2 dependence of the preexponential factor, to the dependence of V_T on temperature, and to the heating-induced degradation of the subthreshold slope [last three terms in the right-hand side (RHS) of (8)]; given the dependence of low-field mobility on temperature in the UTB SOI MOSFETs ($\mu \propto T^{-1.4}$ according to the experiments in [40]), the first term in the RHS of (8) tends to slightly reduce the temperature coefficient of I_{OFF}.

The overall temperature coefficient is positive, and the OFF current can increase by more than one order of magnitude for a 100-K increase of temperature.

The tunneling leakage current is quite relevant as it contributes to increase the static power dissipation, hence contribute to the SHE, but its temperature dependence is negligible. Therefore, it is not involved in tradeoffs related to the heating effects, the only need being to limit its value by adopting gate dielectrics with large enough permittivity in order to achieve the EOT required for high performance, with relatively thick physical thickness.

III. Simulation of SHE in the UTB MOSFETs

A. Simulation Methodology

The electrothermal analysis of the UTB SOI MOSFETs has been performed using the TCAD simulator [41].

Carrier transport is treated via a calibrated drift-diffusion model with quantum corrections introduced by the density-gradient model. In order to obtain realistic values for the simulated current of ultrashort MOSFETs operating in a quasi-ballistic regime, the parameters of the mobility model have been modified in order to reproduce the results of the MC device simulation for ultrashort MOSFETs, following the approach proposed by Bude [42] and Granzner *et al.* [43].

The heat generation is treated conventionally via the $\mathbf{J} \cdot \mathbf{F}$ model (Section II-A), and the heat transport is modeled by the Fourier's law, using the thickness-dependent thermal conductivity calculated according to Liu and Asheghi [15], and shown in Fig. 1 (see Section II-B).

The calibration of the drift-diffusion transport model has been performed at different temperatures by comparison with a full-band self-consistent MC simulator for a 3-D electron gas (3DEG) with corrections to the electrostatic potential in order to include the effect of carrier quantization on the spatial distribution of the inversion charge [44]. Quantum–mechanical corrections are introduced by the effective potential approach proposed in [45].

Besides the phonon scattering, the MC code includes a model for surface roughness (SR) based on the average vertical effective field experienced by the carriers, which has been proposed and validated in [46]. Ionized impurity scattering has been implemented following the usual 3DEG formalism. Electron–plasmon scattering inside the heavily doped regions is also included. This scattering mechanism plays an important role because it thermalizes the particles as they approach the drain. The carrier–plasmon interaction is a very strong inelastic scattering and has to be included when simulating the quasi-ballistic transport since the amount of backscattered carriers depends on the balance between the elastic and inelastic scatterings.

Although the 3DEG is simulated and the quantum effects are introduced through a correction to the electrostatic potential, owing to an accurate calibration of the surface scattering parameters in order to fit the mobility of both the bulk and SOI devices [46], [47], [50], the simulator provides results in good agreement with a multisubband MC simulator consistently accounting for the 2-D electron gas, as demonstrated in [48].

A comparison between DD and MC-calculated I–V characteristics for a 25-nm bulk MOSFET is shown in Figs. 2–4. Subthreshold characteristics are in good agreement at both 300 K and 400 K, proving the consistency of the two methods when the device is biased below the threshold and the transport is dominated by diffusion. Standard drift diffusion underestimates the ON current of the ultrashort devices operating in a quasi-ballistic regime (Figs. 3 and 4). On the other hand, a much better agreement is attained when adopting the drift diffusion with a saturation velocity model calibrated, as suggested by Bude [42] and Granzner *et al.* [43], in order to achieve a good agreement with the MC in terms of the calculated I–V characteristics.

The possibility to achieve a good agreement between the DD and the MC is proven further by Fig. 5, where the ON current normalized to the value corresponding to $T = 300$ K is reported as a function of temperature for three different devices: a PD 25-nm SOI MOSFET and two UTB FD SOI MOSFETs with 25- and 18-nm gates, respectively.

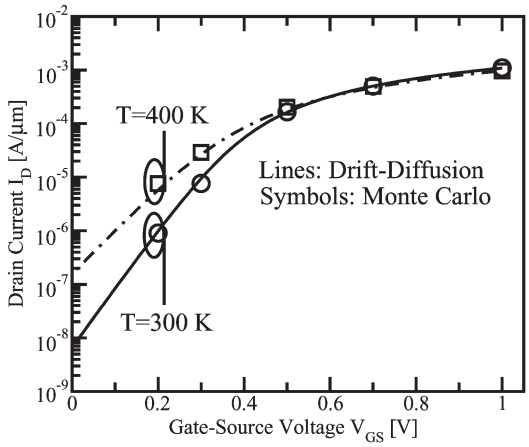

Fig. 2. Transfer characteristics of a 25-nm bulk MOSFET calculated by the (symbols) MC and the (lines) calibrated DD for (circles and solid line) $T = 300$ K and (squares and dot-dashed line) $T = 400$ K; $V_{\rm DS} = 1.0$ V.

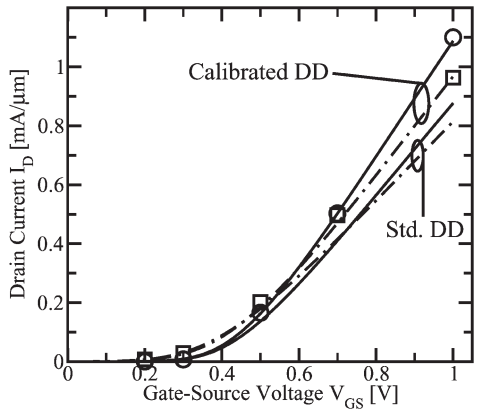

Fig. 3. Linear-scale transfer characteristics of a 25-nm bulk MOSFET calculated by the (symbols) MC and the (lines) standard and calibrated DDs for (circles and solid line) $T = 300$ K and (squares and dot-dashed line) $T = 400$ K; $V_{\rm DS} = 1.0$ V.

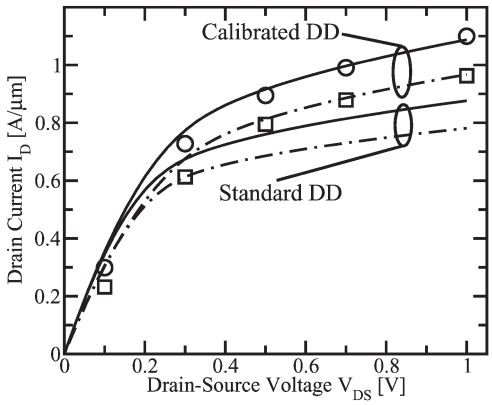

Fig. 4. Output characteristics of a 25-nm bulk MOSFET calculated by the (symbols) MC and the (lines) standard and calibrated DDs for (circles and solid line) $T = 300$ K and (squares and dot-dashed line) $T = 400$ K; $V_{\rm GS} = 1.0$ V.

The temperature dependence of the backscattering coefficient $(1 - r)/(1 + r)$ (3) is shown in Fig. 6. The increase of temperature causes an enhancement of phonon scattering rate and degrades the ballistic transport.

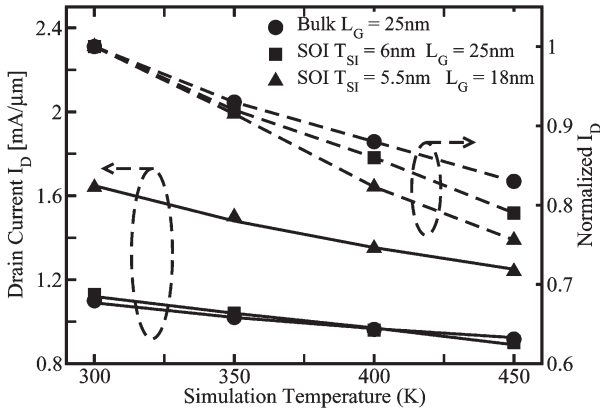

Fig. 5. ON current versus temperature for a 25-nm bulk MOSFET and two UTB FD SOI MOSFETs with 25- and 18-nm gates, respectively, biased at $V_{\rm GS} = V_{\rm DS} = 1.0$ V. Symbols: MC; lines: DD. Temperature dependence is emphasized by the (right scale) normalized current with respect to the value corresponding to 300 K.

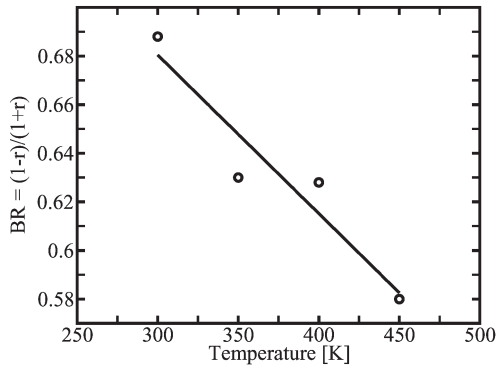

Fig. 6. Temperature dependence of the backscattering coefficient $(1-r)/(1+r)$ (3) evaluated by the MC at the VS of a 25-nm UTB SOI MOSFET biased at $V_{\rm GS} = V_{\rm DS} = 1.0$ V.

Although a good agreement between the DD and the MC can be achieved, it must be noted that it requires a device-dependent tuning of the saturation velocity and of the exponent that describes the temperature dependence of the saturation velocity in the conventional model for high-field-dependent carrier mobility [49]

$$v_{\rm sat} = v_{\rm sat0}\left(\frac{T}{T_0}\right)^{\alpha}. \tag{9}$$

It should be noted that the calibration of the DD affects only the model for $v_{\rm sat}$, whereas all the parameters describing the dependence of mobility on doping concentration and transversal field at the semiconductor/oxide interface are kept at their default values.

Table I reports the optimized values of the parameters for the saturation-velocity model determined in order to reproduce the results of MC simulations for a bulk and two UTB FD SOI MOSFETs with almost undoped silicon body (Figs. 2–5). The parameters obtained for the bulk MOSFET proved adequate also for PD devices with the same gate length and the same doping distribution as the bulk MOSFET, with $T_{\rm SI}$ scaled down to 15 nm. Table I indicates that FD devices with almost undoped channel require larger enhancement of the saturation velocity

TABLE I
PARAMETERS FOR THE VELOCITY-SATURATION MODEL (9), DETERMINED BY COMPARISON WITH THE MC SIMULATION AT DIFFERENT TEMPERATURES. THE PARAMETER SET OBTAINED FOR THE BULK MOSFET PROVED ADEQUATE ALSO FOR THE PD-SOI DEVICES WITH THE SAME DOPING PROFILE AS THE BULK ONE AND WITH THE SILICON THICKNESS SCALED DOWN TO 15 nm

	Bulk 25 nm	UTB-FD SOI 25 nm	UTB-FD SOI 18 nm
v_{SAT} [10^7 cm/s]	1.78	2.11	2.11
α	0.365	0.680	0.920
β	1		

compared with highly doped bulk or PD MOSFETs. This is due to the fact that undoped devices operate closer to the ballistic limit owing to the reduced impact of surface scattering, whereas in the highly doped bulk and PD counterparts, the large amount of depletion charge enhances the vertical field pushing the carriers toward the surface (see the discussion reported in [34]). It is also worth noting that the highly doped devices require a lower value for the parameter α of (9) due to the dominant role played by the temperature-independent SR scattering. A larger value for α is required in the case of the undoped devices in which the current is mainly limited by the temperature-dependent phonon scattering.

1) Simulated Devices: The simulated devices are bulk and SOI (both PD and FD) MOSFETs with a gate length of $L_G = 25$ nm.

A bulk device, assumed as a reference, has been designed according to the ITRS for high-performance transistors and features a highly doped channel plus halos in order to counteract the short-channel effects. The main technological characteristics, such as EOT, gate spacer length, and source/drain junction depth, are those indicated by the ITRS 2005 for the 25-nm high-performance bulk MOSFETs; halo profiles have been tailored in order to comply with the expectations of the roadmap in terms of the OFF current.

Starting from the reference bulk MOSFET, PD-SOI transistors have been designed which feature the same channel, halo and S/D doping profiles, a silicon-film thickness $T_{\rm SI}$ of 50, 25, and 15 nm, a nominal extension length $L_{\rm EXT} = 13.75$ nm, and a BOX with nominal thickness $T_{\rm BOX} = 50$ nm.

An FD SOI MOSFET has been included in the comparison. This device features a lightly doped ultrathin silicon body over a 50-nm BOX. $T_{\rm SI}$ is set to 6 nm, as required, in order to limit the DIBL and the OFF current.

The values of geometrical parameters, such as the length of the S/D extension region, the thickness of the elevated S/D regions $(T_{\rm SD})$, and $T_{\rm BOX}$, have been varied with respect to the nominal ones because these may have an impact on the SHE effects, as analyzed in [21] by a 1-D analytical thermal model.

A sketch of the typical 2-D cross section of the simulated SOI devices is shown in Fig. 7, and the main characteristics of the simulated SOI devices are summarized in Table II.

IV. ANALYSIS OF SHE IN THE UTB SOI MOSFETS

This section reports the results of self-consistent electrothermal simulations of the SOI MOSFETs and highlights the main

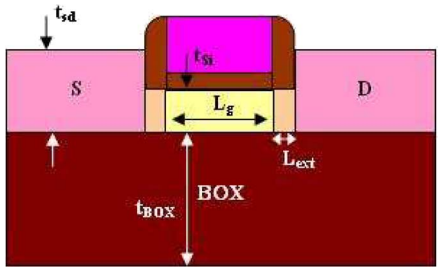

Fig. 7. Two-dimensional sketch of the simulated SOI devices.

TABLE II
MAIN PARAMETERS OF THE SIMULATED SOI DEVICES

Gate Length [nm]	L_G=25 nm			
Rel. Dielec. Const.	7			
T_{OX} / EOT [nm]	1.6/0.9			
SOI thickn. T_{SI} [nm]	50	25	15	6
BOX thickn. T_{BOX} [nm]	25, 50, 150			
Elev. S/D thickn. T_{SD} [nm]	T_{SI}			6-30
S/D ext. length L_{EXT} [nm]	13.75			8-50
Channel doping [cm^{-3}]	3×10^{18} + halo			3×10^{15}
Gate work funct. [eV]	4.06	4.08	4.26	4.72

issues related to SHE in these devices. The dependence of the SHE effects on technological parameters is analyzed in order to point out the need for a device design explicitly taking into account SHE.

The choice of appropriate thermal boundary conditions is crucial in order to get significant results. In this paper, an isothermal boundary condition at 300 K is always assumed at the contact to the silicon bulk region underneath the back oxide, thus assuming an ideal heat sink at the back of the dice. An adiabatic thermal boundary condition is assumed at the lateral boundaries of the simulated structure. The intermetal and passivation dielectrics are assumed to be thick enough to impede heat dissipation toward the upper surface of the IC. The simulation grid is large enough to minimize the impact of boundary conditions (14 μm large and 20 μm thick).

The thermal boundary conditions at the drain, source, and gate electrodes are difficult to set unless a realistic interconnect structure is assumed for a given specific circuit application (see, e.g., [27]). In this paper, we consider two extreme limit cases: 1) adiabatic boundary conditions at the contacts with no heat conduction through the interconnects, representing the worst possible case in terms of SHE; and 2) lumped thermal resistance connecting the device terminal to a 300 K isothermal boundary condition. The best possible case (minimum heating) is that of a minimum-width device ($W = 6\,L_G$ according to the ITRS) connected to very long metal/polysilicon wires exchanging heat in the vertical direction toward the substrate heat sink through a stack of intermetal insulator, back oxide, and silicon substrate. The lumped resistance representative of the cooling interconnect is calculated according to the theory of heat transport along extended surfaces [51]. In order to consider the limit case of maximum possible cooling, the interconnects are assumed to be much longer than the so-called healing length, which is the characteristic length for exponential temperature attenuation due to heat exchange with

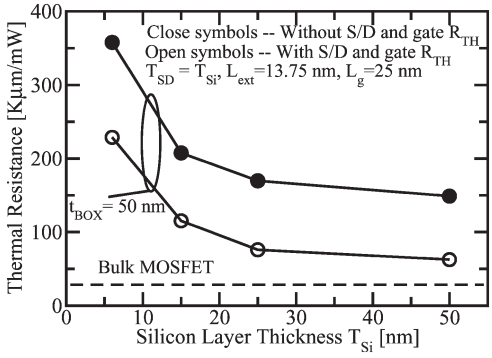

Fig. 8. Device thermal resistance versus silicon layer thickness $T_{\rm SI}$. Open symbols: Cooling effect through source, drain, and gate included. Filled symbols: Adiabatic source, drain, and gate contacts. Horizontal dashed line: $R_{\rm th}$ for the 25-nm bulk MOSFET.

the ideal sink through the insulator–semiconductor stack [51], leading to the following expression for the lumped thermal resistance [17]:

$$R_{\rm TH-int.} = W_m^{-1}\sqrt{\frac{st_m k_i k_m}{t_i}} \tag{10}$$

where W_m is the width of the interconnect line, k_i and k_m are the thermal conductivities of the insulator beneath the interconnect and of the interconnect metal (polysilicon) line, respectively, t_i and t_m are the thicknesses of the insulator layer and of the interconnect line, respectively, and s is a correction factor accounting for thermal coupling between the densely packed interconnect lines, which is calculated according to Chiang *et al.* [52]. The values for the geometrical parameters of (10) are assumed according to the ITRS.

An additional surface thermal resistance of 2×10^{-4}K$\cdot$cm^2/W is added to the gate contact in order to account for surface effects at both the silicon-dielectric and dielectric-gate interfaces [53], [54].

The calculated thermal resistance $(R_{\rm th})$ for the UTB SOI MOSFETs is shown in Fig. 8 as a function of the thickness of the silicon layer. As we gradually move from the highly doped PD devices to the UTB MOSFET with low-doped channel and $T_{\rm SI} = 6$ nm, the device thermal resistance largely increases due to the reduction of the thermal conductivity occurring as a consequence of the increasing role of the phonon boundary scattering, according to the discussion in Section II-B and to the references therein. By neglecting the cooling effect through the drain, source and gate interconnects lead to a significant increase of the device thermal resistance. The SHE is larger in the SOI MOSFETs compared with the bulk transistor as the latter one is effectively cooled, owing to the high thermal-conductivity path along the silicon bulk toward the ideal sink placed at the substrate contact.

The calculated thermal resistance $(R_{\rm th})$ for the UTB SOI MOSFETs is shown in Fig. 9 as a function of the gate length: Shorter gate lengths translate into a more compact device with smaller cross section on the plane of the silicon/back oxide interface and, therefore, less efficient cooling through the back oxide.

Fig. 10 shows the calculated thermal resistance $(R_{\rm th})$ for the UTB SOI MOSFETs as a function of the thickness of the

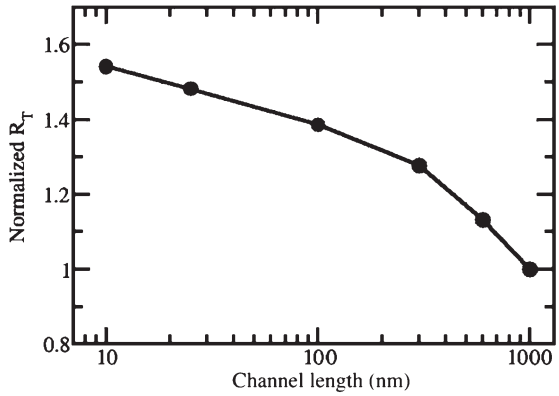

Fig. 9. Device thermal resistance versus L_G.

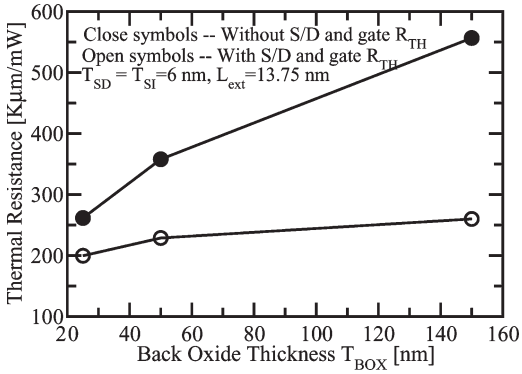

Fig. 10. Device thermal resistance versus back-oxide thickness T_{BOX}. Open symbols: Cooling effect through source, drain, and gate included. Filled symbols: Adiabatic source, drain, and gate contacts. $T_{\mathrm{SI}} = T_{\mathrm{BOX}} = 6$ nm.

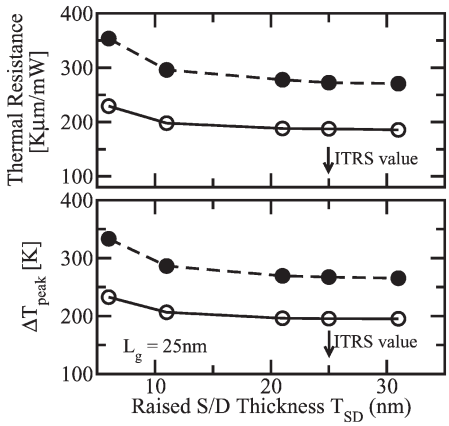

Fig. 11. (Upper graph) Device thermal resistance and maximum temperature rise at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 1.1$ V versus height of the raised S/D region L_{EXT}; the arrow indicates the nominal value of T_{SD} prescribed by the ITRS 2005. $T_{\mathrm{SI}} = 6$ nm, $T_{\mathrm{BOX}} = 50$ nm, and $L_{\mathrm{EXT}} = 13.75$ nm.

back-oxide layer. Increasing the back oxide leads to larger thermal resistance due to the low thermal conductivity of SiO_2. The dependence on T_{BOX} is larger in the case of the adiabatic thermal boundary condition at the device contacts.

Figs. 11 and 12 show the calculated device thermal resistance and the peak temperature rise under I_{ON} conditions, as functions of the height of the raised S/D region and of the length

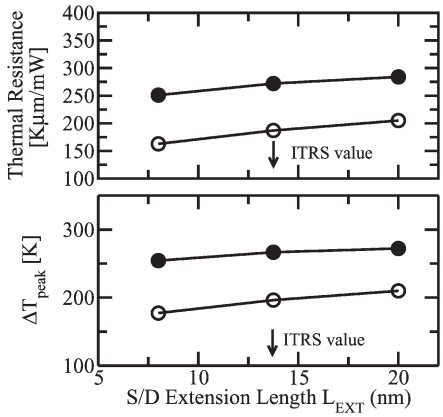

Fig. 12. (Upper graph) Device thermal resistance and maximum temperature rise at $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 1.1$ V versus length of the S/D extension region L_{EXT}; the arrow indicates the nominal value of L_{EXT} prescribed by the ITRS 2005. $T_{\mathrm{SI}} = 6$ nm, $T_{\mathrm{BOX}} = 50$ nm, and $T_{\mathrm{SD}} = 25$ nm.

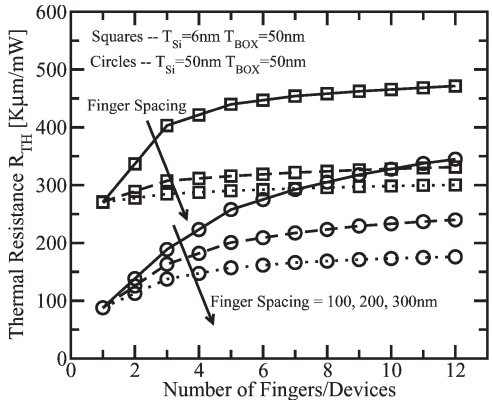

Fig. 13. Device thermal resistance versus number of fingers for (circles) PD and (squares) FD 25-nm SOI MOSFETs and different packing densities. R_{th} rapidly increases with the number of fingers and saturates for the number of fingers on the order of ten.

of the S/D extension region, respectively. These dependences were investigated in [21] by means of a 1-D thermal model that neglects the heat conduction through the BOX in the vertical direction toward the silicon substrate beneath the back oxide. Our results based on a more realistic 2-D heat-conduction simulation show that the dependence on these geometrical parameters on SHE is less relevant than predicted by Pop *et al.* [21].

Digital circuits require tight device packing, whereas analog design requires multifinger layout; adjacent devices/fingers do thermally interact due to the lateral heat spreading, leading to an enhanced SHE [25]. In this paper, the effect of the multifinger layout is investigated by simulating a single-finger device and calculating the corresponding lateral temperature profile evaluated in the silicon at the depth of 1 nm below the silicon surface. The profile for N fingers with a given finger spacing W_{spac} is obtained by superposition of N temperature profiles spaced by W_{spac}. In Fig. 13, the device thermal resistance is shown as a function of the number of fingers for PD and FD 25-nm SOI MOSFETs and different packing densities. R_{th} rapidly increases with the number of fingers, the impact of multifinger layout being larger for larger packing density (smaller spacing).

The PD MOSFET is sensitive to the multifinger layout because of the relatively large lateral thermal conductivity in the 50-nm-thick silicon layer, leading to large thermal healing length and interaction among the different fingers. The UTB MOSFET is not sensitive to the multifinger layout if the spacing is larger than 200 nm because, due to the degraded thermal conductivity, the thermal healing length is shorter than $W_{\rm spac}$; when the spacing is reduced below the healing length (e.g., $W_{\rm spac} < 200$ nm), the thermal interaction between adjacent fingers becomes very significant due to the very large carrier heating that takes place in these ultrathin devices.

A. Implications of SHE on Digital Operation

So far, we have investigated SHE for devices biased at $V_{\rm GS} = {\rm V_{DS}} = 1.1$ V, corresponding to dissipation power $P_{\rm DC} = V_{\rm CC} I_{\rm ON}$. Devices of digital circuits undergo successive switching transients contributing to dynamic power dissipation interleaved by OFF-state periods contributing to static power dissipation and device heating due to the gate tunneling and drain subthreshold leakage currents. Therefore, actual SHE corresponds to a lower power dissipation than under dc $I_{\rm ON}$ conditions.

In [55], the dynamic dissipated power under realistic switching conditions has been estimated to $P_{\rm Dyn} = 0.13 \cdot P_{\rm DC}$. In modern high-performance digital ICs, the contribution of the static power associated to the leakage currents has risen to become comparable with $P_{\rm Dyn}$ [7]. In order to estimate the temperature rise under operating conditions, we assume a total average dissipated power $P_{\rm DISS} = 2 \cdot P_{\rm Dyn} = 0.26\ P_{\rm DC}$. The temperature rise associated to such power-dissipation level in SOI MOSFETs has been estimated and is shown in Fig. 14 as a function of $T_{\rm SI}$. The average temperature rise can surpass 63 K in the FD MOSFET unless enough cooling through the contact's interconnects occurs. This SHE-induced temperature rise leads to 90-°C operating temperature for 27-°C ambient temperature, corresponding to the upper limit set by the ITRS, dictated by reliability concerns. In fact, both the lifetime of metallizations and the time to breakdown (TBD) of the gate dielectric are strongly degraded at large temperatures [25], [56], with temperature dependence of TBD becoming more dramatic as the thickness of the gate dielectric is scaled down into the nanometer regime [56]. The temperature-activated degradation of TBD of the gate dielectric is related to the large temperature dependence of the defect-assisted gate leakage mechanisms such as Poole–Frenkel conduction.

Fig. 15 shows the degradation of the ON current due to the SHE calculated by isothermal simulations performed at the average temperature estimated previously (Fig. 14), and it also shows that the degradation, although significant, is not dramatic and would not lead to a relevant reduction of the performance of digital circuits. A 10% degradation of the ON current is predicted in the case of the thinnest silicon layer; this is significantly larger compared with [55] where a similar analysis performed for 0.12-μm MOSFETs led to an estimated 2% reduction of the ON current due to heating that occurs under switching conditions. The much larger impact of SHE in the 25-nm MOSFETs of this paper can be explained by the reduction of the gate length and by the degradation of the thermal conductance in thin silicon films, and it was qualitatively anticipated in [55]. Pulsed I–V measurements compared with the dc measurements [19], [55] typically indicate a 15%–20% degradation of the ON current due to the SHE under the dc condition at $V_{\rm GS} = V_{\rm DS} = V_{\rm DD}$.

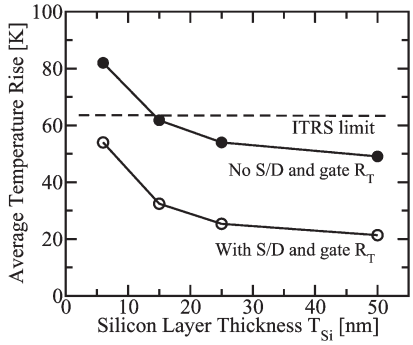

Fig. 14. Average temperature rise due to the SHE in the UTB SOI MOSFETs under a dissipation condition $P_{\rm DISS} = 0.26\ V_{\rm CC} I_{\rm ON}$, taking account for the average dynamic power dissipation and the leakage static power dissipation for a high-performance digital IC.

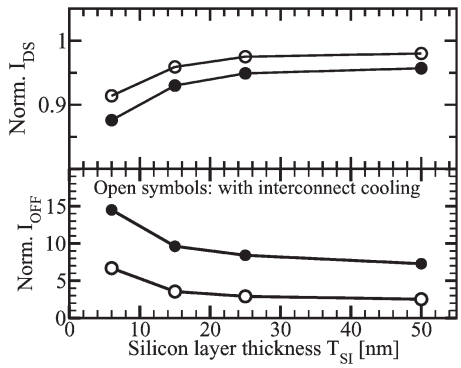

Fig. 15. ON current and drain OFF current normalized to the 300-K values for the UTB SOI MOSFETs under a dissipation condition $P_{\rm DISS} = 0.25\ V_{\rm CC} I_{\rm ON}$, taking account for the average dynamic power dissipation and the static power dissipation for a high-performance digital IC.

The impact of SHE on the thermally activated OFF current is shown in Fig. 15; the temperature rise leads to a large increase of the drain current for the nominally OFF device, leading to an increased power dissipation under static conditions.

B. Implications of SHE on Analog Operation

SHE is expected to have an impact on the operation of analog circuits fabricated with SOI technologies, and an analysis of such effects has been given in [57] with reference to a 0.7-μm SOI technology.

In this section, we analyze SHE in the 25-nm PD-SOI n-MOSFET with $T_{\rm SI} = 50$ nm. Device heating has an impact on the small-signal parameters such as transconductance g_m and output conductance $g_{\rm ds}$. In particular, the dependence of $g_{\rm ds}$ on SHE has been the subject of specific analysis because the frequency dependence of this parameter can be employed to estimate the device heating [18], [20], [58].

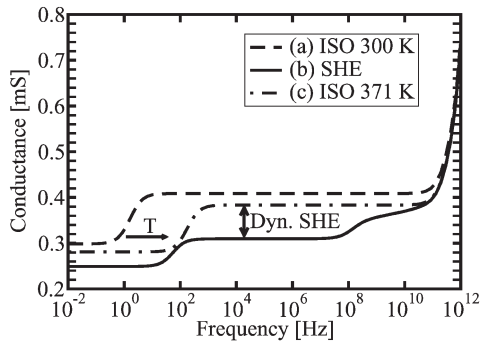

Fig. 16. Frequency dependence of the output conductance of the PD-SOI 25-nm MOSFET ($T_{\rm SI} = T_{\rm BOX} = 50$ nm), biased at $V_{\rm GS} = V_{\rm DS} = 1.0$ V calculated for three different cases: 1) isothermal simulation at $T = 300$ K; 2) nonisothermal simulation accounting for SHE; and 3) isothermal simulation at $T = 371$ K, the average temperature in the device under nonisothermal conditions.

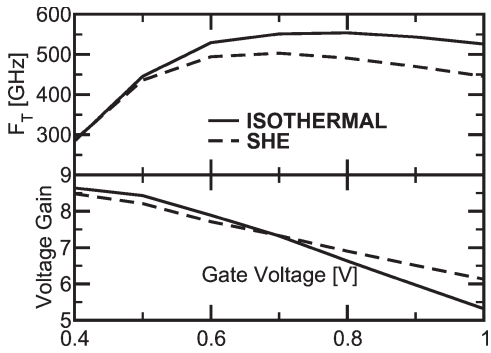

Fig. 17. Open-circuit voltage gain and cutoff frequency F_T as a function of gate voltage for the PD 25-nm SOI MOSFET ($T_{\rm SI} = 50$ nm). The SHE hardly affects A_V while it degrades the cutoff frequency F_T.

In Fig. 16, the frequency dispersion of the output conductance of the PD-SOI 25-nm MOSFET, biased at $V_{\rm GS} = V_{\rm DS} = 1.0$ V, is shown for three different cases:

1) isothermal simulation at $T = 300$ K;
2) nonisothermal simulation accounting for SHE;
3) isothermal simulation at $T = 371$ K, the average temperature in the device under nonisothermal conditions.

We may notice the existence of a frequency dependence in the isothermal case due to the drain–source coupling through the bulk region below the back oxide. This effect has been analyzed by Kilchytska *et al.* [59], [60]. According to the model proposed in [59] and [60], this coupling involves a capacitive voltage divider that includes the frequency-dependent substrate capacitance $C_{\rm SUB}$. The frequency dispersion of $C_{\rm SUB}$ leads to two transitions in the $g_{\rm ds}$ versus frequency characteristic. The first one occurs at low frequency and is related to the finite response time of minority carriers in the substrate. A second transition occurs at frequencies larger than the inverse dielectric-relaxation time. At such large frequencies, even the majority carriers cannot follow the signal, leading to a drop of $C_{\rm SUB}$ and, as a consequence, to a significant enhancement of the output conductance [59], [60]. By increasing the device temperature above 300 K, as in cases 2) and 3), this low-frequency transition moves at larger frequency due to the temperature dependence of generation–recombination processes. The differences between cases 2) and 3) are related to ac thermal effects that lead to a further reduction of $g_{\rm ds}$ in the nonisothermal case compared with the isothermal one at the same average temperature. An additional transition occurs in 2) at approximately 10^8 Hz because the ac thermal effects are low-pass-filtered due to the finite device thermal time constant. At larger frequencies, the three $g_{\rm ds}$-frequency curves tend to merge due to the temperature-independent high-frequency transition.

In addition to a reduction of the output conductance, the SHE leads to a degradation of the transconductance, which is mainly due to an enhancement of the scattering rate inside the channel and in the S/D regions.

Both parameters have an impact on the small-signal open-circuit voltage gain in common-source configuration $A_v \approx g_m/g_{\rm ds}$. Fig. 17 shows that the voltage gain is affected by SHE, leading to a slight decrease at low gate voltage overdrive and to a significant increase at relatively large overdrive, as the decrease of $g_{\rm ds}$ prevails over the degradation of g_m. In [57], the simulation of a common-source voltage amplifier based on a 0.7-μm PD-SOI MOSFET predicted a 0.1-dB reduction of the voltage gain due to SHE.

As shown in Fig. 17, the cutoff frequency is largely degraded by SHE due to the degradation of device transconductance.

V. Conclusion

Extensive thermal analysis of the SOI n-MOSFETs with $L_G = 25$ nm has been performed using the calibrated DD and thermal-transport models. The large power consumption and confined device structures result in large SHE, increasing as silicon thickness is reduced and gate length is scaled down. The thermal healing length reduces as the SOI layer is thinned down, thus reducing the thermal coupling between devices. Using thin BOX seems to be necessary in order to reduce the SHE, even if part of the benefits from the SOI is sacrificed. Using larger elevated S/D and short S/D extensions can marginally mitigate SHE. The SHE's effect on device performance is not obvious as the degradation of the ON current is not dramatic. However, the high operating temperatures in the SOI device will affect the device reliability severely.

The effects of SHE on the ac small-signal performance of n-MOSFETs have been investigated for the PD devices, showing that the open-circuit voltage gain is marginally affected for relatively low gate voltage overdrive while the cutoff frequency is severely degraded.

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