Analysis of Single-Trap-Induced Random Telegraph Noise and Its Interaction With Work Function Variation for Tunnel FET

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***Abstract*— This paper analyzes the impacts of a single acceptor-type and donor-type interface trap induced random telegraph noise (RTN) on tunnel FET (TFET) devices and its interaction with work function variation (WFV) using atomistic 3-D TCAD simulations. Significant RTN amplitude ($\Delta I_D/I_D$) is observed for a single acceptor trap near the tunneling junction, whereas a donor trap is found to cause more severe impact over a broader region across the channel region. In addition, several device design parameters that can be used to improve TFET subthreshold characteristics (thinner equivalent oxide thickness or longer L_{eff}) are found to increase the susceptibility to RTN. Our results indicate that under WFV, TFET exhibits weaker correlation between I_{ON} and I_{OFF} than that in the conventional MOSFET counterpart. In the presence of WFV, the RTN amplitude can be enhanced or reduced depending on the type of the trap and the composition/orientation of metal-gate grain.**

***Index Terms*— Random telegraph noise (RTN), tunnel FET (TFET), variability, work function variation (WFV).**

I. Introduction

VOLTAGE scaling is an effective approach to reduce the static and dynamic power consumptions for ultra-low-power applications. However, the reduction in supply voltage leads to exponential increase in circuit delay and variability, and eventually impedes the applicability of low-voltage design. To achieve satisfactory circuit performance at low supply voltage, innovative transistor structures with adequate I_{ON} while maintaining low I_{OFF} are required. Tunnel FET (TFET), which utilizes interband tunneling as the major conduction mechanism, has attracted much attention because of its capability to surmount the thermionic limitation and provide superior switching characteristics (such as steeper subthreshold swing (S.S.) and superior $I_{\text{ON}}/I_{\text{OFF}}$) than the conventional MOSFET counterparts [1]–[6].

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With the scaling of device dimensions, random variations have emerged as crucial concerns [7]–[11] and may undermine the viability and advantages of TFET. In particular, Avci *et al.* [11] pointed out that the work function variation (WFV) associated with the grain granularity characteristic of metal gate has significant impact on TFET devices. In addition, the random telegraph noise (RTN) caused by the trapping/detrapping of carriers at the interface trap is becoming an important source of fluctuation for extremely scaled MOSFETs [12]–[15]. The impact of RTN on TFET, however, is rarely studied and merits investigation. In this paper, we provide an in-depth assessment of single-trap-induced RTN for silicon TFET devices using 3-D atomistic TCAD simulations [16]. In addition, the impact of WFV on TFET devices is analyzed and combined with RTN simultaneously to evaluate the interaction between these two variation sources. The rest of this paper is organized as follows. Section II describes the operation of TFET and the simulation frameworks used for the analysis of RTN and WFV. In Section III, we examine the dependences of RTN amplitude on trap location and device geometry for a single acceptor-type or donor-type trap placed across the gate insulator/silicon interface of TFET. In Section IV, atomistic 3-D Monte Carlo simulations are performed to statistically analyze the impact of WFV on TFET and investigate its interaction with RTN. The underlying mechanisms that govern the behaviors of TFET under RTN and WFV are presented. Finally, the conclusions are drawn in Section V.

II. Device Operation and Simulation Framework

The inset of Fig. 1(a) shows the band diagrams of a reversely-biased p-i-n TFET operating in ON/OFF states. For an n-type TFET in OFF state, the energy level of valence band in the source region (p-type doped) is lower than the conduction band in the channel region (intrinsically doped), thus yielding no empty states available in the channel region for electrons tunneling from the source. With increasing gate bias, the conduction band of the channel region is coupled down to below the valence band of the source region hence significant tunneling occurs with the decrease in critical tunneling length. For the analysis of TFET, the nonlocal band-to-band tunneling model that accounts for arbitrary tunneling barrier with nonuniform electric field is employed

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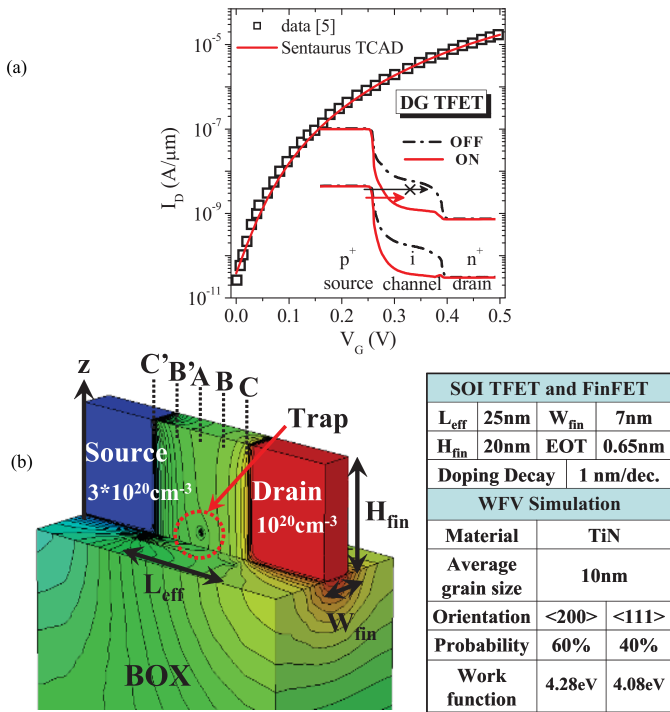

SOI TFET and FinFET			
L_{eff}	25nm	W_{fin}	7nm
H_{fin}	20nm	EOT	0.65nm
Doping Decay		1 nm/dec.	
WFV Simulation			
Material		TiN	
Average grain size		10nm	
Orientation		<200>	<111>
Probability		60%	40%
Work function		4.28eV	4.08eV

Fig. 1. (a) Calibration of the nonlocal tunneling model with [5] for DG TFET and (b) the schematic of TFET with perturbed potential by a charged trap. The inset in (a) illustrates the energy band profiles of TFET in ON/OFF states and the table shown in (b) summarizes the geometries for TFET and FinFET devices, and parameters used for the simulation of WFV.

[16] and [17]. In this framework, the tunneling paths are dynamically determined according to the gradient of energy band and the parameters used in the nonlocal tunneling model are calibrated with the data in [5] for double-gate (DG) TFET Fig. 1(a).

In this paper, the geometries of SOI TFET structures (Fig. 1(b)) and operating bias conditions similar to the case in [5] are used. 3-D TCAD atomistic simulation [14] that is adequately calibrated with the published experimental data is adopted to consider the impact of RTN caused by a single localized trap, and the resulting distorted potential contour is shown in Fig. 1(b). In addition, the meshes used in this paper are strategically refined in the tunneling region and near the trap location to enhance the computational accuracy without severely degrading the numerical efficiency for atomistic 3-D simulations. In this paper, the static change in drain current is considered for an acceptor-type (carry a negative charge in trapped state) or a donor-type (carry a positive charge in detrapped state) interface trap, whereas the dynamic transition determined by the emission/capture time of conducting carrier is ignored. Thus, the results represent the amplitude fluctuation between the limiting end cases. For the analysis of WFV, the shapes of polycrystalline grains, with the work function of each grain depending on its orientation is considered using a novel Voronoi approach to imitate irregular grain patterns [18]. In our atomistic simulations, TiN metal gate material composed of two distinct grain orientations with 60% and 40% occurring probabilities and work function difference of 0.2 eV is employed with average grain size = 10 nm (summarized in Fig. 1(b)) [19].

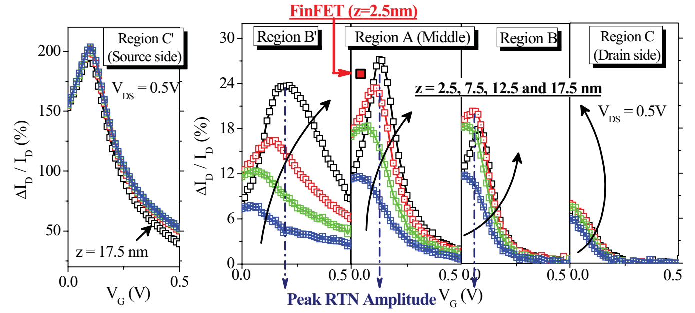

Fig. 2. Dependence of RTN amplitude ($\Delta I_D/I_D$) on the location of a single acceptor trap at sidewall insulator/silicon interface. The positions of the red square (in Region A) and tunneling junction (in Region C′) exhibit the largest impact for FinFET and TFET devices, respectively.

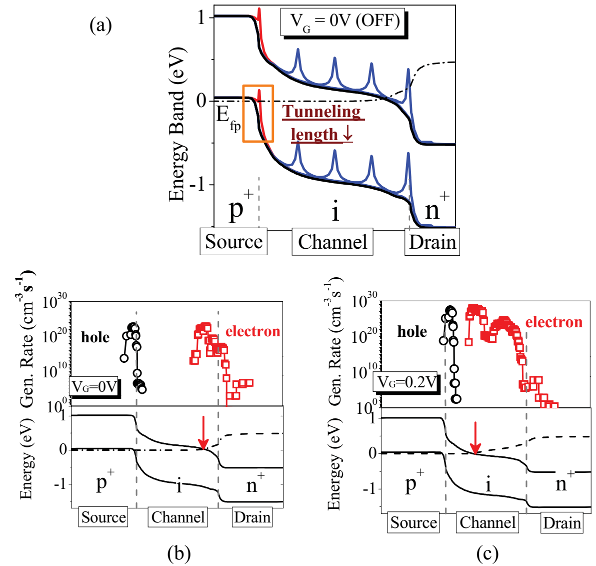

Fig. 3. Energy band diagrams along the channel length direction with (a) a single acceptor trap placed at various locations and the electron/hole band-to-band generation rate at (b) $V_G = 0$ V and (c) $V_G = 0.2$ V without RTN. The profiles for band diagram and generation rate are probed at the insulator/silicon interface and $z = 0.5\ H_{\text{fin}}$ (z-axis is along the fin height direction defined in Fig. 1(b)).

III. Impact of RTN on TFET Devices

Fig. 2 shows the dependence of RTN amplitude ($\Delta I_D/I_D$) on the position of a single acceptor-type trap placed across the insulator/silicon sidewall interface. Because of the exponential dependence of the tunneling current on critical tunneling path [2], significant impact of RTN is observed for trap located near the tunneling junction (Region C′ defined in Fig. 1(b)) and the influence decreases toward the drain side. Fig. 3(a) shows the energy band diagrams of TFET along the channel length direction with a trapped acceptor-type trap at various locations. As can be seen, in the presence of a negatively-charged trap near the tunneling junction, the band peaks up in the vicinity of the trap location, thus reducing the tunneling length and resulting in large RTN impact. On the other hand, for trap away from the tunneling junction, the critical tunneling length is unchanged (Fig. 3(a)). In this case, the RTN amplitude depends on the distance between the charged trap and the spot with significant electron generation rate (similar to the

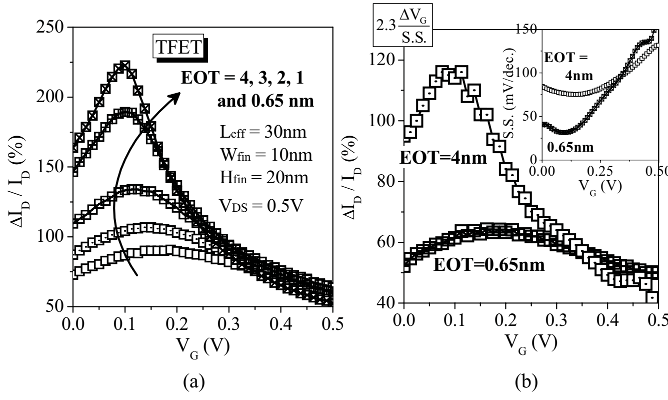

Fig. 4. Comparison of RTN amplitude for TFET with various EOTs calculated from (a) atomistic 3-D TCAD simulations and (b) simplified model. The simple model can qualitatively describe the trends predicted by the TCAD simulations for a single acceptor trap placed at the tunneling junction.

case for the conventional FinFET [14]). Therefore, the shift of the position with significant electron generation rate toward the tunneling junction at higher V_G (Fig. 3(b) and (c)) results in the larger RTN amplitude. It can be seen that the peak of RTN amplitude (indicated by the dashed arrow in Fig. 2) occurs at higher gate biases for trap closer to the tunneling junction (Region B′) than those in regions away from the tunneling junction (Regions A and B). In addition, larger RTN amplitude is observed for trap located around the top of the fin (z-direction) because of higher electric field to generate more electrons near the top of the fin. Compared with the conventional FinFET device (see the red square in Fig. 2 that marks the largest impact of RTN for the conventional FinFET) [14], TFET, with its strong dependence of current on the critical tunneling length, exhibits higher susceptibility to RTN for a single trap located near the tunneling junction because of the reduction of tunneling length. It should be noted that in TFET, the RTN amplitude can be more than 100% because of the increase in current when the trap is occupied.

In the following, the impacts of several important device parameters such as equivalent oxide thickness (EOT) and gate length ($L_{\rm eff}$) on RTN are examined. Fig. 4 shows the dependence of RTN amplitude on V_G for TFET with various EOTs. The single acceptor-type trap is placed at the tunneling junction for the worst-case condition. As can be seen, because of the screening of charged trap by the increasing conducting carriers, the RTN amplitude decreases with increasing V_G similar to the conventional MOSFET [13]–[15]. In Fig. 4(b), a simple model is proposed to qualitatively describe the behavior of RTN amplitude and for analyzing the underlying factors that determine the RTN amplitude in TFET. The model is expressed as follows [14], [20]:

$$\frac{\Delta I_D}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial E_S}\frac{\partial E_S}{\partial V_G} = 2.3\frac{\Delta V_G}{\text{S.S.}} \tag{1}$$

that is proportional to the trap-induced V_G shift (ΔV_G) and inversely proportional to the S.S. Consistent with the atomistic 3-D simulations shown in Fig. 4(a), TFET with thinner EOT suffers more severe RTN impact because of the significant

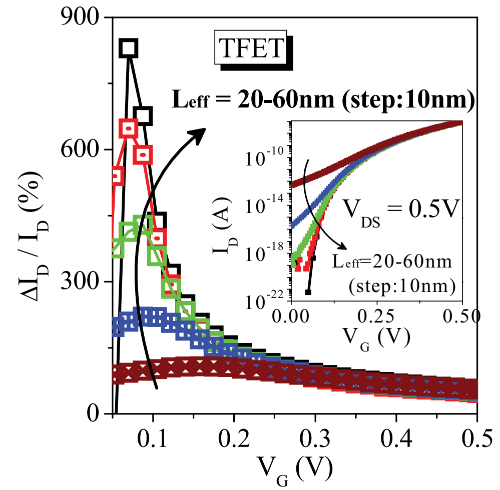

Fig. 5. Impact of $L_{\rm eff}$ on RTN amplitude for TFET with a single acceptor-trap placed at the tunneling junction. The inset shows the I_D–V_G characteristics of TFETs under various $L_{\rm eff}$ with $W_{\rm fin} = 10$ nm, $H_{\rm fin} = 20$ nm, and EOT $= 0.65$ nm.

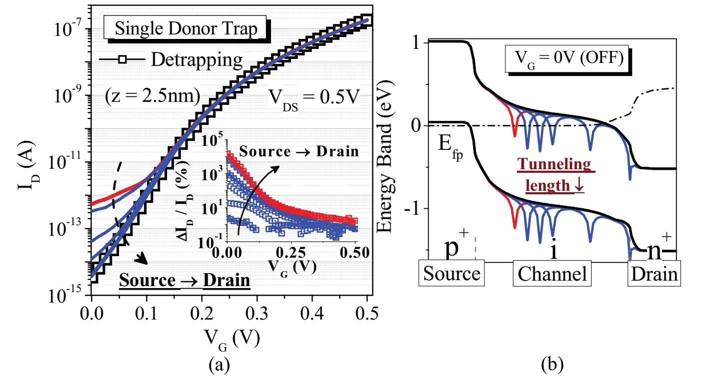

Fig. 6. (a) Impact of a single donor-type trap placed across the TFET sidewall insulator/silicon interface along the channel length direction and (b) the corresponding energy band diagrams at $V_G = 0$ V.

improvement in S.S. as predicted by the simplified model (Fig. 4(b)).

In Fig. 5, the dependence of RTN amplitude on V_G for TFET with various $L_{\rm eff}$ is shown. It can be seen that longer $L_{\rm eff}$ which enables steeper S.S. exhibits larger RTN amplitude. Simultaneously, it is noted that the scaling of $L_{\rm eff}$ suffers less impact from RTN (at the expense of poor subthreshold characteristics), a trend opposite to that in the conventional MOSFET for which the RTN amplitude is inversely proportional to the device size [12] and [13]. The significant RTN amplitude (over several hundreds of percent) observed in Figs. 4(a) and 5 show the substantial increase in current caused by an occupied interface trap located near the tunneling junction.

Fig. 6(a) shows the $I_D - V_G$ characteristics of TFET with a single donor-type trap (carry a positive charge in detrapped state) placed across the TFET sidewall insulator/silicon interface. As can be seen, drastic degradations in $I_{\rm OFF}$ and large RTN amplitude (inset of Fig. 6(a)) are observed. In contrast with the case for an acceptor trap where significant impact occurs only near the tunneling junction (Fig. 2), a donor-

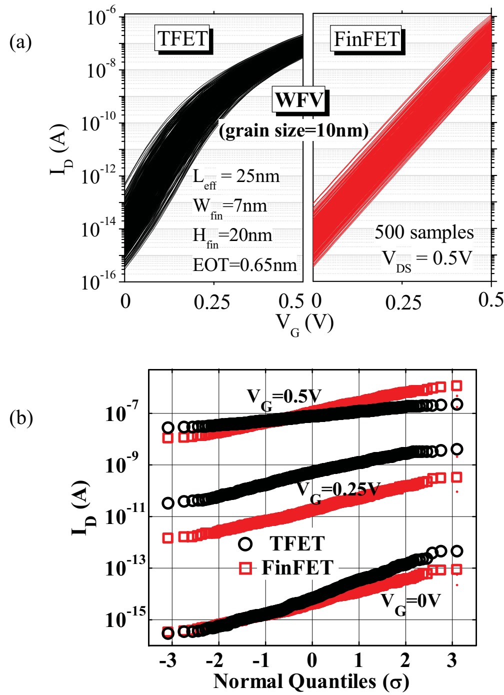

Fig. 7. Comparisons of (a) I_D–V_G dispersions and (b) the cumulative probability of I_D at $V_G = 0, 0.25$ and 0.5 V for TFET and FinFET in the presence of WFV (average metal-gate grain size = 10 nm [19]).

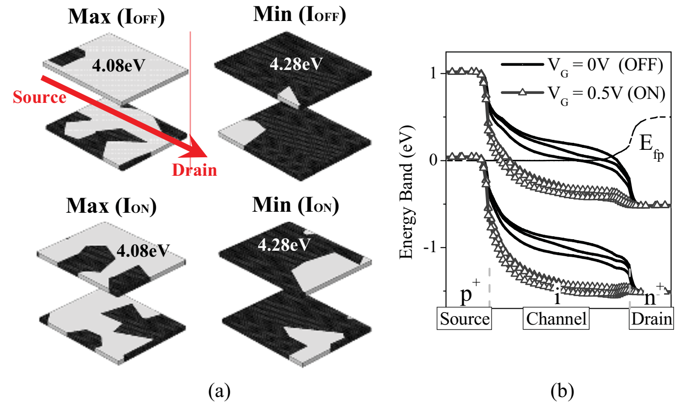

Fig. 8. (a) The metal-gate grain patterns corresponding to the maximum/minimum I_{ON} and I_{OFF} (gray and black region stands for the grain with smaller and higher work function, respectively), and (b) the extreme energy band diagrams (maximum and minimum I_{ON} and I_{OFF}) in ON/OFF states under WFV. The tunneling paths are severely impacted in OFF state, thus resulting in broader I_D dispersion than that in ON state.

type trap causes severe impact over broad region across the channel region with considerably larger RTN amplitude. Fig. 6(b) shows the corresponding band diagrams of TFET along the channel length direction with a single donor-type trap at various locations. The critical tunneling length is altered even for the cases with trap located away from the tunneling junction, thus making TFET more susceptible to the RTN induced by the donor-type trap.

IV. Impact of WFV and Its Interaction With RTN

In this section, we evaluate the impact of WFV on the characteristics of TFET and incorporate a single acceptor-type or donor-type trap in our simulations to examine the resulting microscopic interactions between these two variation sources. Fig. 7 shows the impact of WFV on the I_D–V_G characteristics for TFET and FinFET devices under identical I_{OFF} and metal-gate grain patterns. 3-D atomistic Monte-Carlo simulations are performed with an ensemble of 500 microscopically different transistors to capture the statistical behavior of WFV. Fig. 7 shows that because of its steeper S.S. at low V_G, TFET enables superior current driving capability compared with the FinFET counterpart before the saturation of TFET current around $V_G = 0.5$ V. Meanwhile, it is noted that the I_D fluctuation of TFET decreases with increasing V_G which is similar to the conventional FinFET but with different conducting mechanism from TFET device.

Fig. 8(b) shows the corresponding ON-/OFF-state energy band diagrams under the extreme conditions of WFV (i.e., devices with maximum and minimum I_{ON} and I_{OFF}) in Fig. 7(a). As can be seen, the inclusion of metal-gate WFV leads to dispersions in the energy bands in the channel region and alters the critical path for tunneling. The noticeable change in the tunneling path during OFF state gives rise to the broader I_{OFF} distribution, whereas the increase in V_G pushes the critical path to the tunneling junction where the influence from WFV tends to be less, thus resulting in smaller I_{ON} variation.

To investigate the mechanism determining the susceptibility of TFET to WFV during ON/OFF state, Fig. 8(a) shows the combinations of metal-gate grain patterns corresponding to the maximum and minimum values of I_{ON} and I_{OFF}. In Fig. 8(a), the gray and black region stands for the metal grain with smaller (4.08 eV) and higher (4.28 eV) work function, respectively, and the arrow line denotes the direction of electron current flow. Because of the downward band diagram with increasing V_G (Fig. 3(b) and 3(c)), the critical tunneling path decreases and the spot with significant electron generation rate shifts from the drain side (under lower V_G) toward the tunneling junction (under higher V_G). Thus, the maximum and minimum I_{OFF} occur for the TFET possessing more grains with smaller and higher value of work function near the drain side, respectively. On the other hand, as I_{ON} is related to the grain patterns near the tunneling junction [21], TFET with more smaller-work-function grains in the vicinity of source region yields higher I_{ON}. It is also noted in Fig. 8(a) that the maximum (or minimum) I_{ON} and I_{OFF} come from distinct devices with different metal-gate grain patterns.

Fig. 9 compares the correlation between I_{ON} and I_{OFF} for TFET and FinFET devices in the presence of WFV. Because of its varying S.S. (Fig. 1(a)) and different dependence of I_{ON} and I_{OFF} on grain pattern (Fig. 8(a)), TFET shows weaker correlation between I_{ON} and I_{OFF} ($\rho = 0.49$) as opposed to the closer linkage ($\rho = 0.95$) found in the conventional FinFET counterpart (attribute to the common dependence of FinFET I_{ON} and I_{OFF} on device threshold voltage, V_T). This implies that if one optimizes WFV for I_{ON}, it does not necessarily result in an improvement in the I_{OFF} variation, which may possibly emerge as a potential drawback of TFET compared with the conventional FinFET. On the other hand, in terms of the optimization for I_{ON} and I_{OFF}, the lower correlation in

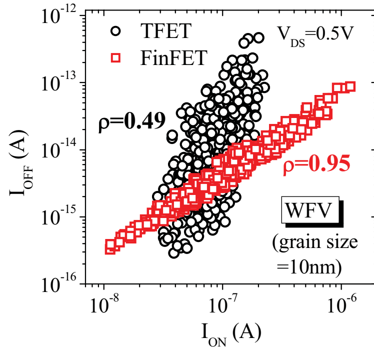

Fig. 9. Comparison of the correlation between I_{ON} and I_{OFF} for TFET and FinFET devices considering WFV. Compared with FinFET, I_{ON} exhibits less correlation with I_{OFF} in TFET.

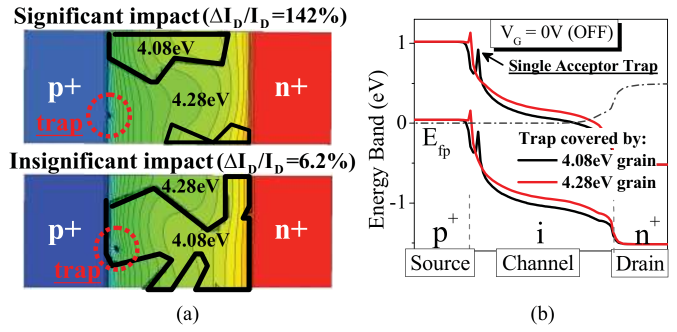

Fig. 11. (a) Schematics of the metal-gate grain patterns illustrating significant and insignificant RTN impact with a single acceptor trap placed near the tunneling junction at $V_G = 0$ V. The regions enclosed by black lines indicate the grains with smaller work function (4.08 eV). Fig. 11(b) shows the corresponding band diagrams for the cases in (a).

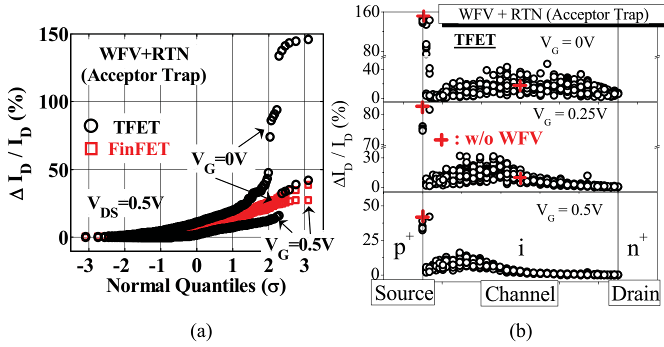

Fig. 10. (a) Comparison of RTN amplitude for TFET and FinFET devices at $V_G = 0$ and 0.5 V, and (b) the dependence of RTN amplitude on the lateral location of the trap considering WFV. Each circle in (b) represents a microscopically different TFET with an acceptor-type trap randomly placed across the sidewall interface and the cross symbol denotes the RTN amplitude without WFV.

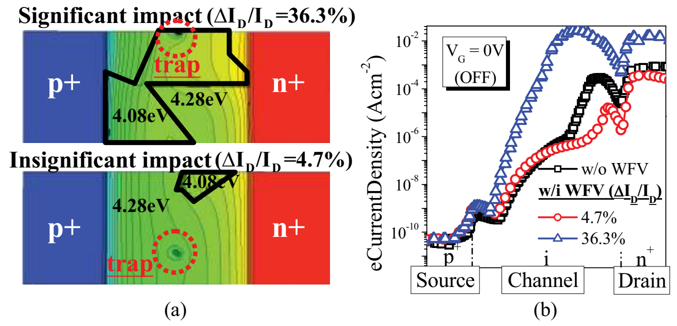

Fig. 12. (a) Schematics of the metal-gate grain patterns illustrating significant and insignificant RTN impact with a single acceptor trap in the middle region (Region A) at $V_G = 0$ V. The regions enclosed by black lines indicate the grains with smaller work function (4.08 eV). Fig. 12(b) shows the corresponding electron current density sliced through the trap location from source to drain for the cases in (a).

TFET decouples the linkage between ON and OFF state, thus enables us to independently and simultaneously improve I_{ON} and I_{OFF} [21]. From the variability point of view (Fig. 7), our results indicate that WFV gives rise to comparable I_D variations for TFET and FinFET, whereas substantial differences are observed in the presence of RTN. Fig. 10 shows the comparison of TFET and FinFET considering WFV and with an acceptor-type trap randomly placed across the sidewall interface. Because of the change in tunneling length and significant increase in tunneling current, discontinuous and considerably larger RTN amplitude are observed for TFET with trap near the tunneling junction. Fig. 10(b) shows the dependence of RTN amplitude on the lateral location of the trap for each microscopically different TFET under various V_G biases. Similar to the case in Fig. 2, regions near the tunneling junction are most vulnerable to RTN and the impact decreases toward the drain side. It is observed that for trap away from the tunneling junction, the locations with significant impact occur around the middle of the channel region at $V_G = 0$ V and gradually move to the tunneling junction with increasing V_G. Moreover, the variations in RTN amplitude caused by WFV can be clearly seen, particularly for a single acceptor-type trap placed near the tunneling junction at $V_G = 0$ V.

Fig. 11 shows the schematics of metal-gate grain patterns and the corresponding band diagrams of TFETs exhibiting significant and insignificant impact with a single acceptor-type trap placed near the tunneling junction. As can be seen, the inclusion of WFV leads to different amount of band bending and consequently, alters the influence of trap on the critical tunneling path and RTN amplitude. From Fig. 11(b), it can be seen that the grain with smaller work function (4.08 eV) yields more band bending and the localized trap shows less impact on the tunneling path, thus mitigating RTN amplitude. For trap away from the tunneling junction, the influence of RTN is determined by the relative distance between the charged trap and the position with large generation rate (or current density). As such, the variations of current density profile caused by WFV alter the relative distance and result in different RTN amplitude. Fig. 12 shows that significant RTN impact ($\Delta I_D/I_D = 36.3\%$) happens for the TFET with a single trap placed in proximity to the spot with significant generation rate (current density) because of the coverage of grain with smaller work function.

Fig. 13 shows the variations of RTN amplitude and its dependence on the lateral location of the trap in the presence of a donor-type trap and WFV. With the significant reduction in tunneling length (Fig. 6), TFET exhibits severe degradations in I_{OFF} and exceptionally large RTN amplitude (maximum $\Delta I_D/I_D \sim 10^6\%$). In addition, in contrast with the acceptor trap (Fig. 10(b)), the region with high susceptibility and large

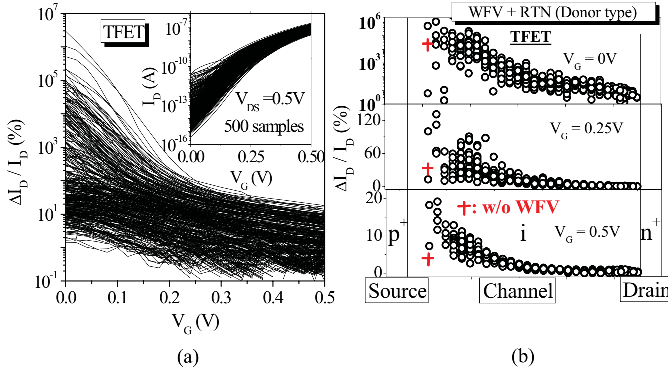

Fig. 13. (a) The variations of RTN amplitude for TFET in the presence of a donor-type trap and WFV, and (b) the dependence of RTN amplitude on the lateral location of the trap at various V_G. Each circle in (b) represents the RTN amplitude of each microscopically different TFET considering WFV and with a donor-type trap randomly placed across the sidewall interface.

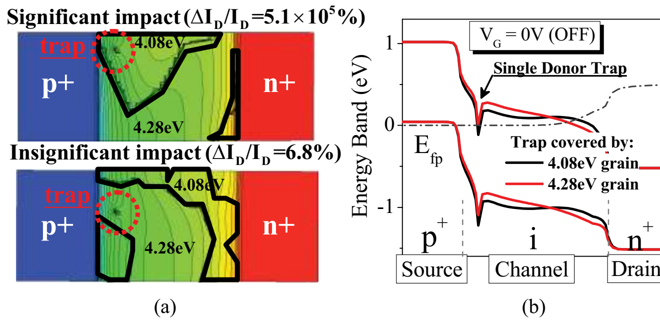

Fig. 14. (a) Schematics of the metal-gate grain patterns corresponding to significant and insignificant impact for a single donor-type trap near the tunneling junction at $V_G = 0$ V. The grains with smaller work function (4.08 eV) are enclosed by black lines. Fig. 14(b) shows the band diagrams for the cases in (a).

RTN amplitude variation is significantly wider (between the tunneling junction and middle of channel region in Fig. 13(b)). Fig. 14 shows the metal-gate grain patterns with significant and insignificant impact and the corresponding band diagrams for a single donor-type trap placed near the tunneling junction. It can be seen that with the increase in tunneling length, the RTN amplitude is drastically reduced for a donor-type trap beneath the grain with higher work function.

V. Conclusion

In this paper, we have investigated the impacts of RTN caused by a single acceptor-type and donor-type interface trap on TFET devices. 3-D TCAD atomistic simulations considering the influence of a localized charged trap are utilized to assess the dependence of RTN amplitude on trap location and device geometry. We show that significant RTN impact occurs for an acceptor-type trap near the tunneling junction, whereas the region with high susceptibility and large RTN amplitude variation is significantly wider (between the tunneling junction and middle of channel region) for a donor-type trap. In addition, the device design strategies (thinner EOT or longer $L_{\rm eff}$) that can be used to improve the TFET subthreshold characteristics are shown to degrade the immunity to RTN. In the presence of WFV, our results indicate that $I_{\rm ON}$ and $I_{\rm OFF}$ of TFET exhibit less correlation than that in the conventional FinFET because of the varying S.S. and different dependence of $I_{\rm ON}$ and $I_{\rm OFF}$ on the metal-gate grain pattern. Finally, the inclusion of WFV can enhance or reduce the impact of RTN depending on the type of the trap and the metal-gate grain composition/orientation.

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