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Analysis of Subthreshold Carrier Transport for Ultimate DGMOSFET

Hak Kee Jung and Sima Dimitrijev, *Senior Member, IEEE*

***Abstract*—A novel transport model for the subthreshold mode of double-gate MOSFETs (DGMOSFETs) is proposed in this paper. The model enables the analysis of short-channel effects (SCEs) such as the subthreshold swing (SS), the threshold-voltage rolloff, and the drain-induced barrier lowering. The proposed model includes the effects of thermionic emission and the quantum tunneling of carriers through the source–drain barrier. An approximative solution of the two-dimensional Poisson equation is used for the distribution of the electric potential, and the Wentzel–Kramers–Brillouin approximation is used for the tunneling probability. The model is verified by comparing the SS with numerical simulations. The new model is used to investigate the subthreshold characteristics of a DGMOSFET having the gate length in the nanometer range with an ultrathin gate oxide and channel thickness. The SCEs degrade the subthreshold characteristics of DGMOSFETs when the gate length is reduced below 10 nm, and any design in the sub-10-nm-regime should include the effects of quantum tunneling.**

***Index Terms*—Double-gate MOSFET (DGMOSFET), drain-induced barrier lowering (DIBL), short-channel effect (SCE), subthreshold swing (SS), threshold-voltage rolloff, tunneling.**

I. Introduction

As MOS TECHNOLOGY progresses, device dimensions shrink into the nanometer scales. The double-gate MOSFET (DGMOSFET) is a particularly promising candidate for ultimate CMOS scaling due to its good control of short channel effects (SCEs) such as the near-ideal subthreshold slope and the mobility enhancement [1]–[3]. The double-gate design provides inherent electrostatic coupling in the channel [4]. This intimate coupling between the gates and the channel makes DGMOSFET technology the most scalable of all FET designs. The DGMOSFET is electrostatically superior to a single-gate MOSFET because two gates are used to control the channel from both sides, thus allowing for additional gate-length scaling by nearly a factor of two. The two gates control roughly twice as much current as a single gate, resulting in stronger switching signals. In addition, the ballistic transport of carriers can be achieved with DGMOSFETs due to the low doping in the channel and the DG features. The challenge lies in obtaining suitable threshold voltages for high-speed logic devices, while controlling the extrinsic resistance. However, for sub-20-nm DGMOSFETs, the SCEs such as the threshold-voltage rolloff (ΔV_{th}), drain-induced barrier lowering (DIBL), and degradation of the subthreshold swing (SS) become very important issues that cannot be neglected.

Many papers have demonstrated through numerical simulations that DGMOSFETs with effective channel lengths of under 20 nm exhibit significant quantum-tunneling transport. The density-gradient method [5], [6], the two-dimensional (2-D) Schrödinger–Poisson solver [7], and Green's functions [9] have been used to show that the quantum mechanical tunneling in DGMOSFETs can be significant when the device is scaled down to the 10-nm range and may even dominate in some cases. These methods are based on very complicated equations that require a self-consistent solution with a complex numerical code, that obscures the understanding of the short-channel effects in DGMOSFETs. A model with the physical meaning of the model parameters is needed for circuit simulation and IC design. Recently, a 2-D analytical solution for SCEs in DGMOSFETs with channel lengths above 20 nm was proposed by Liang and Taur [10] based on the drift- and diffusion-current mechanisms. For sub-20-nm DGMOSFETs, the thermionic and the tunneling currents have to be included when analyzing the carrier transport in the subthreshold regime.

Consequently, this paper aims to propose a model for the subthreshold characteristics of DGMOSFETs that includes the contribution of both the thermionic emission and quantum tunneling to the subthreshold current. The tunneling probability is obtained from the Wentzel–Kramers–Brillouin (WKB) approximation, which is used to obtain the gate-length and voltage-dependent tunneling currents.

This paper is arranged as follows. The proposed model is described in Section II. In Section III, we present the key results and compare the model with 2-D simulation results. There is a special focus on the influence of tunneling in the subthreshold regime on scaling limitation in DGMOSFET. Section IV summarizes the results.

II. Model

A. Device Structure

The structure of the DGMOSFET used in this paper is schematically presented in Fig. 1. This symmetric structure is characterized by two identical polysilicon gates with no overlap with the source/drain extensions. The thickness of a p-type doped silicon (t_{Si}), the thickness of the gate oxide (t_{ox}), and the channel length L_g are the geometric parameters. The doping level of the p-type silicon channel is $N_A = 10^{16}$ cm^{-3}. The n-type source and drain regions are uniformly doped at a level

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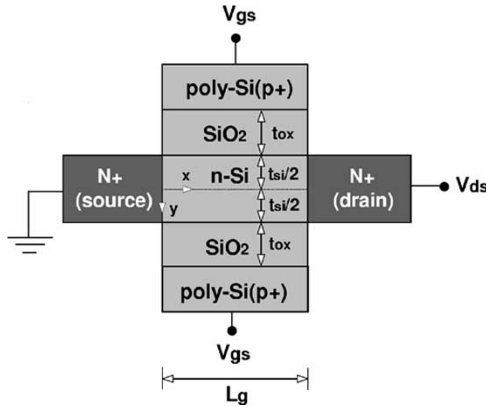

Fig. 1. Schematic structure of the symmetrical DGMOSFET used in this paper.

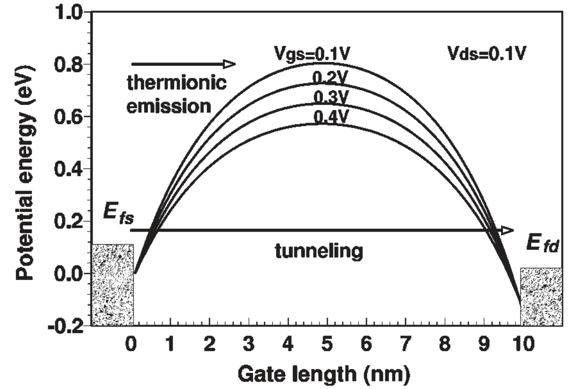

Fig. 2. Energy band diagrams along the x-axis for the increasing gate voltage in a DGMOSFET with $L_g = 10$ nm. E_{fs} and E_{fd} are the Fermi levels in the source and drain regions, respectively.

of 10^{20} cm^{-3}. The polygate is a uniformly doped p-type with a doping concentration of 10^{20} cm^{-3}.

B. Subthreshold Current

For DGMOSFETs with channel lengths in the 10-nm region, it can be assumed that the thermionic emission and tunneling currents dominate. This assumption is equivalent to the assumption that the drift and diffusion currents can be neglected, and will be verified by a comparison to the simulation results in Sections III-A and B.

The thermionic emission and tunneling are two independent current mechanisms, as illustrated in Fig. 2, so the two current models are developed separately. For either current, an equation for the electric potential in the channel is necessary. The channel potential in the subthreshold region can be obtained from the 2-D Poisson equation under the condition of full depletion

$$\nabla^2\Psi = \frac{qN_A}{\epsilon_{\mathrm{Si}}} \tag{1}$$

where q is the electronic charge and ϵ_{Si} is the silicon permittivity. Ψ can be expressed as [11]

$$\Psi(x,y) = V_{\mathrm{gs}} - \Phi_{\mathrm{MS}} + U_{\mathrm{1D}}(y) + \phi_{\mathrm{2D}}(x,y) \tag{2}$$

where V_{gs} is the gate voltage, Φ_{MS} is the gate-to-channel work function difference, and $U_{\mathrm{1D}}(y)$ is the one-dimensional (1-D) potential in the direction of thickness

$$\begin{aligned} U_{\mathrm{1D}}(y) &= \frac{V_A}{2}\left(\frac{y^2}{t_{\mathrm{Si}}^2} - \frac{1}{4} - \frac{1}{r}\right) \\ V_A &= \frac{qN_A t_{\mathrm{Si}}^2}{\epsilon_{\mathrm{Si}}} \\ r &= \frac{\epsilon_{\mathrm{ox}} t_{\mathrm{Si}}}{\epsilon_{\mathrm{Si}} t_{\mathrm{ox}}}. \end{aligned} \tag{3}$$

The term $V_{\mathrm{gs}} - \Phi_{\mathrm{MS}} + U_{\mathrm{1D}}(y)$ in (2) is the solution to the 1-D Poisson equation in the thickness direction, representing the channel potential in a long channel device, as defined by the ionized doping atoms. The term $\phi_{\mathrm{2D}}(x,y)$ is the solution of the 2-D Laplace equation describing the influence of the source/drain. With the boundary conditions, $\phi_{\mathrm{2D}}(x,y)$ can be expressed as follows [11]:

$$\phi_{\mathrm{2D}}(x,y) = \sum_j \Gamma_j \cos\frac{y}{\lambda_j} \frac{\left[V_j\left(\sinh\frac{x}{\lambda_j} + \sinh\frac{L_g - x}{\lambda_j}\right) + V_{\mathrm{ds}}\sinh\frac{x}{\lambda_j}\right]}{\sinh\frac{L_g}{\lambda_j}}. \tag{4}$$

In (4), λ_j are eigenvalues satisfying

$$\begin{aligned} \tan\frac{t_{\mathrm{Si}}}{2\lambda_j} &= \frac{r\lambda_j}{t_{\mathrm{Si}}} \\ \Gamma_j &= \frac{2\lambda_j}{t_{\mathrm{Si}}} \frac{\sqrt{1 + \frac{t_{\mathrm{Si}}^2}{r^2\lambda_j^2}}}{\left(\frac{1}{r} + \frac{1}{2} + \frac{1}{2}\frac{t_{\mathrm{Si}}^2}{r^2\lambda_j^2}\right)} \\ V_j &= V_{\mathrm{bi}} - V_{\mathrm{gs}} + \Phi_{\mathrm{MS}} + \frac{V_A\lambda_j^2}{t_{\mathrm{Si}}^2} \end{aligned}$$

where V_{bi} is the built-in voltage and V_{ds} is the drain voltage. In (4), only the lowest-order mode is included because of its dominance.

The thermionic current is determined by the number of electrons that overcome the barrier height between the source and drain per unit time. Based on the Maxwell–Boltzmann statistics, the concentration of electrons in the source at energy levels higher than the barrier peak is $n_m = (n_i^2/N_A)\mathrm{e}^{q\Psi_{\min}/kT}$, where n_i is the intrinsic carrier concentration. The minimum channel potential $\Psi_{\min}$, corresponding to the current path, can be found from the condition $\partial\Psi(x,y)/\partial x = 0$. Given that these electrons move randomly with the average thermal velocity v_{th}, about 1/6 of these electrons move towards the drain, and the number of electrons that hit the cross-sectional area $t_{\mathrm{Si}}W$ per unit time is $n_m v_{\mathrm{th}} t_{\mathrm{Si}} W/6$. Therefore, the thermionic current is

$$I_{\mathrm{ther}} = \frac{qn_m(y)v_{\mathrm{th}}t_{\mathrm{Si}}W}{6} \approx \frac{qn_m(d_{\mathrm{eff}})v_{\mathrm{th}}t_{\mathrm{Si}}W}{6}. \tag{5}$$

The parameter d_{eff} represents the effective current path [11] and is determined by

$$\cos\frac{d_{\text{eff}}}{\lambda_1} = \frac{\int_0^{\frac{t_{\text{Si}}}{2}} \cos\frac{y}{\lambda_1} n_m(y)dy}{\int_0^{\frac{t_{\text{Si}}}{2}} n_m(y)dy}.$$

Strictly speaking, (5) gives the thermionic current of electrons moving from the source to the drain and not the net thermionic current, because it does not include the current due to the emission of electrons in the opposite direction (from the drain to the source). The current emitted from the drain, however, can be neglected for sufficiently large V_{ds} voltages.

The quantum mechanical tunneling was not included in the analysis by Chen *et al.* [11], which focused on the modeling of SCE effects due to the thermionic emission (but not including an equation for the thermionic current itself). However, the tunneling current is no longer negligible when the channel lengths decrease to the 10-nm range. In this paper, we use the WKB approximation to determine the tunneling probability. The WKB approximation is relatively simple and reasonably accurate for channel lengths down to a few nanometers. The differences between the results derived from the WKB approximation and the full quantum treatment are insignificant, according to recent report by Stadele [12]. The WKB equation for the tunneling probability is

$$T_{\text{t,l}} = \exp\left[-2\int_{x_1}^{x_2} |\alpha_{\text{t,l}}(x)|\, dx\right]$$

$$\alpha_{\text{t,l}}(x) = \sqrt{\frac{2m_{\text{t,l}}\left[q\Psi(x, d_{\text{eff}}) - E_{\text{fm}}\right]}{\hbar}} \tag{6}$$

where $T_{\text{t,l}}$ is the tunneling probability for electrons with transverse and longitudinal effective mass, respectively, $\Psi(x, d_{\text{eff}})$ is the position-dependent potential, E_{fm} is the Fermi level in the source/drain regions, $m_{\text{t,l}}$ is the transverse/longitudinal effective mass, and x_1 and x_2 are the x points where the potential energy defining the barrier is equal to the Fermi level.

Assuming that the concentration of electrons in the source is equal to the doping level N_D and that 1/6 of these electrons move towards the drain with the average thermal velocity v_{th}, the number of electrons that hit the barrier per unit time is $N_D v_{\text{th}} t_{\text{Si}} W/6$. This number has to be multiplied by the tunneling probability to obtain the tunneling current. It can be seen from (6) that the tunneling probability is different for electrons with the transverse and the longitudinal effective mass. Because of that, it is inappropriate to use the average thermal velocity v_{th} that is obtained from the conductivity effective mass. To resolve this problem, the tunneling current is determined separately for electrons with the transverse and the longitudinal effective masses and then the two components are added to obtain the total tunneling current. Given that 2/3 of the electrons appear with the transverse and 1/3 with the longitudinal effective mass, the following equation for the tunneling current is obtained:

$$I_{\text{tunn}} = \left(\frac{qN_D t_{\text{Si}} W}{6}\right)\left(\frac{2T_{\text{t}} v_{\text{th}_\text{t}}}{3} + \frac{T_l v_{\text{th}_l}}{3}\right) \tag{7}$$

where T_{t} and v_{th_t} are the tunneling probability and the thermal velocity for electrons with the transverse effective mass, respectively, and T_l and v_{th_l} are the tunneling probability and the thermal velocity for the electrons with the longitudinal effective mass, respectively. Similar to the discussion related to the net thermionic current, the tunneling from the drain towards the source can be neglected at sufficiently high V_{ds} voltages.

Adding the thermionic and the tunneling currents, the total subthreshold current of a DGMOSFET in the ballistic regime is obtained

$$I_{\text{tot}} = I_{\text{ther}} + I_{\text{tunn}}.$$

C. SS

The general SS model for subthreshold currents consisting of two components (thermionic and tunneling) can be expressed as

$$\text{SS} = \left[\frac{\partial \log(I_{\text{tot}})}{\partial V_{\text{gs}}}\right]^{-1} = \left[\frac{\frac{\partial I_{\text{ther}}}{\partial V_{\text{gs}}} + \frac{\partial I_{\text{tunn}}}{\partial V_{\text{gs}}}}{\ln 10 \cdot I_{\text{tot}}}\right]^{-1}. \tag{8}$$

Using (5), the following solution for $\partial I_{\text{ther}}/\partial V_{\text{gs}}$ in (8) is obtained

$$\begin{aligned}\frac{\partial I_{\text{ther}}}{\partial V_{\text{gs}}} &= \left(\frac{qv_{\text{th}}t_{\text{Si}}W}{6}\right)\frac{\partial n_m(y)}{\partial V_{\text{gs}}}\\ &= \left(\frac{qv_{\text{th}}t_{\text{Si}}W}{6}\right)n_m(y)\left(\frac{q}{kT}\right)\left(\frac{\partial \Psi_{\min}}{\partial V_{\text{gs}}}\right)\\ &= \left(\frac{qv_{\text{th}}t_{\text{Si}}W}{6}\right)n_m(d_{\text{eff}})\left(\frac{q}{kT}\right)\\ &\quad\times\left[1 - \left(\frac{\Gamma_1 \cos\frac{d_{\text{eff}}}{\lambda_1}}{\sinh\frac{L_g}{\lambda_1}}\right)\frac{w}{v^{\frac{3}{2}}}\right]\end{aligned} \tag{9}$$

where the parameters u, v, and w are defined as

$$\begin{aligned} w &= v\left(\left(1-\cosh\frac{L_g}{\lambda_1}\right)(2\alpha V_1-\beta)+2V_1\sinh\frac{L_g}{\lambda_1}+\alpha V_{DS}\right)\\ &\quad - u\left(V_1 - \alpha(\alpha V_1 - \beta)\right)\\ u &= \left(1-\cosh\frac{L_g}{\lambda_1}\right)\left(\alpha V_1^2 - \beta V_1\right) + V_1^2 \sinh\frac{L_g}{\lambda_1}\\ &\quad + (\alpha V_1 - \beta)V_{DS}\\ v &= V_1^2 - (\alpha V_1 - \beta)^2\\ \alpha &= \coth\frac{L_g}{\lambda_1} - \operatorname{csch}\frac{L_g}{\lambda_1}, \quad \beta = V_{DS}\operatorname{csch}\frac{L_g}{\lambda_1}. \end{aligned} \tag{10}$$

The first derivative of the tunneling current leads to the following result:

$$\frac{\partial I_{\text{tunn}}}{\partial V_{\text{gs}}} = \left(\frac{qN_D t_{\text{Si}} W}{6}\right)\left(\frac{2v_{\text{th}_\text{t}}}{3}\frac{\partial T_{\text{t}}}{\partial V_{\text{gs}}} + \frac{v_{\text{th}_l}}{3}\frac{\partial T_l}{\partial V_{\text{gs}}}\right). \tag{11}$$

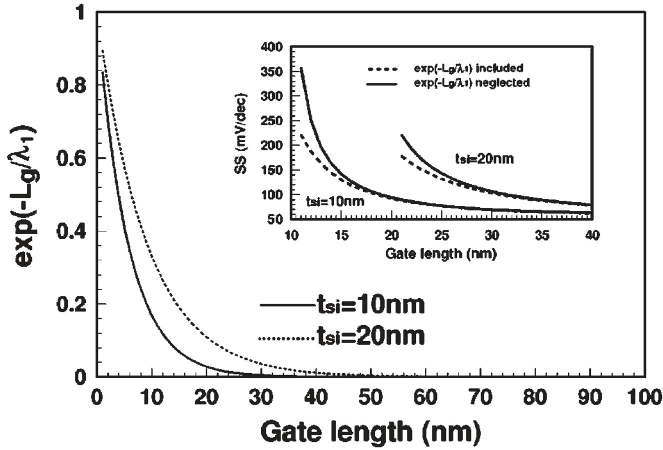

Fig. 3. Values of $\exp(-L_g/\lambda_1)$ for different channel thicknesses and gate lengths.

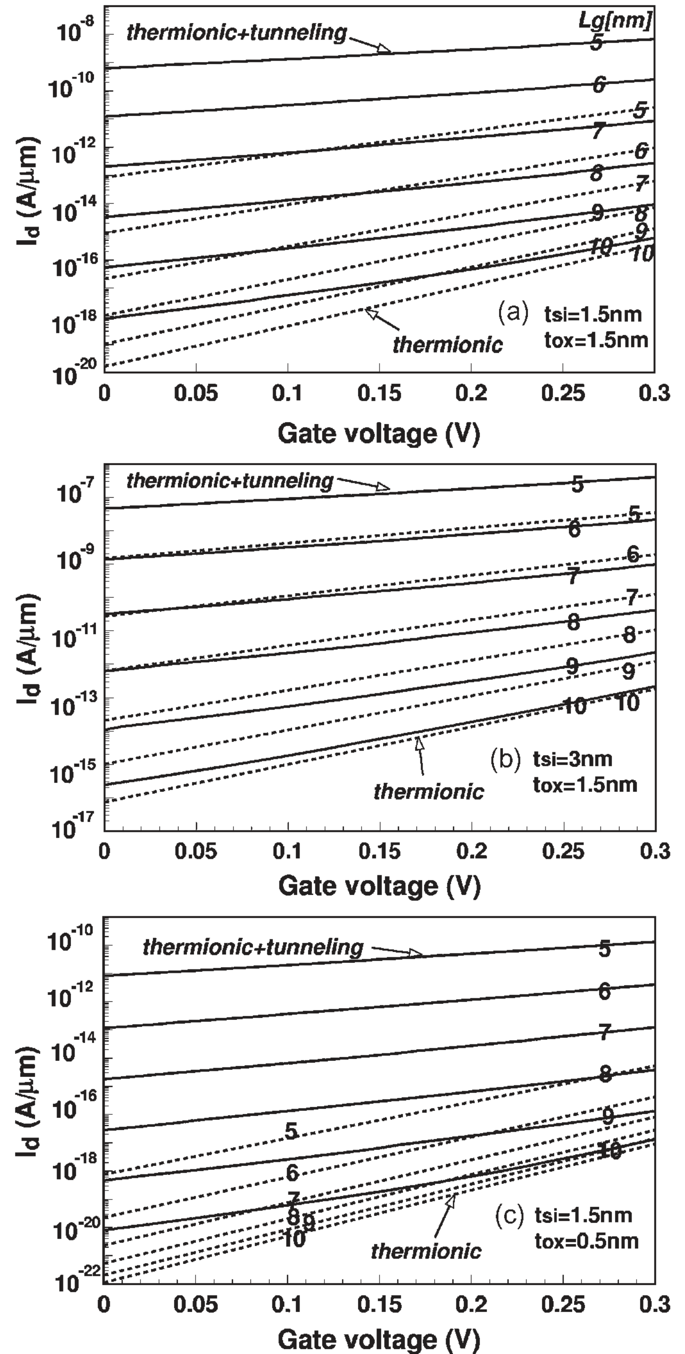

Fig. 4. Drain current in the subthreshold regime at $V_{\mathrm{ds}} = 0.1$ V for different channel lengths, illustrating the contribution of tunneling to the total current for (a) $t_{\mathrm{Si}} = 1.5$ nm and $t_{\mathrm{ox}} = 1.5$ nm, (b) $t_{\mathrm{Si}} = 3.0$ nm and $t_{\mathrm{ox}} = 1.5$ nm and (c) $t_{\mathrm{Si}} = 1.5$ nm and $t_{\mathrm{ox}} = 0.5$ nm.

III. Analysis of SCE in Nanoscale DGMOSFETs and Verification of the Model

The results for subthreshold current, SS, threshold-voltage rolloff, and DIBL in nanoscale DGMOSFETs, obtained with the new model, are presented and analyzed in this section. In addition, the results are compared to available simulation data for the SS and the threshold-voltage rolloff to verify the validity of the model.

A. Subthreshold Current and SS

The assumption $\exp(-L_g/\lambda_1) \ll 1$ proposed by Chen *et al.* [11] is not used because this assumption is not valid when the gate length drops below 20 nm [13]. The exponential term is not negligible for gate lengths below 20 nm, as shown in Fig. 3. To confirm the impact of the $\exp(-L_g/\lambda_1)$ factor on the SS, we calculated SSs with and without the assumption $\exp(-L_g/\lambda_1) \ll 1$. The inset in Fig. 3 shows that the impact of the $\exp(-L_g/\lambda_1)$ factor is significant for sub-20-nm gate lengths.

Fig. 4 shows the subthreshold transfer characteristics (I_{ds} versus V_{gs}) at $V_{\mathrm{ds}} = 0.1$ V for channel lengths from 5 to 10 nm and different gate oxide and channel thicknesses. The slopes of the characteristics are reduced when the tunneling current is added to the thermionic current, which is the effect of the SS increase discussed later. The relative contribution of tunneling becomes smaller when the channel thickness and the gate lengths are increased, as shown in Fig. 4(a) and (b). Also, the subthreshold current due to tunneling becomes much smaller than the thermionic current for gate lengths above 10 nm. Fig. 4(a) and (c) shows that the tunneling current decreases if the gate-oxide thickness is reduced because the effective current path is changed. For $t_{\mathrm{ox}} = 1.5$ nm [Fig. 4(a)], the OFF current due to tunneling becomes unacceptably high when the gate length is reduced. At $L_g = 5$ nm, the tunneling current is more than three orders of magnitude higher than the thermionic current.

Fig. 5 shows that the effective current path d_{eff} is different for different gate oxide thicknesses, which is due to different r and λ_1. It can be seen from (6) that the tunneling rate depends on the effective current path d_{eff}. If r and λ_1 are different, $\phi(x, y)$ is also different. Because r and λ_1 depend on the oxide thickness, the SS also depends on the oxide thickness even under constant channel conditions [11]. As shown in Fig. 5, the tunneling rate changes by nearly two orders of magnitude when the oxide thickness is changed from $t_{\mathrm{ox}} = 0.5$ nm to $t_{\mathrm{ox}} = 1.5$ nm. This results in a nearly two orders of magnitude difference in the OFF current for $t_{\mathrm{ox}} = 0.5$ nm and $t_{\mathrm{ox}} = 1.5$ nm, as shown in Fig. 4.

Fig. 6(a) shows the variation of SS as a function of the gate length. It can be seen that the results from the proposed model

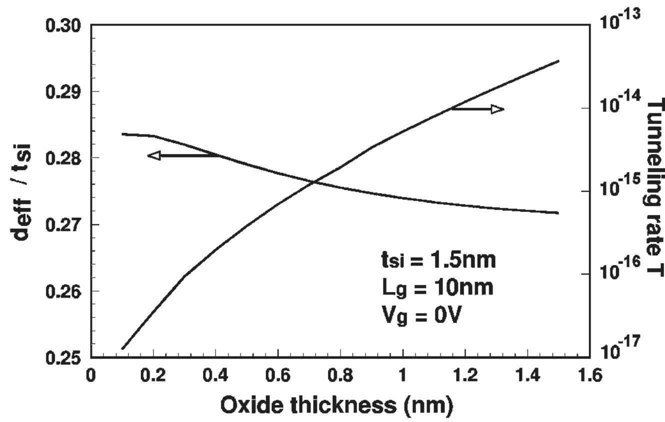

Fig. 5. Normalized effective current path and tunneling rate versus gate oxide thickness.

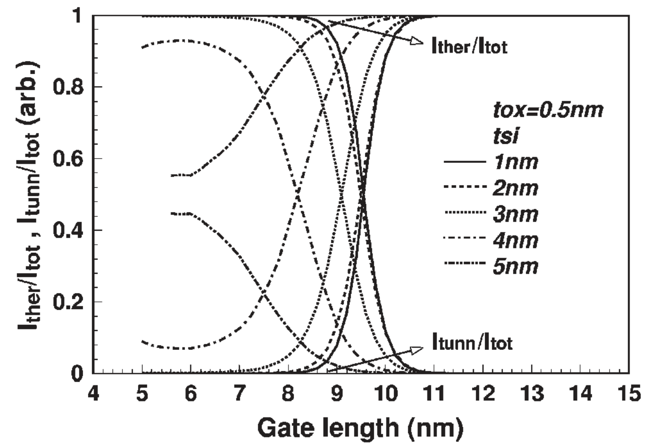

Fig. 7. Current ratios of the thermionic emission current and the tunneling current to the total current for different channel lengths and channel thicknesses.

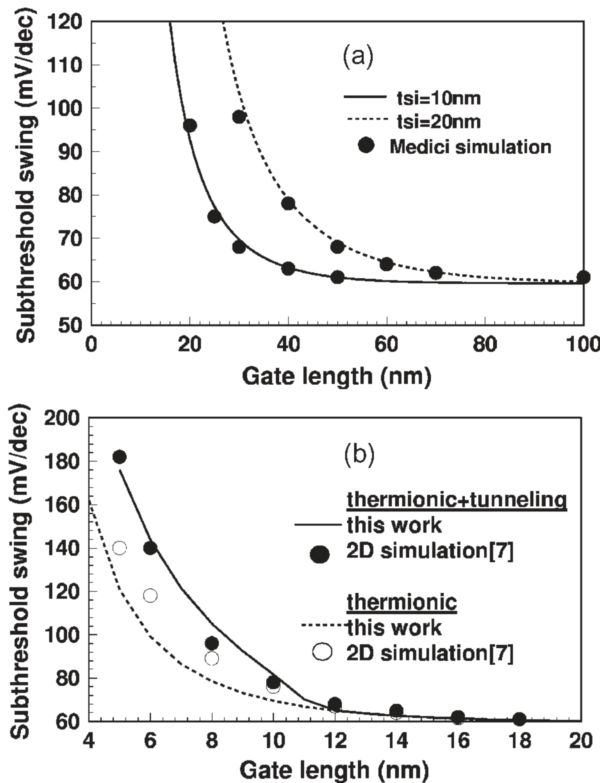

Fig. 6. (a) Comparison of the SSs obtained by the Medici simulation [11] and the proposed model. (b) SS with and without the quantum tunneling as a function of the channel length for DGMOSFETs with $t_{\mathrm{Si}} = 1.5$ nm and $t_{\mathrm{ox}} = 1.5$ nm at $V_{\mathrm{gs}} = 0.1$ V and $V_{\mathrm{ds}} = 0.1$ V.

in this paper agree well with Medici numerical simulation. It is important to emphasize that the numerical simulation includes the drift and diffusion currents, in addition to the thermionic and tunneling currents. The good agreement between the model and the simulation results indicate that the drift and diffusion currents are negligible in the subthreshold regime, which is in agreement with the analysis published by Chen *et al.* [11]. It should also be pointed out that this comparison with the simulation results is made for DGMOSFETs with channels longer than 20 nm. The analysis presented in this paper is focused on channel lengths smaller than 20 nm, where the relative importance of the thermionic and tunneling currents increases in comparison to the drift and diffusion currents. Therefore, this comparison to the simulation results verifies the validity of the assumption that the thermionic and the tunneling terms are sufficient for the presented model.

Fig. 6(b) shows the variation of SS as a function of the gate length in the sub-20-nm region. It can be seen that the results from the proposed model in this paper agree well with 2-D numerical simulation [7]. It can also be seen that the SS degradation is larger for shorter channels. This is because the tunneling becomes more pronounced as the channel length is reduced. The ratios of the thermionic and tunneling currents for the subthreshold current are shown in Fig. 7. It can be seen that the thermionic current dominates for channel lengths above 10 nm, whereas the tunneling current dominates for channel lengths below 10 nm. Given that the dependence of the tunneling current on the gate voltage is weak, the SS increases significantly in the sub-10-nm region, degrading the performance gains achieved by the thin body and the double-gate control of the channel. Reasonable values of the SS (60–80 mV/dec) can only be obtained with above 10-nm gate lengths when the current is mostly due to the thermionic emission, as shown in Fig. 6(b). The relative contribution of the tunneling current can be reduced by an increase in the channel thickness, as shown in Fig. 7, but this method is not suitable because the SS is then increased by the thermionic current.

B. Threshold-Voltage Rolloff

To validate the variation of the threshold voltage with the gate length, obtained from the proposed model, the results of our model are compared to the results of the 2-D numerical simulation available in the literature [7]. The threshold voltage was determined by a method defined for technology computer-aided design (TCAD) applications as the gate voltage corresponding to $I_d = 0.1\ \mu\mathrm{A}/\mu\mathrm{m}$ [8]. Fig. 8 shows that there is a good agreement between this model and the numerical simulation. Thus, it can be concluded that the proposed model takes into account the electrostatic effects very well and that it is suited for calculations of the threshold voltage of small-geometry DGMOSFETs. Fig. 8 also shows that the SCE is increased by the quantum tunneling. These results clearly show the importance

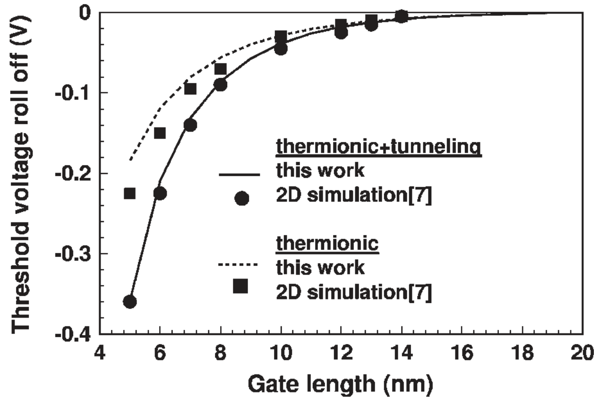

Fig. 8. Threshold-voltage rolloff as a function of the gate length in DGMOSFETs with a channel thickness of $t_{\mathrm{Si}} = 1.5$ nm and a gate oxide thickness of $t_{\mathrm{ox}} = 1.5$ nm. The results of the proposed model are compared to the results obtained by a 2-D numerical simulation [7].

of the tunneling current in nanoscale DGMOSFETs for analysis of SCEs such as the threshold-voltage rolloff. Again, the effects of tunneling become pronounced for DGMOSFETs with gates shorter than 10 nm.

C. DIBL

The threshold-voltage dependence on the drain bias is important for digital applications. The DIBL causes the threshold voltage to be a function of the operating voltages. It is not only the gate voltage that lowers the potential barrier to enable the flow of thermionic and tunneling currents, but the electric field due to the drain voltage can also cause barrier lowering. Therefore, the threshold voltage is reduced by the drain voltage, and even a smaller gate voltage is able to cause a strong inversion, causing a leakage and even a punchthrough in some cases. To reduce this effect, DGMOSFETs have to be designed for the minimum DIBL.

Using the proposed model, the DIBL is calculated and plotted as a function of the gate length in Fig. 9(a). We can see that the DIBL increases due to quantum tunneling for gate lengths below 12 nm. Usually, the DIBL is proportional to the channel thickness and the gate oxide thickness and is inversely proportional to the gate length. The slope is approximately -3, which is related to the fact that the punchthrough voltage has a L_g^3 dependence [14]. However, these relationships no longer hold for the case of thinner gate oxides such as $t_{\mathrm{ox}} = 0.5$ nm and especially for gate lengths of over 10 nm. The DIBL effect becomes very sensitive to gate lengths in the regime of lower gate oxide thicknesses. The design contours of DGMOSFETs having gate oxide thickness from 0.5 to 2.0 nm for a DIBL of 100 mV/V are shown in Fig. 9(b). To maintain the DIBL at about 100 mV/V when the tunneling occurs (sub-10-nm gate lengths), smaller gate oxide and channel thicknesses are necessary.

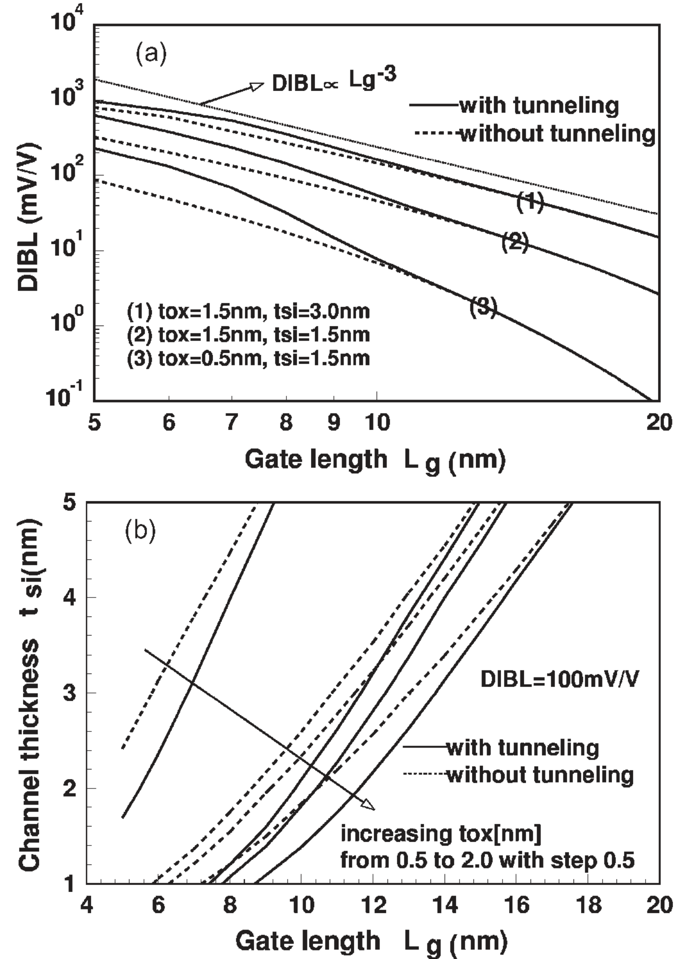

Fig. 9. (a) DIBL as a function of the gate length (DIBL is defined as the change of the threshold voltage per 1 V change of the drain voltage). (b) Design contours of DGMOSFETs having a gate oxide thickness changing from 0.5 to 2.0 nm for a DIBL of 100 mV/V.

IV. Conclusion

A model for analyzing SCEs, such as the SS, threshold-voltage rolloff, and DIBL of nanoscale DGMOSFETs is proposed in this paper. The results of this model have been compared to 2-D numerical simulations to verify the model. Various calculations have been performed to investigate whether our approach can properly model the quantum tunneling between the source and drain in DGMOSFETs in the subthreshold region. A variety of DGMOSFETs with gate lengths ranging from 5 to 20 nm have been studied.

The thermionic emission has been found as the main mechanism of carrier transport for channel lengths above 10 nm. On the other hand, tunneling is dominant in DGMOSFETs with gate lengths below 10 nm, significantly influencing the device scaling in the sub-10-nm region.

To analyze SCEs, we have calculated the SS, threshold-voltage rolloff, and the DIBL. We have observed that as the gate length is reduced, there is a corresponding degradation of SCEs, which becomes very significant in the sub-10 nm-region when the tunneling becomes dominant.

As shown by the results, design rules have to be very strict in DGMOSFETs which have gate lengths below 10 nm since extremely small channel thicknesses and gate oxide thicknesses are necessary. The results demonstrate that the scaling limit due to the quantum tunneling should be about 10 nm for channel thicknesses below 1.5 nm.

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