

## Analysis of subthreshold swing in junctionless double gate MOSFET using stacked high- $k$ gate oxide

Hakkee Jung

Department of Electronic Engineering, Kunsan National University, Republic of Korea

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### ABSTRACT

In this paper, the subthreshold swing was observed when the stacked high- $k$  gate oxide was used for a junctionless double gate (JLDG) MOSFET. For this purpose, a subthreshold swing model was presented using the series-type potential model derived from the Poisson equation. The results of the model presented in this paper were in good agreement with the two-dimensional numerical values and those from other papers. Using this model, the variation of the subthreshold swing for the channel length, silicon thickness, gate oxide thickness, and dielectric constant of the stacked high- $k$  material was observed using the dielectric constant as a parameter. As a result, the subthreshold swing was reduced when the high- $k$  materials were used as the stacked gate oxide film. In the case of the asymmetric structure, the subthreshold swing can be reduced than that of the symmetric JLDG MOSFET when the dielectric constant of the bottom stacked oxide film was greater than that of the top stacked oxide film. In the case of the asymmetric structure, the subthreshold swing could be also reduced by applying the bottom gate voltage lower than the top gate voltage.

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### Corresponding Author:

Hakkee Jung,  
Departement of Electronic Engineering,  
Kunsan National University,  
558 Daehangro, Gunsan, Chonbuk 54150, Republic of Korea.  
Email: hkjung@kunsan.ac.kr

## 1. INTRODUCTION

Recently, integrated circuit technology is focused on high speed operation, low power consumption and large capacity by reducing transistor size. Major semiconductor manufacturers are investing enormous funds in reducing transistor size [1-3]. The device developed to overcome the short channel effect and the difficulty of the process inevitably caused by the size reduction of the transistor is a junctionless double gate JLDG MOSFET [4-7]. In this structure, there is no abrupt change of doping distribution between the source/drain and the channel, so it is easy to process and reduce the degradation of the subthreshold swing, threshold voltage shift, and drain induction barrier lowering (DIBL) caused by the transistor size reduction [8-11]. Recently, a junctionless structure has been developed in various forms to reduce such a short channel effect [12-14]. However, due to the scaling effect, the reduction of transistor size inevitably decreases the gate oxide thickness, which caused the short channel effect by the hot carrier, such as the increase of parasitic current to the gate oxide and the increase of power consumption [15-16].

In order to solve this problem, a study was conducted to use high- $k$  materials as the gate oxide film [17-19]. In addition, many structural studies have been conducted in the case of a double gate MOSFET to reduce the short channel effects such as using two channel materials or two gate metals [20-22]. However, a high- $k$  materials have a disadvantage in that it is not superior to silicon dioxide in forming an interface with silicon used as a channel. In order to overcome these drawbacks, this paper analyzes

the subthreshold swing of a JLDG MOSFET using a stacked gate oxide film with a layer of silicon dioxide and a high dielectric constant material. The subthreshold swing is a measure of how quickly the current decreases when the transistor becomes in a turn-off state. It has a great influence on leakage current, power consumption, and on-off current ratio. Here, we will propose a potential model for analyzing not only the symmetric but also the asymmetric JLDG MOSFET. In the case of the asymmetric JLDG MOSFET, the top and bottom gate structures can be fabricated differently, and the applied voltages of the top and bottom gate can be different. Islam et al. used a distribution function whose top and bottom potential distribution is proportional to the third power of displacement to analyze the subthreshold swing of a JLDG MOSFET with a stacked gate oxide film [23]. However, only cases where the dielectric constant was specific were calculated. In this paper, we analyze the subthreshold swing of the asymmetric JLDG MOSFET for the dielectric constant range from 3.9 to 80, such as SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, Y<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>/ZrO<sub>2</sub>, La<sub>2</sub>O<sub>3</sub>, and TiO<sub>2</sub> which Priya *et al.* [24] used to analyze the transfer characteristics of the junctionless transistor.

In addition, the potential distribution model of the asymmetric junction-based double gate MOSFET presented by Ding et al. is modified to apply for the asymmetric JLDG MOSFET [25]. We will analyze the change of the subthreshold swing and compare the subthreshold swings of the symmetric and asymmetric structures, using the subthreshold swing model proposed in this paper.

## 2. THE SUBTHRESHOLD SWING MODEL OF THE ASYMMETRIC JLDG MOSFET

Figure 1 shows a schematic diagram of the asymmetric JLDG MOSFET used in this paper. The source and drain are heavily doped with  $n^+$  and the channel is doped with  $N_d = 10^{19} / \text{cm}^3$ . The  $p^+$  polysilicon is used as the gate,  $\epsilon_{\text{SiO}_2}$  is the dielectric constant of silicon dioxide used to maintain the superiority of the interface with silicon, and corresponding thickness  $t_{\text{SiO}_2}$  is 1 nm. The  $\epsilon_1$  and  $t_{\text{ox}1}$  are the dielectric constant and thickness of the top gate oxide, respectively, and  $\epsilon_2$  and  $t_{\text{ox}2}$  are the dielectric constant and thickness of the bottom gate oxide, respectively. The dielectric constants,  $\epsilon_1$  and  $\epsilon_2$ , are in the range from 3.9 to 80. This corresponds to dielectric constants of commonly used dielectric materials such as SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, Y<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>/ZrO<sub>2</sub>, La<sub>2</sub>O<sub>3</sub>, and TiO<sub>2</sub>.  $V_{\text{gt}}$  and  $V_{\text{gb}}$  are the gate voltages of the top and bottom, respectively, and the same 0.1 V is used in this paper.  $V_s$  and  $V_d$  are the voltages applied to the source and the drain, respectively. The potential distribution of the asymmetric JLDG MOSFET is obtained using the Poisson equation and boundary conditions as follows [25].

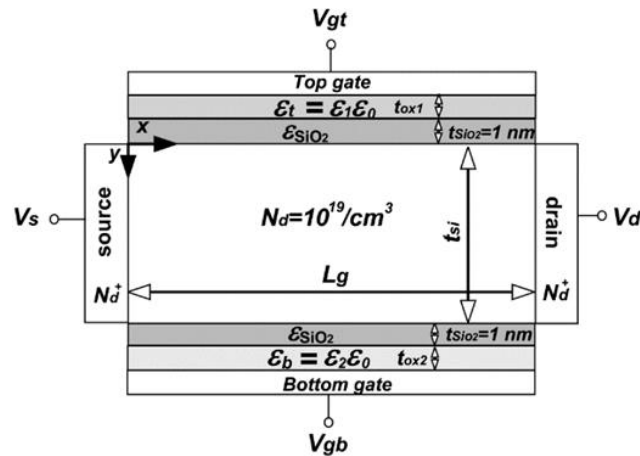


Figure 1. Schematic sectional diagram of asymmetric JLDG MOSFET

$$\frac{\partial^2 \phi(x, y)}{\partial x^2} + \frac{\partial^2 \phi(x, y)}{\partial y^2} = -N_d / \epsilon_{\text{Si}} \quad (1)$$

$$\phi(0, y) = V_s, \quad \phi(L_g, y) = V_s + V_d$$

$$\phi(x, 0) = V_{\text{gt}} - V_{\text{fbt}} + \frac{\epsilon_{\text{Si}}}{C_{\text{ox}1}} \frac{\partial \phi}{\partial y} \Big|_{y=0}, \quad \phi(x, t_{\text{Si}}) = V_{\text{gb}} - V_{\text{fbt}} + \frac{\epsilon_{\text{Si}}}{C_{\text{ox}2}} \frac{\partial \phi}{\partial y} \Big|_{y=t_{\text{Si}}}$$

where  $\varepsilon_{si}$  is the dielectric constant of silicon,  $V_{fbt}$  is the flat-band voltage of the top gate, and  $V_{fbb}$  is the flat-band voltage of the bottom gate.  $C_{ox1}$  and  $C_{ox2}$  are the gate oxide capacitances of the top and bottom sides, which can be expressed as follows.

$$\frac{1}{C_{ox1}} = \frac{1}{C_{SiO_2}} + \frac{1}{C_{\varepsilon_t}}, \quad \frac{1}{C_{ox2}} = \frac{1}{C_{SiO_2}} + \frac{1}{C_{\varepsilon_b}} \quad (2)$$

The potential distribution obtained from the above conditions is as follows from Ding's model [25].

$$\phi(x, y) = V_s + \frac{V_d x}{L_g} + \sum_{n=1}^{\infty} A_n(y) \sin \frac{n\pi x}{L_g} \quad (3)$$

$$A_n(y) = C_n e^{k_n y} + D_n e^{-k_n y} - f_n / k_n$$

$$f_n = \begin{cases} -\frac{4qN_d}{n\pi\varepsilon_{si}}, & n = 1, 3, 5, \dots \\ 0, & n = 2, 4, 6, \dots \end{cases}$$

$$C_n = C_{ox1} \left[ \frac{(\varepsilon_{si} k_n - C_{ox2})(f_n - G_n k_n^2) + r(C_{ox1} + \varepsilon_{si} k_n)(f_n - H_n k_n^2) e^{k_n t_{si}}}{r(C_{ox1} + \varepsilon_{si} k_n)(f_n - H_n k_n^2) e^{k_n t_{si}}} \right] / k_n^2 \left[ \frac{C_{ox1} \varepsilon_{si} k_n (1+r)(1 + e^{2k_n t_{si}}) - (C_{ox1} C_{ox2} + \varepsilon_{si}^2 k_n^2)(1 - e^{2k_n t_{si}})}{C_{ox1} C_{ox2} + \varepsilon_{si}^2 k_n^2} \right]$$

$$D_n = C_{ox1} e^{k_n t_{si}} \left[ \frac{(\varepsilon_{si} k_n + C_{ox2})(f_n - G_n k_n^2) e^{k_n t_{si}} - r(C_{ox1} - \varepsilon_{si} k_n)(f_n - H_n k_n^2)}{r(C_{ox1} - \varepsilon_{si} k_n)(f_n - H_n k_n^2)} \right] / k_n^2 \left[ \frac{C_{ox1} \varepsilon_{si} k_n (1+r)(1 + e^{2k_n t_{si}}) - (C_{ox1} C_{ox2} + \varepsilon_{si}^2 k_n^2)(1 - e^{2k_n t_{si}})}{C_{ox1} C_{ox2} + \varepsilon_{si}^2 k_n^2} \right]$$

$$G_n = \begin{cases} \left( \frac{2}{n\pi} \right) [2(V_s - V_{gt} + V_{fbt}) + V_d], & n = 1, 3, 5, \dots \\ 0, & n = 2, 4, 6, \dots \end{cases}$$

$$H_n = \begin{cases} \left( \frac{2}{n\pi} \right) [2(V_s - V_{gb} + V_{fbb}) + V_d], & n = 1, 3, 5, \dots \\ 0, & n = 2, 4, 6, \dots \end{cases}$$

$$r = C_{ox2} / C_{ox1}, \quad k_n = n\pi / L_g.$$

The subthreshold swing is defined as the change of the top gate voltage to the logarithmic value of the drain current and is expressed as follows.

$$SS = \frac{\partial V_{gt}}{\partial \log I_{ds}} = \ln(10) \left( \frac{kT}{q} \right) \left( \frac{\partial \phi_{\min}}{\partial V_{gt}} \right)^{-1} \quad (4)$$

The  $\partial \phi_{\min} / \partial V_{gt}$  in (4) is obtained from the derivative of the potential distribution with respect to  $V_{gt}$  as

$$\frac{\partial \phi_{\min}}{\partial V_{gt}} = \sum_{n=1}^{\infty} \frac{\partial A_n(y)}{\partial V_{gt}} \sin \left( \frac{n\pi x}{L_g} \right) \Bigg|_{x=x_{\min}, y=t_{si}/2} \quad (5)$$

$$\frac{\partial A_n(y)}{\partial V_{gt}} = e^{k_n y} \frac{\partial C_n}{\partial V_{gt}} + e^{-k_n y} \frac{\partial D_n}{\partial V_{gt}}$$

$$\frac{\partial C_n}{\partial V_{gt}} = \frac{4}{n\pi} \frac{C_{ox1}(\epsilon_{si}k_n - C_{ox2})}{C_{ox1}\epsilon_{si}k_n(1+r)\left(1+e^{2k_n t_{si}}\right) - (C_{ox1}C_{ox2} + \epsilon_{si}^2 k_n^2)(1-e^{2k_n t_{si}})}$$

$$\frac{\partial D_n}{\partial V_{gt}} = \frac{4}{n\pi} \frac{C_{ox1}(\epsilon_{si}k_n - C_{ox2})e^{2k_n t_{si}}}{C_{ox1}\epsilon_{si}k_n(1+r)\left(1+e^{2k_n t_{si}}\right) - (C_{ox1}C_{ox2} + \epsilon_{si}^2 k_n^2)(1-e^{2k_n t_{si}})}$$

In the case of the JLDG MOSFET, most of the drain current moves along the central axis, so  $x = x_{min}$  and  $y = t_{si}/2$  are substituted into (5) to obtain the  $\partial\phi_{min}/\partial V_{gt}$  [26]. As a result, the subthreshold swing model of (6) can be obtained from (4) and (5). The  $x_{min}$  is selected as the position having the minimum potential among the potential distributions of  $y = t_{si}/2$ .

$$SS = \ln(10) \left( \frac{kT}{q} \right) \left[ \sum_{n=1}^{\infty} \frac{4}{n\pi} \sin\left(\frac{n\pi x_{min}}{L_g}\right) \times \frac{C_{ox1} \left[ e^{k_n t_{si}/2} (\epsilon_{si} k_n - C_{ox2}) + e^{3k_n t_{si}/2} (\epsilon_{si} k_n + C_{ox2}) \right]}{C_{ox1} \epsilon_{si} k_n \left( 1 + \frac{t_{ox1}}{t_{ox2}} \right) \left( 1 + e^{2k_n t_{si}} \right) - (C_{ox1} C_{ox2} + \epsilon_{si}^2 k_n^2) \left( 1 - e^{2k_n t_{si}} \right)} \right]^{-1} \quad (n ; \text{odd number}) \quad (6)$$

where  $k$  is the Boltzmann constant and  $T$  is the absolute temperature. In addition, the condition of  $n = 30$  in which  $A_n$  of (3) sufficiently converges is used in (6).

Figure 2 shows the potential distribution along to the central axis obtained using (3) for the channel length of 20 nm, silicon thickness of 10 nm, and  $t_{ox1}(=t_{ox2})$  of 1 nm. As shown in Figure 2, it can be observed that there is a large change in the potential distribution when the dielectric constants of the top and bottom gate oxides change. Compared with  $\text{La}_2\text{O}_3$  having the dielectric constant of 30 and  $\text{SiO}_2$  of about 4 as the stacked top and the bottom gate oxides, it can be observed that the change of  $\phi_{min}$  in the potential distribution also increases as the dielectric constant increases for the same gate voltage change. Therefore, it can be seen from (4) that the subthreshold swing decreases as the dielectric constant of the stacked gate oxide film increases. Since the change in the dielectric constant of the stacked gate oxide directly affects the subthreshold swing, the variation of the subthreshold swing for the change of the dielectric constant of the stacked gate oxides at the top and bottom will be observed using (6) in this paper.

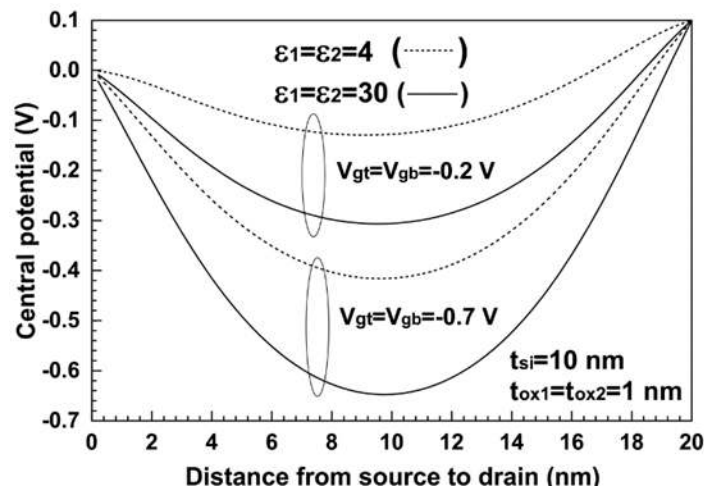


Figure 2. Central potential distribution for  $\epsilon_1 = \epsilon_2 = 4$  and  $\epsilon_1 = \epsilon_2 = 30$  with the top and bottom gate voltage as parameters of the asymmetric JLDG MOSFET

### 3. SUBTHRESHOLD SWING FOR THE STACKED HIGH-*k* MATERIALS

In order to prove the validity of (6), the results of the previous papers are compared with the subthreshold swings of this model in Figure 3. Even if the dielectric constants of the stacked top and bottom gate oxides are changed, it is found to be in good agreement with the model of other papers [23, 27]. Since each of the models is in good agreement with the two-dimensional simulations, (6) is valid. Therefore, we will analyze the subthreshold swing of the asymmetric JLDG MOSFET according to the dielectric constants of the stacked top and bottom gate oxide films using (6).

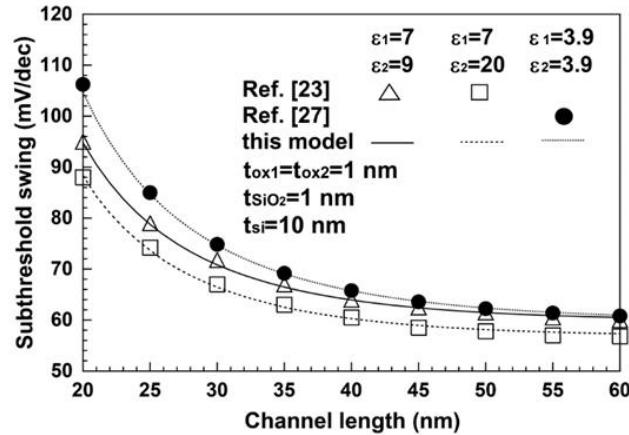


Figure 3. Comparisons with subthreshold swings of this model and the previous papers [23, 27] for the JLDG MOSFET

The change of the subthreshold swing is shown in Figure 4 when the thicknesses of the stacked top and bottom gate oxide films are the same as 1, 2, and 3 nm, and the dielectric constants are only different. As the thickness of the stacked oxide layer increases, the subthreshold swing increases. In addition, the subthreshold swing decreases as the dielectric constant of the stacked bottom gate oxide increases. The reason for this is that the total oxide capacitance increases as the dielectric constant increases, as shown in (2). The results are the same even if the dielectric constants at the stacked top and bottom are interchanged. As the thickness of the oxide layer is increased, the subthreshold swing is more affected by the dielectric constant of the bottom gate oxide. When the thickness of the oxide layer is reduced to 1 nm, the variation of the subthreshold swing due to the change of dielectric constant is hardly observed as shown in Figure 4. In addition, the rate of change of subthreshold swing according to the change of dielectric constant decreases as the channel length increases.

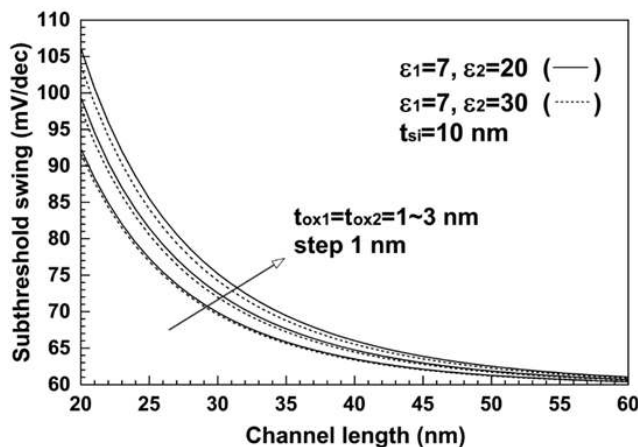


Figure 4. Subthreshold swings of this model with gate oxide thickness and dielectric constant as parameters for the asymmetric JLDG MOSFET

The asymmetric JLDG MOSFETs can be fabricated with different gate oxide thicknesses at the top and bottom. In Figure 5, the contour graph of the subthreshold swings according to the thickness change of the stacked top and bottom gate oxides is shown. The channel length is 20 nm and the silicon thickness is 10 nm.

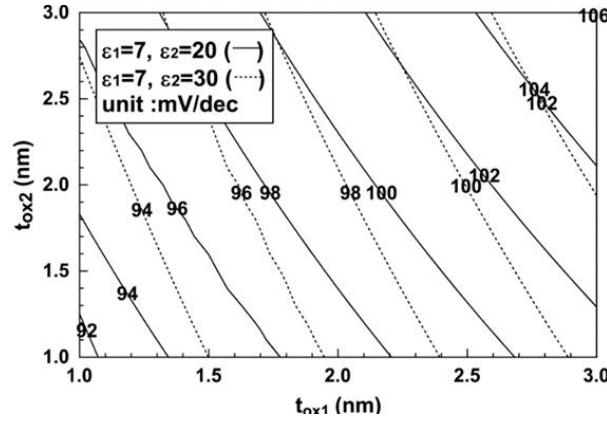


Figure 5. Contours of subthreshold swings for the stacked top and bottom gate oxide thicknesses with dielectric constants of the stacked top and bottom gate oxide as parameters for the asymmetric JLDG MOSFET

As shown in Figure 4, it can be observed that the subthreshold swing decreases at the same top and bottom gate oxide thicknesses as  $\epsilon_2$  increases. It can also be observed that  $t_{ox1}$  has a greater impact on subthreshold swings than  $t_{ox2}$ . That is, the subthreshold swing is more sensitive to the thickness of the oxide film having a small dielectric constant among the stacked oxide films. As the dielectric constant  $\epsilon_2$  at the bottom gate oxide increases, it can be observed that the subthreshold swing is less sensitive to the change in the thickness of the bottom gate oxide film. Therefore, the asymmetrical JLDG MOSFET will be able to control the subthreshold swing more efficiently than the symmetrical structure. That is, in the case of a dielectric material that is difficult to make thin, the process may be more easily performed while maintaining the same subthreshold swing if the thickness of the opposite oxide film is thinned.

In the relationship of Figure 5, it can be seen that the subthreshold swing increases linearly with the sum of the stacked top and bottom oxide thicknesses. Since the oxide thickness and the dielectric constant are inversely proportional to the capacitance, it can be seen empirically that the sum of the inverses of the dielectric constants is proportional to the subthreshold swing. In other words,

$$SS \propto \frac{1}{\epsilon_1} + \frac{1}{\epsilon_2} = \epsilon_{12} \tag{7}$$

Figure 6 shows the relationship between the sum of the reciprocals of the stacked oxide dielectric constants and the subthreshold swing with the channel length as a parameter, when the channel lengths are 15 nm, 20 nm or 30 nm. In Figure 6, the slope of the result of the linear fitting is shown in Table 1. As a result of observing the change of the subthreshold swing in the dielectric constant range (from 4 to 80) of the stacked top and bottom oxide films, it can be seen from Table 1 and Figure 6 that the subthreshold swing and the rate of change of the subthreshold swing ( $dSS/d\epsilon_{12}$ ) increases as the channel length decreases.

Therefore, as the channel length decreases, the dielectric constants of the stacked top and bottom oxide films will have a greater influence. It can be observed that the subthreshold swing of less than 100 mV/dec are difficult to obtain in the simulated dielectric constant range when the channel length is reduced to about 15 nm. Therefore, the variation of the subthreshold swing for silicon thickness as well as channel length is calculated and shown in Figure 7. If the silicon thickness is reduced, the subthreshold swing of less than 100 mV/dec can be obtained, despite of the channel length of 15 nm in the calculated dielectric constant range. As the thickness of the silicon decreases, it can be seen in Figure 7 and Table 1 that the subthreshold swing decreases and the rate of change of the subthreshold swing ( $dSS/d\epsilon_{12}$ ) decreases. Comparing Figure 6 and Figure 7, it can be observed that the change of silicon thickness has a greater influence on the subthreshold swing than that of the channel length. Therefore, more attention should be paid to the silicon thickness setting.

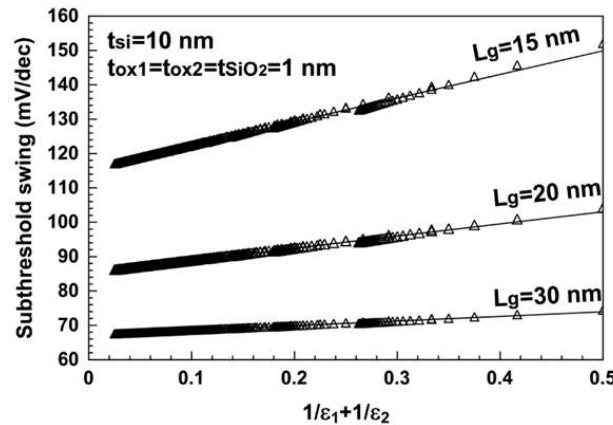


Figure 6. Subthreshold swings for the sum of the inverses of the dielectric constants for the stacked top and bottom gate oxide with the channel length as a parameter

Table 1. The rate of change of the subthreshold swing according to the change of the sum of the reciprocals of the stacked oxide dielectric constants for the channel length and silicon thickness

$t_{si}=10$ nm $L_g$ (nm)	$dSS/d\epsilon_{12}$ (mV/dec)	$L_g=15$ nm $t_{si}$ (nm)	$dSS/d\epsilon_{12}$ (mV/dec)
15	68.9	6	35.4
20	35.4	8	51.4
30	13.4	10	68.9

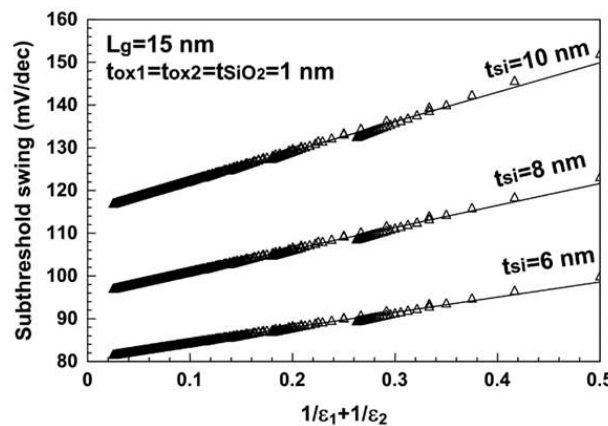


Figure 7. Subthreshold swings for the sum of the inverses of the dielectric constants for the top and bottom stacked gate oxide with the silicon thickness as a parameter

For the asymmetric JLDG MOSFETs, the gate voltages at the top and bottom can be applied differently. In the case of a junction-based DG MOSFET, the subthreshold swing increases as the top gate voltage decreases and as the bottom gate voltage increases [25]. In the case of the asymmetric JLDG MOSFET, the variation of subthreshold swing according to the top and bottom gate voltages is shown in Figure 8. The channel length is 20 nm and the silicon thickness is 10 nm, the thickness of not only SiO<sub>2</sub> at the top and bottom but also the thickness of the stacked oxide film is 1 nm. As shown in Figure 8, the subthreshold swing increases as the top gate voltage decreases and the bottom gate voltage increases with the asymmetric junction-based MOSFET. In Figure 8, the dots show the subthreshold swings when the top and bottom gate voltages are also the same and dielectric constants of the stacked top and bottom gate oxide layers are the same as 10. In the case of this symmetrical JLDG MOSFET, the same subthreshold swing value of 93 mV/dec is shown regardless of the applied gate voltage. However, in the asymmetric structure, that is, the subthreshold swing is changed as shown in Fig. 8 when the top and bottom gate voltages and the dielectric constants of the stacked gate oxide films are different. When the dielectric constant of the stacked bottom gate oxide film is larger than the dielectric constant of the stacked top gate oxide film,

the subthreshold swing decreases. Increasing the top gate voltage not only reduces the subthreshold swing but also decreases the rate of change in Figure 8. That is, in the case of  $V_{gt} = -0.7$  V, the subthreshold swing increases by about 62 mV/dec from 71 mV/dec to 133 mV/dec if the bottom gate voltage changes from -2 V to 0 V; however, the subthreshold swing increases only about 52 mV/dec from 61 mV/dec to 113 mV/dec in the case of  $V_{gt} = -0.3$  V. Therefore, the subthreshold swing can be reduced when the dielectric constant of the stacked bottom gate oxide film is larger than the stacked top gate dielectric constant and the bottom gate voltage is smaller than the top gate voltage applied.

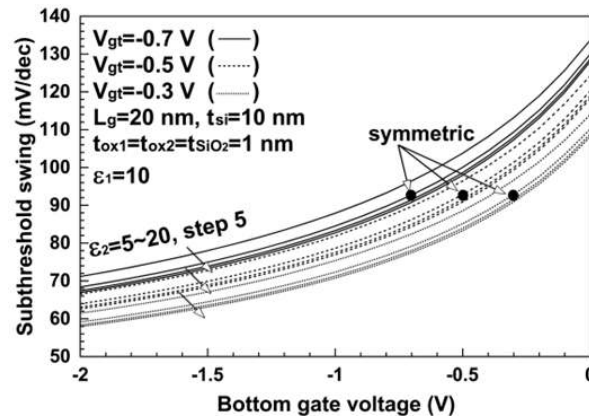


Figure 8. Subthreshold swings for the bottom gate voltage with the top gate voltage and the stacked gate dielectric constant of bottom side as parameters

#### 4. CONCLUSION

In this paper, the variation of the subthreshold swing was observed when the stacked gate oxide is used to reduce the short channel effects caused by scaling of the asymmetric JLDG MOSFET. For this purpose, we proposed an analytical subthreshold swing model, using the potential distribution derived from the Poisson equation. The analytical subthreshold swing model presented in this paper was in good agreement with the result of 2D numerical simulation and other papers. Using this model, the variation of the subthreshold swings for channel length, silicon thickness, and gate oxide thickness in a JLDG MOSFETs was observed using the dielectric constant as a parameter. As a result, the subthreshold swing was reduced when the dielectric constant of the stacked oxide film was larger than  $\text{SiO}_2$ . In addition, the subthreshold swing was more sensitive to the thickness of the oxide film having a smaller dielectric constant among the stacked top and bottom oxide films. When the top and bottom oxide films have the same structure, the subthreshold swing is more sensitive to the silicon thickness than the channel length. An advantage of the asymmetric structure is that the top and bottom gate voltages can be applied differently. When the bottom gate voltage was smaller than the top gate voltage, the subthreshold swing was lower than when the top and bottom gate voltages were the same. It was found that the subthreshold swing is proportional to the sum of the inverse of the dielectric constant of stacked oxides for top and bottom gate oxide, and the proportional constant decreases as the channel length increases and the silicon thickness decreases. As a result, it is observed that not only problems such as defects with the silicon interface caused by using the high- $k$  materials can be solved but also a subthreshold swing can be reduced when a high- $k$  materials are stacked with  $\text{SiO}_2$ .

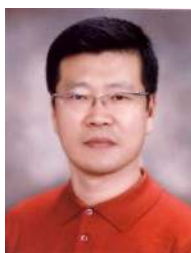
#### REFERENCES

- [1] C. Nistor, "Samsung begins mass production of the Exynos I T200 chip for IoT use," 2017. [Online]. Available: <https://www.notebookcheck.net/Samsung-begins-mass-production-of-the-Exynos-i-T200-chip-for-IoT-use.229970.0.html>.
- [2] D. Schor, "VLSI 2018: Samsung's 8 nm 8LPP, a 10 nm extension," 2018. [Online]. Available: <https://fuse.wikichip.org/news/1443/vlsi-2018-samsungs-8nm-8lpp-a-10nm-extension/>.
- [3] E. Kim, "Samsung Electronics to Accelerate Investment in Semiconductors," 2019. [Online]. Available: <http://www.businesskorea.co.kr/news/articleView.html?idxno=37562>.
- [4] Y. Wang, et al., "High performance of junctionless MOSFET with asymmetric gate," *Superlattices and Microstructures*, vol. 97, pp. 8-14, 2016.
- [5] L. Chen, et al., "The Physical analysis on electrical junction of junctionless FET," *AIP ADVANCES*, vol. 7, no. 2, pp. 025301-1-5, 2017.



- [6] Y. H. Shin, et al., "Analytical Model for Junctionless Double-Gate FET in Subthreshold Region," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1433-1440, 2017.
- [7] K. E. Kaharudin, et al., "Geometric and process design of ultra-thin junctionless double gate vertical MOSFETs," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 9, no. 4, pp. 2863-2873, 2019.
- [8] Q. Xie, et al., "Analysis of Short-Channel Effects in Junctionless DG MOSFETs," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3511-3514, 2017.
- [9] H. Jung, "Analysis of Threshold Voltage Roll-Off and Drain Induced Barrier Lowering in Junction-Based and Junctionless Double Gate MOSFET," *Journal of Korean Institute of Electrical and Electronic Material Engineers*, vol. 32, no. 2, pp. 104-109, 2019.
- [10] Y. Wang, et al., "High performance of junctionless MOSFET with asymmetric gate," *Superlattices and Nanostructures*, vol. 97, pp. 8-14, 2016.
- [11] A. N. M. Khatir, et al., "3D Simulation of Fin Geometry Influence on Corner Effect in Multifin Dual and Tri-gate SOI-FinFETs," *TELKOMNIKA Indonesian Journal of Electrical Engineering*, vol. 12, no. 4, pp. 3253-3256, 2014.
- [12] K. E. Kaharudin, et al., "Analysis of analog and RF behaviors in junctionless double gate vertical MOSFET," *Bulletin of Electrical Engineering and Informatics (BEEI)*, vol. 9, no. 1, pp. 101-108, 2020.
- [13] F. Merad and A. Guen-Bouazza, "DC performance analysis of a 20 nm gate length n-type Silicon GAA junctionless (Si-JL-GAA) transistor," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 10, no. 4, pp. 4043-4052, 2020.
- [14] K. E. Kaharudin, et al., "Performance analysis of ultrathin junctionless double gate vertical MOSFETs," *Bulletin of Electrical Engineering and Informatics (BEEI)*, vol. 8, no. 4, pp. 1268-1278, 2019.
- [15] R. Shanker, et al., "A Degradation Model of Double Gate and Gate-All-Around MOSFETs With Interface Trapped Charges Including Effects of Channel Mobile Charge Carriers," *IEEE Transactions on Device and Materials Reliability*, vol. 14, no. 2, pp. 689-697, 2014.
- [16] I. Hussain, et al., "A Unified Approach for Performance Degradation Analysis from Transistor to gate Level," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 8, no. 1, pp. 412-420, 2018.
- [17] V. Kumar, et al., "Performance Analysis of Double Gate n-FinFET Using High-k Dielectric Materials," *International Journal of Innovative Research in Science, Engineering and Technology*, vol. 5, no. 7, pp. 13242-13249, 2016.
- [18] A. Balhara and D. Punia, "Design and Analysis of Double Gate MOSFET Devices using High-k Dielectric," *International Journal of Electrical Engineering*, vol. 7, no. 1, pp. 53-60, 2014.
- [19] J. Ajayan, et al., "Analysis of nanometer-scale InGaAs/InAs/InGaAs composite channel MOSFETs using high-k dielectric for high speed applications," *International Journal of Electronics and Communications*, vol. 79, pp. 151-157, 2017.
- [20] S. C. Wagaj and S. C. Patil, "Comparison study of Dual Material Gate Silicon on Insulator junctionless Transistor and with Junction Transistor for Analog Performance," *International Journal of Materials, Mechanics and Manufacturing*, vol. 7, no. 3, pp. 144-149, 2019.
- [21] V. Pathak and G. Saini, "A Graded Channel Dual-Material Gate Junctionless MOSFET for Analog Applications," *Procedia Computer Science*, vol. 125, pp. 825-831, 2018.
- [22] S. C. Wagaj and S. C. Patil, "Analytical current Model for Dual Material Double Gate Junctionless Transistor," *Indonesian Journal of Electrical Engineering and Information*, vol. 7, no. 3, pp. 555-563, 2019.
- [23] M. S. Islam, et al., "Modelling and Performance Analysis of Asymmetric Double Gate Stack-Oxide Junctionless FET in Subthreshold Region," *International Journal of Mathematics and Computers in Simulation*, vol. 11, pp. 116-120, 2017.
- [24] G. L. Priya and N. B. Balamurugan, "New dual material double gate junctionless tunnel FET: Subthreshold modeling and simulation," *International Journal of Electronics and Communications*, vol. 99, pp. 130-138, 2019.
- [25] Z. Ding, et al., "An analytic model for channel potential and subthreshold swing of the symmetric and asymmetric double-gate MOSFETs," *Microelectronics Journal*, vol. 42, no. 3, pp. 515-519, 2011.
- [26] T. A. Oproglidis, et al., "Analytical drain current compact model in the depletion operation region of short-channel triple-gate junctionless transistors," *IEEE Transactions on Electron Devices*, vol. 64, no. 1, pp. 66-72, 2017.
- [27] C. Jiang, et al., "A two-dimensional analytical model for short channel junctionless double-gate MOSFETs," *AIP ADVANCES*, vol. 5, no. 5, pp. 057122-1-13, 2015.

## BIOGRAPHY OF AUTHOR



**Prof. Hak Kee Jung** received the B.S. degree from Ajou University, Korea, in 1983, the M.S. and Ph.D. degrees from Yonsei University, Seoul, Korea, in 1985, 1990, respectively, all in electronic engineering. In 1990, he joined Kunsan National University, Chonbuk, Korea, where he is currently a Professor in department of electronic engineering. From 1995 to 1995, he held a research position with the Electronic Engineering Department, Osaka University, Osaka, Japan. From 2004 to 2005, and 2016 to 2017, he was with the School of Microelectronic Engineering, Griffith University, Nathan, QLD, Australia. His research interests include semiconductor device physics and device modeling with a strong emphasis on quantum transport and Monte Carlo simulations.