Analysis of Temporal Noise in CMOS Photodiode Active Pixel Sensor

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***Abstract*—Temporal noise sets the fundamental limit on image sensor performance, especially under low illumination and in video applications. In a CCD image sensor, temporal noise is primarily due to the photodetector shot noise and the output amplifier thermal and $1/f$ noise. CMOS image sensors suffer from higher noise than CCDs due to the additional pixel and column amplifier transistor thermal and $1/f$ noise. Noise analysis is further complicated by the time-varying circuit models, the fact that the reset transistor operates in subthreshold during reset, and the nonlinearity of the charge to voltage conversion, which is becoming more pronounced as CMOS technology scales. The paper presents a detailed and rigorous analysis of temporal noise due to thermal and shot noise sources in CMOS active pixel sensor (APS) that takes into consideration these complicating factors. Performing time-domain analysis, instead of the more traditional frequency-domain analysis, we find that the reset noise power due to thermal noise is at most half of its commonly quoted kT/C value. This result is corroborated by several published experimental data including data presented in this paper. The lower reset noise, however, comes at the expense of image lag. We find that alternative reset methods such as overdriving the reset transistor gate or using a pMOS transistor can alleviate lag, but at the expense of doubling the reset noise power. We propose a new reset method that alleviates lag without increasing reset noise.**

***Index Terms*—CMOS APS, image sensor, reset noise, shot noise, subthreshold operation, temporal noise, time-domain noise analysis.**

I. Introduction

TEMPORAL noise sets the fundamental limit on image sensor performance, especially under low illumination and in video applications. In a CCD image sensor, temporal noise is primarily due to the photodetector shot noise and the output amplifier thermal and $1/f$ noise. In a CMOS active pixel sensor (APS) several additional sources contribute to temporal noise. These include the pixel reset, follower, and access transistor thermal, shot, and $1/f$ noise and the column amplifier thermal and $1/f$ noise. Hand analysis of the noise in CCDs and CMOS APS have been published by several authors [1]–[7]. Their analysis shows that at low illumination the dominant source of noise is reset and readout transistors, while at high illumination the dominant source of noise is the photodiode shot noise. The noise power due to the reset transistor, which is sampled at the end of reset, is often quoted to be $(kT/C)V^2$. Several authors [8], [9], however, reported that the measured reset noise is significantly smaller than kT/C. In analyzing noise due to photodiode shot noise, one typically assumes that the photodiode charge to voltage relation is linear. As supply voltage scales with CMOS technology, this relation, however, becomes increasingly nonlinear.

In this paper, we present a detailed and rigorous analysis of noise due to thermal and shot noise sources in photodiode APS that takes into consideration these complicating factors. We show that during reset the reset transistor operates in subthreshold and steady state is not achieved. As a result, the conventional frequency domain noise analysis method cannot be applied. To calculate reset noise power we consider the time-varying reset circuit model and perform *time-domain* noise analysis using the MOS transistor subthreshold noise model [10]. We show that reset noise power is at most half of its commonly quoted kT/C value, which corroborates the published experimental results. The lower reset noise, however, comes at the expense of image lag. Since steady state is not reached during reset, the final photodiode reset voltage depends on its initial value. This problem can be alleviated by overdriving the gate of the reset transistor or by using a pMOS instead of an nMOS transistor for reset. These techniques, however, double the reset noise power. We propose a new "pseudo-flash" reset method, which can alleviate image lag without increasing reset noise. A similar technique was independently developed by Pain *et al.* [11]. We then present an analysis of photodiode shot noise that takes into consideration the nonlinearity of the photodiode charge to voltage conversion. We again perform time-domain noise analysis using a time-varying circuit model. We find that the nonlinearity actually improves the signal-to-noise ratio (SNR) at high illumination. We present experimental results from test structures fabricated in 0.35-μ CMOS processes. We find that the measured reset noise mean square value is indeed close to $kT/2C$, and that the measured SNR value matches well with our hand analysis.

The rest of the paper is organized as follows. In Section II we describe the circuit and operation of the photodiode APS analyzed in the paper. In Section III we present our analysis of reset noise. In Section IV we discuss the image lag due to incomplete reset and present our pseudo-flash reset method. In Section V we present the analysis of the photodiode shot noise that takes into consideration the nonlinearity of the photodiode charge to voltage conversion. For completeness, in Section VI

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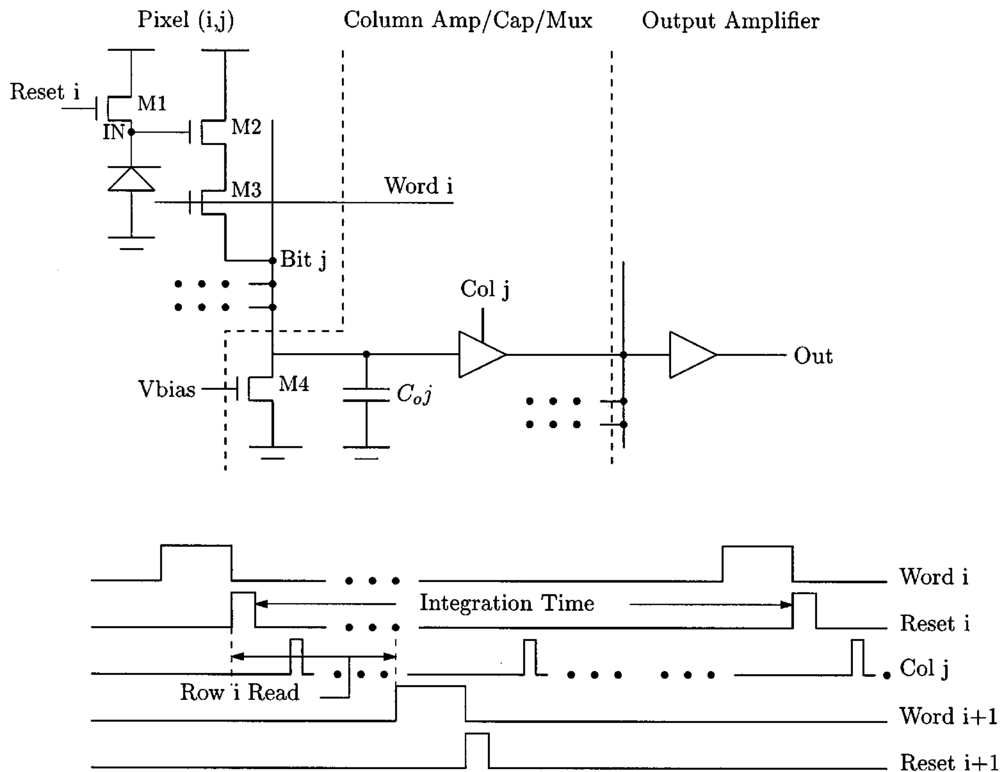

Fig. 1. APS circuit and timing diagram.

we use HSPICE to estimate the noise contributions of the follower, access and column amplifier transistors. We find that the contributions of these transistors to the noise is negligible compared to reset and photodiode shot noise. Finally, in Section VII, we present our experimental results.

We note here that this paper provides a more complete treatment of our results than our earlier conference paper [12]. In particular, the conference paper did not contain any of the key derivations, included only partial testing results, and did not address reset induced image lag or discuss the pseudo-flash reset scheme.

II. Photodiode APS Circuit and Operation

The photodiode APS circuit we analyze in this paper is shown in Fig. 1. Each pixel comprises a photodiode, a reset transistor M1, a source follower transistor M2, and an access transistor M3. Column circuits include a bias transistor M4, which acts as the source-follower amplifier current source, and a storage capacitor C_o. The operation of the sensor is described in Fig. 1. The sensor is read out one row at a time. At the end of each row's integration time, the pixel values are stored in the column capacitors C_{oj}. The row is then reset and the stored pixel values are read out via the column multiplexer. Correlated double sampling, which is typically performed to reduce fixed pattern noise (FPN), is not shown in the timing diagrams. Its effect on temporal noise can be readily analyzed using the results derived in the paper.

We are interested in finding the input-referred rms noise value in volts. To compute it, we sum up the input-referred noise power contributions of each phase of the APS operation, i.e., reset, integration, and readout. Noise generated during reset and integration are sampled onto C_o, and then transferred to the output during readout. We do not analyze the effect of the $1/f$ noise due to the photodetector and reset transistor here. We also ignore the fact that the reset noise voltage decays during integration and before it is sampled.

III. Noise During Reset

During reset, the gate of the reset transistor M1 is set to a high voltage, typically v_{dd}. At the beginning of reset, M1 is either operating in the saturation region or in subthreshold depending on the photodiode voltage at the end of integration. If the photodiode voltage is low enough, M1 is in saturation at first and for a very short amount of time before it goes into subthreshold for the rest of reset.

The circuit noise model during reset is shown in Fig. 2. The current source $I_d(t)$ models the transistor shot noise, while the current source $I_s(t)$ models the shot noise due to photodiode dark current i_{dc} and photocurrent i_{ph}. In subthreshold, $I_d(t)$ can be modeled as a white Gaussian noise process with the two-sided power spectral density (PSD) [10]

$$S_{I_{\mathrm{d}}}(f) = q i_{\mathrm{d}} \mathrm{A}^2/\mathrm{Hz} \tag{1}$$

where i_{d} is the drain current of M1. The photodiode noise source $I_s(t)$ is also mainly due to shot noise and has the PSD

$$S_{I_s}(f) = q(i_{\mathrm{ph}} + i_{\mathrm{dc}}) \mathrm{A}^2/\mathrm{Hz}. \tag{2}$$

If the reset time t_r is sufficiently greater than the settling time t_{settle}, i.e., the time at which the transistor subthreshold current

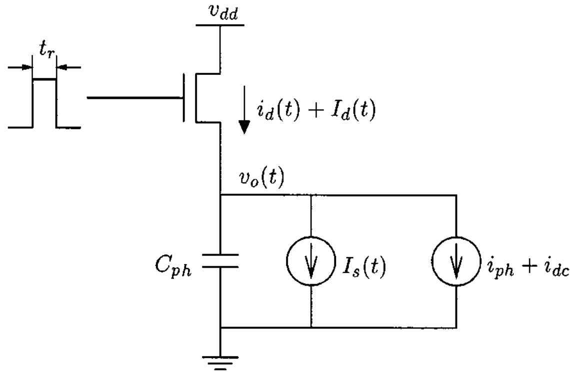

Fig. 2. APS circuit noise model during reset.

i_d equals the photodiode current $i_{\rm ph} + i_{\rm dc}$, then steady state is achieved and the average reset noise power is given by

$$\overline{V_n^2} = \int_{-\infty}^{\infty} \frac{2q(i_{\rm ph} + i_{\rm dc})}{(g_{m1} + g_{mb1})^2} \frac{1}{1 + \left(2\pi f \frac{C_{\rm ph}}{(g_{m1} + g_{mb1})}\right)^2} df \tag{3}$$

where g_{m1} and g_{mb1} are the transconductances of M1 in subthreshold, and the factor of 2 is due to the fact that in steady state $i_{\rm d} = i_{\rm ph} + i_{\rm dc}$. Performing the integral we get that

$$\overline{V_n^2} = \frac{q(i_{\rm ph} + i_{\rm dc})}{C_{\rm ph}(g_{m1} + g_{mb1})}. \tag{4}$$

Since in subthreshold $i_d = (kT/q)(g_{m1} + g_{mb1})$, we get $\overline{V_n^2} = (kT/C_{\rm ph})$, which is the same as the often quoted reset noise value.

This analysis, however, holds only if steady state is achieved during reset, which can only occur if the settling time is shorter than the reset time. To find out whether the circuit is in steady state, we need compute the settling time $t_{\rm settle}$. Applying Kirchhoff's current law we get that

$$\frac{dV_{\rm ph}(t)}{dt} = \frac{i_d(t) + I_n(t) - i_{\rm ph} - i_{\rm dc}}{C_{\rm ph}\left(V_{\rm ph}(t)\right)} \tag{5}$$

where $I_n(t) = I_d(t) + I_s(t)$ and $V_{\rm ph}$ is the photodiode voltage. Assuming that the signal is much larger than the noise we can express the photodiode voltage during reset as the sum of a signal voltage $v_{\rm ph}(t)$ and a noise voltage $V_n(t)$, i.e., $V_{\rm ph}(t) = v_{\rm ph}(t) + V_n(t)$, and approximate the capacitance $C_{\rm ph}(V_{\rm ph}(t)) \approx C_{\rm ph}(v_{\rm ph}(t))$. With these approximations, we can write the signal part of (5) as

$$\frac{dv_{\rm ph}(t)}{dt} = -\frac{i_{\rm ph} + i_{\rm dc}}{C_{\rm ph}\left(v_{\rm ph}(t)\right)} + \frac{i_{\rm d}\left(v_{\rm ph}(t)\right)}{C_{\rm ph}\left(v_{\rm ph}(t)\right)}. \tag{6}$$

Solving this equation, as detailed in Appendix A, we get the graph in Fig. 3, which shows that the settling time $t_{\rm settle} \geq$ 1 ms even for very high photocurrents. This settling time is much larger than the typical reset time, which is typically in the few microseconds range. Therefore steady state is not achieved during reset and we must analyze the reset noise for a time-varying circuit using time-domain analysis. We first note that i_d is a function of $(v_{\rm ph}(t) + V_n(t))$. Linearizing around the

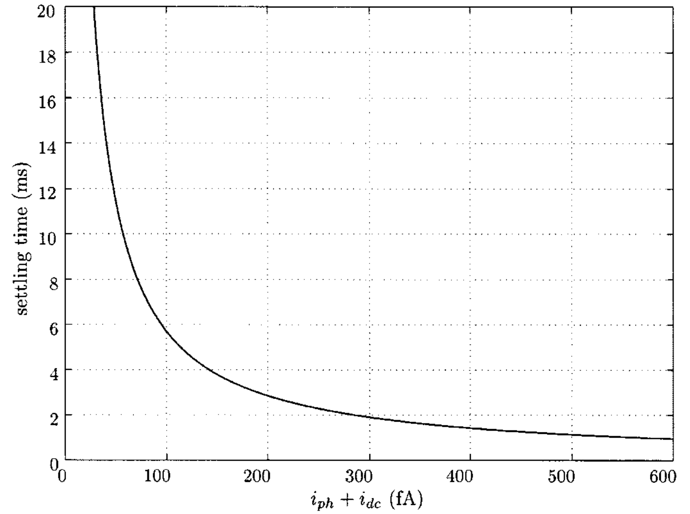

Fig. 3. Reset settling time $t_{\rm settle}$ versus photodiode current.

signal voltage $v_{\rm ph}(t)$ we get that $i_d(t) \approx i_d(v_{\rm ph}(t)) - g(t)V_n(t)$, where $g(t) = -(di_d/dv_{\rm ph})$ is the total transistor transconductance. The noise part of (5) is thus given by

$$I_n(t) = C_{\rm ph}\left(v_{\rm ph}(t)\right) \frac{dV_n(t)}{dt} + g(t)V_n(t). \tag{7}$$

Note that this is a general first-order linear differential equation and the solution at the end of reset can be expressed as a functional of the noise source current

$$V_n(t_r) = \int_0^{t_r} \frac{I_n(\tau)}{C_{\rm ph}(\tau)} \exp\left(-\int_\tau^{t_r} \frac{g(\tau_0)}{C_{\rm ph}(\tau_0)} d\tau_0\right) d\tau. \tag{8}$$

When the noise autocorrelation function is a δ function, which is the case for thermal and shot noise, we get that

$$\overline{V_n^2(t_r)} = \int_0^{t_r} \frac{R(\tau)}{C_{\rm ph}^2(\tau)} \exp\left(-2\int_\tau^{t_r} \frac{g(\tau_0)}{C_{\rm ph}(\tau_0)} d\tau_0\right) d\tau \tag{9}$$

where $R(\tau)$ is the PSD of the (white) noise source. For a more general noise process, a similar formula was derived in [13]. It can be readily verified from (9) that the contribution from the noise above threshold is extremely small, and can thus be ignored. We can also ignore the shot noise associated with $i_{\rm ph} + i_{\rm dc}$, since these currents are much smaller than the reset transistor drain current. With these simplifying assumptions, $R(\tau) = qi_d(\tau)$, and $C_{\rm ph}(\tau)$ is a constant, which we denote by $C_{\rm ph}$.

To find $\overline{V_n^2(t_r)}$, we need to evaluate the inner integral in (9). To calculate $g(t)$, we need to calculate the signal voltage $v_{\rm ph}(t)$ using (28) as detailed in Appendix A. Given that $i_{\rm ph} + i_{\rm dc} \ll i_d(t)$, we can approximate (28) by

$$v_{\rm ph}(t) \approx v_T \ln\left(\frac{K_0 t}{v_T C_{\rm ph}} + e^{(v_1/v_T)}\right) \tag{10}$$

where $v_T = kT/q$, $K_0 = (W/L)I_0 e^{(v_g\kappa/v_T)}$, v_1 is the transition voltage, and $t = 0$ corresponds to the time when the reset transistor enters subthreshold. We let $\delta = (v_T C_{\rm ph}/i_{\rm d}(0))$ be the *thermal time*, i.e., the time to charge the photodiode capacitance

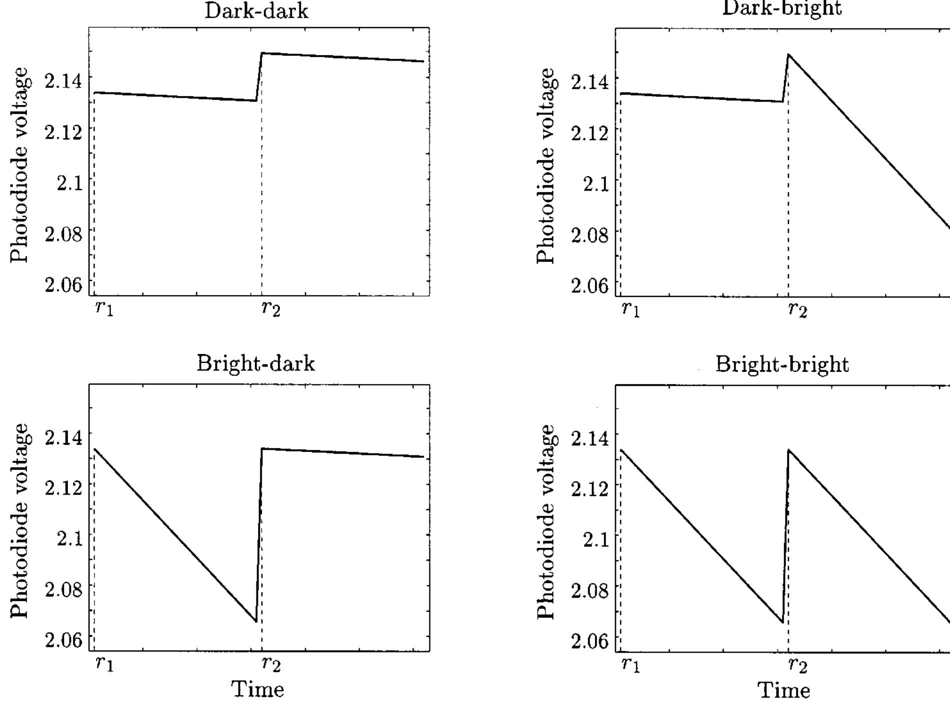

Fig. 4. Simulated photodiode voltage waveform due to incomplete reset. r_1 and r_2 refer to the end of reset for the first and second frames, respectively.

to v_T using $i_{\rm d}(0)$. Substituting in the I–V characteristics of the MOS transistor in subthreshold, we get that

$$i_{\rm d}(\tau) \approx \frac{v_T C_{\rm ph}}{\tau + \delta}. \tag{11}$$

Now evaluating the inner integral in (9) with $t_r - t_1$ replacing t_r, and $g(t) = (i_{\rm d}(t)/v_T)$ we get that

$$\int_\tau^{t_r - t_1} \frac{g(\tau_0)}{C_{\rm ph}(\tau_0)}\, d\tau_0 = \int_\tau^{t_r - t_1} \frac{1}{\tau_0 + \delta}\, d\tau_0 = \ln \frac{t_r - t_1 + \delta}{\tau + \delta}. \tag{12}$$

Substituting into (9), we get that the mean square noise voltage at the end of reset is given by

$$\overline{V_n^2(t_r)} = \frac{1}{2}\frac{kT}{C_{\rm ph}}\left(1 - \frac{\delta^2}{(t_r - t_1 + \delta)^2}\right). \tag{13}$$

Thus the mean square reset noise voltage is less than $1/2$ of the often quoted $kT/C_{\rm ph}$ value. Since t_r is typically in the few microsecond range, while $t_1 \leq 0.2$ ns and $\delta \approx 6$ ns for our test structure circuit, the mean square reset noise voltage value is in fact very close to $kT/2C_{\rm ph}$. For example, assuming $C_{\rm ph} = 22$ fF, which is consistent with the circuit in our test structure discussed in Section VII, we get an input-referred rms reset noise voltage of 303 μV at room temperature.

The intuitive reason for the $kT/2C_{\rm ph}$ result is twofold. First, by inspecting (9) we see that the noise decays exponentially while it is being integrated onto $C_{\rm ph}$. In subthreshold where the transistor I–V relation is exponential, the decay and integration balance each other and the circuit is in "virtual" steady state. The second reason is that in the case we are considering, shot noise due to the reset transistor drain current dominates, which in steady state contributes only $kT/2C_{\rm ph}$ [14]. Now, if reset time is long enough, steady state is eventually reached and, as mentioned earlier, the noise power becomes $kT/C_{\rm ph}$. This can be verified using conventional frequency-domain analysis or time-domain analysis as detailed in Appendix B.

IV. Image Lag Due to Incomplete Reset

In the previous section, we found that reset noise power is at most half of its commonly quoted kT/C value. This reduction in noise, however, comes at the expense of image lag. Since steady state is not reached, the final reset voltage can depend on the photodiode voltage at the beginning of reset resulting in image lag.[1] In this section, we explore the image lag problem, and propose a new reset method, which alleviates lag without increasing reset noise.

To analyze image lag, we assume the standard APS circuit and operation described in Section II. In Fig. 4, we plot the simulated photodiode voltage waveform for four different frame-to-frame illumination conditions assuming integration time $t_{\rm int} =$ 30 ms, reset time $t_r = 1\,\mu$s, dark current $i_{\rm dc} = 2.3$ fA, and bright level photocurrent $i_{\rm ph} = 50$ fA. The *bright* condition in the figure refers to the case where the photodiode voltage at the end of integration is low enough so that at the beginning of the next reset, the reset transistor operates above threshold.

As can be seen, if the first frame is bright, then the final reset voltages for the two frames are the same. On the other hand, if the first frame is dark, the final reset voltage for the second frame is noticeably different from that of the first frame, resulting in image lag. To see why, note that at the beginning of reset, following a bright frame, the reset transistor operates

[1]Note that the source of image lag here is different from the source of image lag in CCDs, which is very well studied. In CCDs image lag is caused by incomplete charge transfer. This can be eliminated using a pinned photodiode [15].

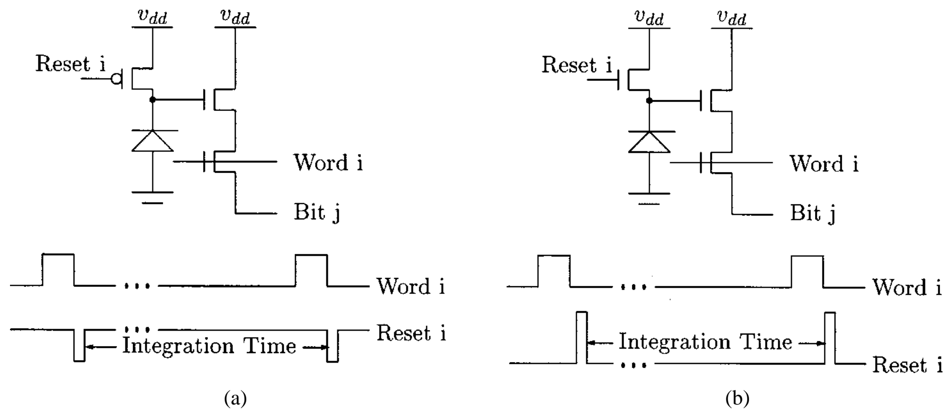

Fig. 5. (a) PMOS and (b) overdriving gate reset methods.

above threshold (for $\leq$0.2 ns). Therefore it reaches the transition voltage v_1 very quickly and spends almost all of the reset time in subthreshold. Thus, the final reset voltage is virtually independent of the initial photodiode voltage. For example, assuming a 1 μs reset time, the final reset voltage can only vary by at most 5 μV as a function of the brightness of the previous frame, which is much smaller than the reset noise.

Reset induced image lag can be eliminated using a pMOS reset transistor or by overdriving the reset transistor gate as shown in Fig. 5. In both cases, the reset transistor operates in the linear region during reset. Thus the final reset voltage is v_{dd}, independent of the initial photodiode voltage, and lag is eliminated. However, reset noise is significantly increased. First, the noise due to the reset transistor is increased to $kT/C_{\rm ph}$. Second, noise may be introduced due to the resistive coupling to the supply voltage [9]. Using a pMOS transistor also has the disadvantage of increased pixel area.

To achieve both low reset noise and low lag, we propose the new reset method shown in Fig. 6. The reset transistor drain is connected to a signal called Reset_dr instead of directly to the supply voltage v_{dd}. As shown in the figure, Reset_dr is dropped to a low voltage, e.g., ground, at the beginning of reset. This "pseudo-flash" operation ensures that the reset transistor always starts above threshold, thus eliminating lag. At the same time, reset noise is not increased and is still equal to $kT/2C_{\rm ph}$.

V. Noise During Integration

During integration, shot noise due to the dark current $i_{\rm dc}$ and photocurrent $i_{\rm ph}$ dominates, with PSD $S_{I_s}(f) = q(i_{\rm ph} + i_{\rm dc})$ A^2/Hz. To analyze noise generated during integration we again consider (5) but with the reset transistor turned off. If we assume that the photodiode capacitance is constant over the integration time, it is easy to show that the mean square value of the noise voltage sampled at the end of integration, i.e., at $t_{\rm int}$, is given by

$$\overline{V_n^2(t_{\rm int})} = \frac{q(i_{\rm ph} + i_{\rm dc})}{C_{\rm ph}^2} t_{\rm int}. \qquad (14)$$

The photodiode capacitance, however, is a function of its reverse bias voltage and can thus change significantly over integration time. So again we need to perform time-domain noise analysis.

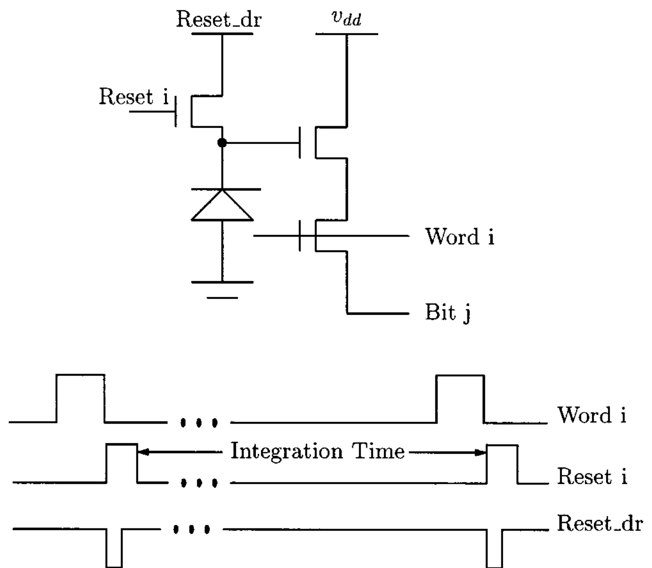

Fig. 6. Proposed pseudo-flash reset method.

Assuming that the noise is much smaller than the signal, we can write the noise part of (5) as

$$I_n(t) = I_s(t) = C_{\rm ph}(v_{\rm ph}(t)) \frac{dV_n(t)}{dt} + g_c(t)V_n(t) \qquad (15)$$

where $g_c(t) = -(1/C_{\rm ph}(v_{\rm ph}(t)))\,(dC_{\rm ph}(v_{\rm ph}(t))/dv_{\rm ph}(t))$ $(i_{\rm ph} + i_{\rm dc})$ is the varying capacitance induced conductance. This again is a general first-order linear differential equation and the mean square value of V_n at the end of integration is given by

$$\begin{aligned}\overline{V_n^2(t_{\rm int})} = {} & q(i_{\rm ph} + i_{\rm dc}) \int_0^{t_{\rm int}} \frac{1}{C_{\rm ph}^2(v_{\rm ph}(\tau))} \\ & \cdot \exp\Big(-2(i_{\rm ph} + i_{\rm dc}) \\ & \cdot \int_\tau^{t_{\rm int}} \frac{d(1/C_{\rm ph}(v_{\rm ph}(\tau_0)))}{dv_{\rm ph}(\tau_0)} d\tau_0\Big)\, d\tau. \qquad (16)\end{aligned}$$

Note that (14) follows from this more general equation if we assume that $C_{\rm ph}$ is constant during integration. To take the dependency of the photodiode capacitance on the reverse bias voltage

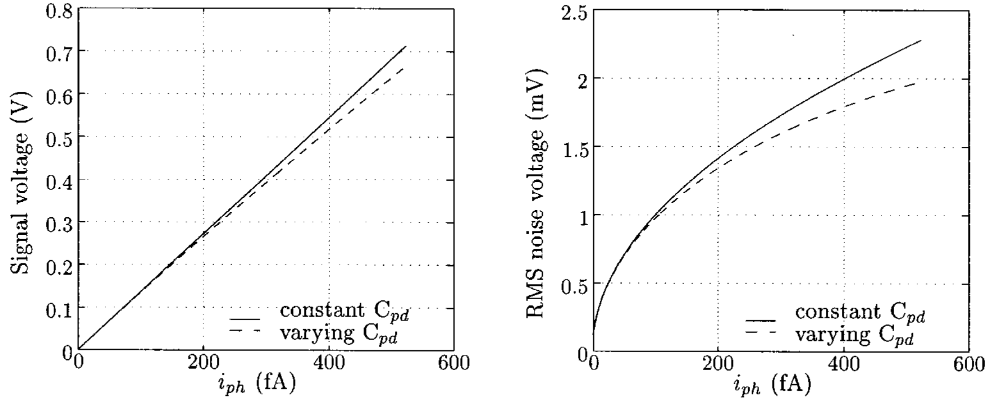

Fig. 7. Signal and noise levels as functions of input photocurrent.

into consideration, we make the simplifying assumption of an abrupt pn-junction to get that

$$C_{\mathrm{ph}}(v_{\mathrm{ph}}(t)) = C_{\mathrm{ph}}(v_{\mathrm{ph}}(0))\sqrt{\frac{v_{\mathrm{ph}}(0)+\phi}{v_{\mathrm{ph}}(t)+\phi}} \tag{17}$$

where ϕ is the built-in junction potential, and $v_{\mathrm{ph}}(0)$ is the voltage on C_{ph} at the beginning of integration. Solving the signal part of (5) during integration, we find that

$$v_{\mathrm{ph}}(t) = v_{\mathrm{ph}}(0) - \frac{(i_{\mathrm{ph}}+i_{\mathrm{dc}})}{C_{\mathrm{ph}}(v_{\mathrm{ph}}(0))}t + \frac{(i_{\mathrm{ph}}+i_{\mathrm{dc}})^2 t^2}{4C_{\mathrm{ph}}^2(v_{\mathrm{ph}}(0))(v_{\mathrm{ph}}(0)+\phi)}. \tag{18}$$

The square term in (18) shows that the signal is actually reduced by the nonlinearity. We can now explicitly express $C_{\mathrm{ph}}(v_{\mathrm{ph}}(t))$ as a function of t to get

$$C_{\mathrm{ph}}(v_{\mathrm{ph}}(t)) = C_{\mathrm{ph}}(v_{\mathrm{ph}}(0))\frac{1}{1-\dfrac{(i_{\mathrm{ph}}+i_{\mathrm{dc}})t}{2C_{\mathrm{ph}}(v_{\mathrm{ph}}(0))(v_{\mathrm{ph}}(0)+\phi)}}. \tag{19}$$

Thus we have

$$\frac{d(1/C_{\mathrm{ph}}(v_{\mathrm{ph}}(t)))}{dv_{\mathrm{ph}}(t)} = \frac{1}{C_{\mathrm{ph}}(v_{\mathrm{ph}}(0))}\frac{1}{2(v_{\mathrm{ph}}(0)+\phi)-\dfrac{i_{\mathrm{ph}}+i_{\mathrm{dc}}}{C_{\mathrm{ph}}(v_{\mathrm{ph}}(0))}t}. \tag{20}$$

Substituting (18)–(20) into (16), we get that the mean square noise voltage at the end of integration is given by

$$\overline{V_n^2(t_{\mathrm{int}})} = \frac{q(i_{\mathrm{ph}}+i_{\mathrm{dc}})}{C_{\mathrm{ph}}^2(v_{\mathrm{ph}}(0))}t_{\mathrm{int}} \cdot \left(1-\frac{1}{2(v_{\mathrm{ph}}(0)+\phi)}\frac{i_{\mathrm{ph}}+i_{\mathrm{dc}}}{C_{\mathrm{ph}}(v_{\mathrm{ph}}(0))}t_{\mathrm{int}}\right)^2. \tag{21}$$

To demonstrate the effect of varying capacitance during integration, we consider an example with $v_{\mathrm{ph}}(0) = 2.1$ V, $C_{\mathrm{ph}}(v_{\mathrm{ph}}(0)) = 22$ fF, $i_{\mathrm{dc}} = 2.28$ fA, $\phi = 0.7$V, and $t_{\mathrm{int}} = 30$ ms. These numbers are consistent with the parameters of our test structure circuit and experiments. Fig. 7 plots the signal $v_{\mathrm{ph}}(t_{\mathrm{int}})$ and the input-referred rms value of the noise as a function of the photocurrent i_{ph} for both constant and varying C_{ph}. Note that the effect of the nonlinearity is only pronounced for large signal values, and results in reduction of both the signal and the noise. The SNR, however, improves as we shall see later. As technology scales or when employing certain high dynamic range schemes [7], the nonlinearity effects on SNR cannot be ignored.

VI. Noise During Readout

During readout, noise is due to transistors M2, M3, M4, and the column and chip level circuits thermal and $1/f$ noise. Ignoring the noise contributions of the column and chip level circuits, which are very small, and the $1/f$ noise, readout noise can be easily computed via the small-signal circuit in Fig. 8. In this figure, $I_{\mathrm{M2}}(t)$, $V_{\mathrm{M3}}(t)$, and $I_{\mathrm{M4}}(t)$ are the thermal noise sources associated with M2, M3, and M4, respectively, g_{m2} and g_{m4} are the transconductances of M2 and M4, g_{d3} is the channel conductance of M3, and C_o is the column storage capacitance including the bitline capacitance. Assuming steady state, which is well justified here, it can be easily shown that the bitline-referred mean square noise voltages due to M2, M3, and M4 are given by

$$\overline{V_{n,\,\mathrm{M2}}^2} = \frac{2}{3}\frac{kT}{C_o}\frac{1}{1+\dfrac{g_{m2}}{g_{d3}}} \tag{22}$$

$$\overline{V_{n,\,\mathrm{M3}}^2} = \frac{kT}{C_o}\frac{1}{g_{d3}\left(\dfrac{1}{g_{d3}}+\dfrac{1}{g_{m2}}\right)} \tag{23}$$

and

$$\overline{V_{n,\,\mathrm{M4}}^2} = \frac{2}{3}\frac{kT}{C_o}g_{m4}\left(\frac{1}{g_{d3}}+\frac{1}{g_{m2}}\right) \tag{24}$$

respectively. These equations show that different noise sources are associated with different noise bandwidth, and thus have different effects on the bitline-referred noise.

To obtain more accurate results for noise during readout (including $1/f$ noise), we use HSPICE. We sweep the IN voltage, perform dc analysis to determine the circuit bias point for each IN voltage value, and then perform ac noise analysis. Using

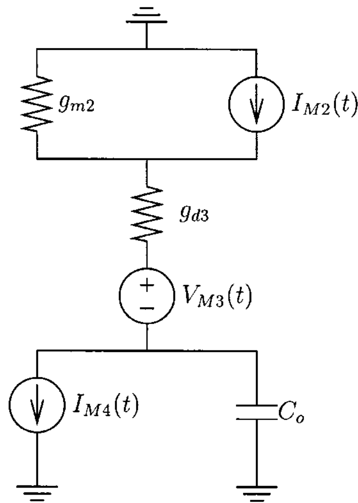

Fig. 8. Small-signal model for noise analysis during readout.

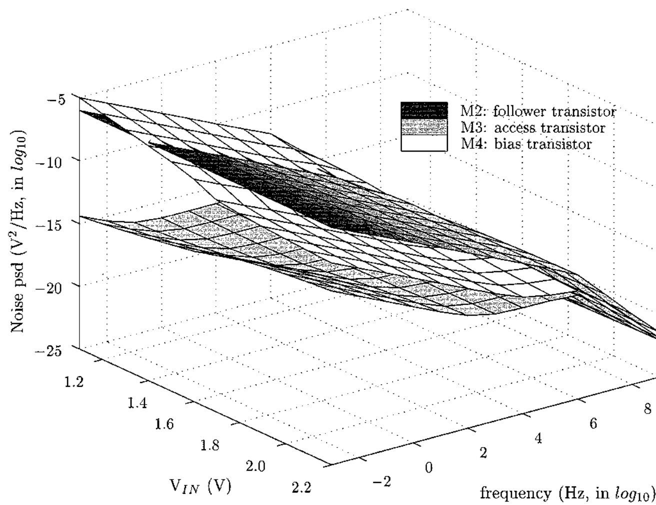

Fig. 9. Readout noise PSD due to M2, M3, and M4.

TABLE I
64×64 APS TEST STRUCTURE CHARACTERISTICS

Technology	0.35 μm, 4-layer metal 1-layer poly, nwell CMOS
Number of Pixels	64×64
Pixel Area	14μm×14μm
Transistors per pixel	3
Fill Factor	29%
Photodetector	nwell/psub diode
Pixel Interconnect	Metal1 and Poly

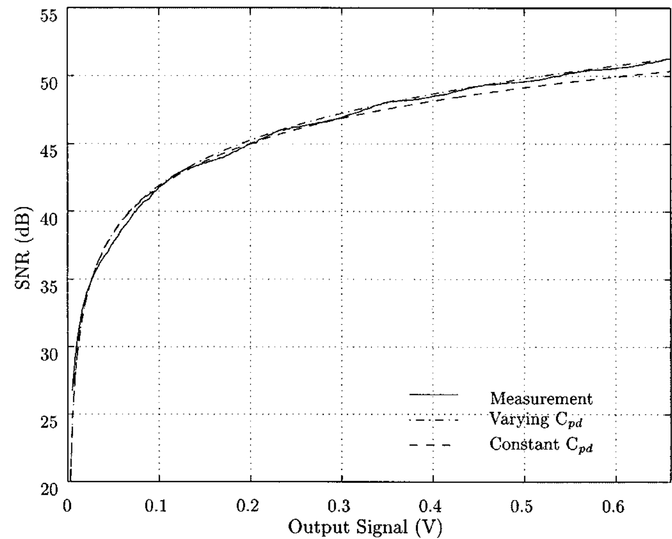

Fig. 10. Simulated versus measured SNR.

this methodology, we simulated our APS circuit including the column and chip level circuits [16]. As expected, the noise contributions from column and chip level circuits were found to be very small. To compare the contributions of M2, M3, and M4 during readout we plot the simulated output-referred PSD for each in Fig. 9. Note that except when the IN voltage is near its reset value, the noise from M3 is several orders of magnitude lower than the noise from M2 and M4. Summing up the contributions from the three transistors to the total output noise, we find that the output-referred rms noise voltage from the readout stage to be around 63 μV, independent of the IN voltage value. Using the simulated IN to OUT voltage gain value of 0.81, this is equivalent to an input-referred value of 78 μV.

VII. Experimental Results

In this section, we present noise measurement results, and compare them to the analysis results presented in the previous sections. The measurements are obtained from our 64×64 pixel APS test structure [16], which were fabricated in a 0.35-μ standard digital CMOS process. A summary of the main sensor characteristics are provided in Table I. The characterization setup is the same as the setup we used to perform QE [17] and FPN [18] measurements. The analog output from our sensor is first amplified using a low noise amplifier (LNA), then digitized using a 16-bit ADC.

To measure noise, special care is taken to reduce environmental interference, which can be caused by light source fluctuations, temperature fluctuations, electromagnetic interference, etc. To do so, we housed the setup in a well air-conditioned dark room. We used a light source with intensity fluctuations of less than 0.5%. Temperature and light intensity were recorded each time data was taken. We repeated the measurements many times so that any remaining environmental interference can be averaged out.

In taking the noise measurements we first determined the board level noise, including the LNA noise and ADC quantization noise. This was done by directly driving OUT with a low-noise dc voltage source. The measured output-referred rms noise voltage was found to be 82 μV, which is comparable to the estimated readout stage noise, but much lower than the reset noise. As a result, reset noise can still be accurately measured.

To measure the reset noise, we reset the pixel and sample the output voltage twice. Each sample can be expressed as the sum of two components, the reset noise and other noise. The reset noise is the same, while the other noise is uncorrelated. By repeating these measurements we estimate both the reset noise power and the other noise power accurately. The rms reset noise voltage was estimated to be 262 μV, while the other noise was estimated to be 113 μV. Using the simulated IN to OUT voltage

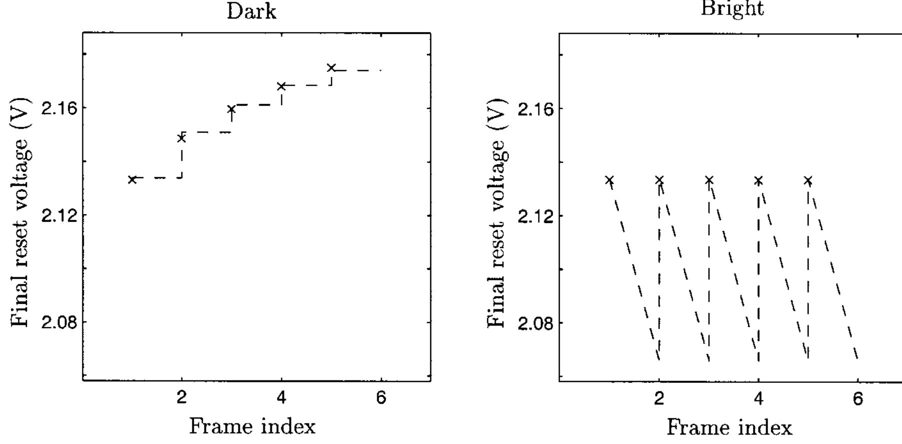

Fig. 11. Measured final reset voltage for five consecutive frames (indicated by $\times$). Dashed lines are the simulated photodiode voltage.

gain of 0.81, we get an estimated input-referred rms reset noise voltage of 323 μV, which is very close to the 303 μV given by $\sqrt{kT/2C_{\mathrm{ph}}}$, and much lower than the $\sqrt{kT/C_{\mathrm{ph}}}$ value of 428 μV. The experiment was repeated at several reset times ranging from 1 to 10 μs and under several low illumination levels. We could not perform the noise measurement at steady-state condition, since the required reset time exceeded the longest reset time of one second allowed by our pattern generator.

We also measured the overall rms noise voltage at different signal levels. In Fig. 10 we plot the measured and the calculated SNR versus the output signal. Two calculated SNR curves are given, one assuming constant photodiode capacitance and the other assuming varying photodiode capacitance as discussed in Section V. Note that the measured SNR curve is very close to the calculated curve assuming varying capacitance, but that the curve assuming constant capacitance becomes slightly lower than the others at high illumination levels.

To illustrate the image lag caused by incomplete reset as described in Section IV, we performed experiments under dark and bright conditions. In Fig. 11 we plot the measured final reset voltage averaged over many trials and the simulated photodiode voltage (as indicated by the dashed lines) for five consecutive frames. The figure confirms that lag occurs following a dark frame. We repeated the bright experiment under several illumination levels and did not observe any image lag. We could not test our pseudo-flash reset method, since in our implementation the drain of the reset transistor was permanently connected to v_{dd}.

VIII. Conclusion

We presented a detailed and rigorous analysis of noise in CMOS photodiode APS. We found that typical reset times are not long enough to achieve steady state. Using time-domain analysis, we found that reset noise is very close to $kT/2C$. This result, we believe, explains the discrepancy between measured reset noise and the commonly quoted kT/C value. We proposed a new pseudo-flash reset method that alleviates image lag due to incomplete reset without increasing reset noise. We analyzed noise due to the photodetector shot noise taking nonlinearity into consideration and found that nonlinearity improves SNR at high illumination. Finally, we presented experimental results obtained from test structures that were fabricated in 0.35-μ CMOS processes, which corroborate the results of our theoretical analysis.

Appendix A
Reset Settling Time

To calculate settling time, we first find the time t_1 at which the reset transistor transitions from above to below threshold. The reset transistor then operates in subthreshold for a period of $t_2 = t_{\mathrm{settle}} - t_1$ until it reaches steady state, i.e., until its drain current almost equals $i_{\mathrm{ph}} + i_{\mathrm{dc}}$.

While the reset transistor is operating above threshold, its drain current is given by

$$i_{\mathrm{d}}(t) = \frac{W}{2L} C_{\mathrm{ox}} \mu_n (v_{dd} - v_{\mathrm{th}}(v_{\mathrm{ph}}) - v_{\mathrm{ph}})^2 \tag{25}$$

where the threshold voltage

$$v_{\mathrm{th}}(v_{\mathrm{ph}}) = v_{\mathrm{th0}} + \gamma \left(\sqrt{v_{\mathrm{ph}} + \phi} - \sqrt{\phi} \right) \mathrm{V}. \tag{26}$$

For most of the reset time, M1 operates in subthreshold, and i_{d} can be expressed as [19]

$$i_{\mathrm{d}}(t) = \frac{W}{L} I_0 \exp\left(\left[\frac{(v_{\mathrm{g}} - v_{\mathrm{ph}})\kappa}{v_T} - \frac{(v_{\mathrm{ph}} - v_{\mathrm{b}})(1-\kappa)}{v_T} \right] \right) \cdot \left(1 - e^{-((v_{\mathrm{d}} - v_{\mathrm{ph}})/v_T)} \right) \tag{27}$$

where v_{g} is the gate voltage, v_{d} is the drain voltage, v_{ph} is the source voltage, v_{b} is the bulk voltage,κ is the gate efficiency factor, $v_T = (kT/q)$, and I_0 is a constant that depends on the transistor threshold voltage.

The transition between above and below threshold occurs when the currents calculated using (25) and (27) are equal. Assuming the test structure circuit parameter values, the voltage at which this transition occurs, i.e., the transition voltage $v_1 \approx 2$ V and t_1 is ≤ 0.2 ns even when the photodiode voltage $v_{\mathrm{ph}}(0)$ is very low.

To find t_2, we first set $v_1 = 2$ V and assume that the capacitance $C_{\mathrm{ph}}(v_{\mathrm{ph}}(t)) = C_{\mathrm{ph}}$, i.e., is independent of t. Defining

$K_0 = (W/L) I_0 e^{(v_g \kappa / v_T)}$ and substituting from (27) into (6) then solving it, we get that

$$v_{\rm ph}(t) = v_T \ln \frac{-K_0 + K_0 e^{(i_c t / v_T C_{\rm ph})} + i_c e^{(v_1/v_T)}}{i_c e^{(i_c t / v_T C_{\rm ph})}} \quad (28)$$

where $i_c = i_{\rm ph} + i_{\rm dc}$, and time is shifted such that $t = 0$ corresponds to the time when the reset transistor enters subthreshold.

Combining (28) and (27) we can explicitly write $i_d(t)$ as a function of time. Now assuming that steady state is achieved for $i_d(t) = 2i_c$, we find that

$$t_2 = \frac{v_T C_{\rm ph}}{i_c} \ln \frac{K_0}{i_c e^{(v_1/v_T)} - K_0}. \quad (29)$$

Thus we get the settling time $t_{\rm settle} = t_1 + t_2$, which is more than 1 ms for typical illumination conditions.

Appendix B
Derivation of Reset Noise Using Time-Domain Analysis

To simplify notation we define $i'_d = i_{\rm ph} + i_{\rm dc}$. The autocorrelation function of the shot noise is thus given by

$$R(t) = \begin{cases} q i_{\rm d}(t) + q i'_d, & t < t_{\rm settle} \\ 2 q i'_{\rm d}, & t \geq t_{\rm settle}. \end{cases}$$

Now define $g' = (q i'_d / kT)$, then for $t \geq t_{\rm settle}$ $g(t) = g'$. Using (9) we get the mean square noise voltage

$$\begin{aligned}
\overline{V_n^2(t_r)} &= \int_0^{t_{\rm settle}} \frac{q i_d(\tau) + q i'_d}{C_{\rm ph}^2} \cdot \exp\left(-2\int_\tau^{t_r} \frac{g(\tau_0)}{C_{\rm ph}} d\tau_0\right) d\tau \\
&\quad + \int_{t_{\rm settle}}^{t_r} \frac{2 q i'_d}{C_{\rm ph}^2} \exp\left(-2\int_\tau^{t_r} \frac{g'}{C_{\rm ph}} d\tau_0\right) d\tau \\
&= \frac{1}{2}\frac{kT}{C_{\rm ph}}\left(1 - \frac{\delta^2}{(t_{\rm settle} - t_1 + \delta)^2}\right) \cdot e^{-2(g'/C_{\rm ph})(t_r - t_{\rm settle})} \\
&\quad + \frac{1}{3}\frac{q i'_d}{C_{\rm ph}^2}\left((t_{\rm settle} - t_1 + \delta) - \frac{\delta^3}{(t_{\rm settle} - t_1 + \delta)^2}\right) \cdot e^{-2(g'/C_{\rm ph})(t_r - t_{\rm settle})} \\
&\quad + \frac{kT}{C_{\rm ph}}\left(1 - e^{-2(g'/C_{\rm ph})(t_r - t_{\rm settle})}\right) \\
&\approx \frac{1}{2}\frac{kT}{C_{\rm ph}} e^{-2(g'/C_{\rm ph})(t_r - t_{\rm settle})} \\
&\quad + \frac{1}{3}\frac{q i'_d t_{\rm settle}}{C_{\rm ph}^2} e^{-2(g'/C_{\rm ph})(t_r - t_{\rm settle})} \\
&\quad + \frac{kT}{C_{\rm ph}}\left(1 - e^{-2(g'/C_{\rm ph})(t_r - t_{\rm settle})}\right). \quad (30)
\end{aligned}$$

The first term of the above equation is derived in the same way we derived (13). It is due to the reset transistor shot noise during the nonsteady-state period. Similarly, the second term is due to the photodiode shot noise during the nonsteady-state period. Using $i'_d = i_d(t_{\rm settle}) \approx (v_T C_{\rm ph}/(t_{\rm settle} + \delta))$ [see (11) in the main text], we get that $(1/3)(q i'_d t_{\rm settle}/C_{\rm ph}^2) \approx (1/3)(kT/C_{\rm ph})$. As expected the second term is smaller than the first, since for $t < t_{\rm settle}$ $i'_d < i_d(t)$. The last term represents the noise generated during $t \geq t_{\rm settle}$.

As $t_r \to \infty$, $e^{-2(g'/C_{\rm ph})(t_r - t_{\rm settle})}$ approaches zero and the first two terms vanish. This confirms that the noise generated before $t_{\rm settle}$ finally decays to zero. The last term on the other hand approaches $kT/C_{\rm ph}$, which is the same as the steady-state result obtained using frequency-domain analysis. We now verify that the above derivation also leads to $(kT/2C_{\rm ph})$ for $t \ll t_{\rm settle}$. It is clear that in this case the third term of (30) does not exist. The second term can be ignored, since $i'_d \ll i_d(t_r)$, $(1/3)(q i'_d t_r / C_{\rm ph}^2) \ll (1/3)(kT/C_{\rm ph})$. This leaves us with the first term which is equal to the right-hand side of (13).

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References

[1] A. J. P. Theuwissen, *Solid-State Imaging with Charge-Coupled Devices*. Norwell, MA: Kluwer, 1995.
[2] G. C. Holst, *CCD Arrays Cameras and Displays*, 2nd ed. New York: JCD Publishing, 1998.
[3] J. Hynecek, "Spectral analysis of reset noise observed in CCD charge-detection circuits," *IEEE Trans. Electron Devices*, vol. 37, pp. 640–647, Mar. 1990.
[4] P. Centen, "CCD on-chip amplifiers: Noise performance versus MOS transistor dimensions," *IEEE Trans. Electron Devices*, vol. 38, pp. 1206–1216, May 1991.
[5] O. Yadid-Pecht, B. Mansoorian, E. Fossum, and B. Pain, "Optimization of noise and responsivity in CMOS active pixel sensors for detection of ultra low light levels," in *Proc. SPIE*, vol. 3019, San Jose, CA, Feb. 1997, pp. 125–136.
[6] S. K. Mendis, S. E. Kemeny, R. C. Gee, B. Pain, C. O. Staller, Q. Kim, and E. R. Fossum, "CMOS active pixel image sensors for highly integrated imaging systems," *IEEE J. Solid State Circuits*, vol. 32, pp. 187–197, Feb. 1997.
[7] S. Decker, D. McGrath, K. Brehmer, and C. G. Sodini, "A 256 x 256 CMOS imaging array with wide dynamic range pixels and column-parallel digital output," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2081–2091, Dec. 1998.
[8] O. Yadid-Pecht, B. Pain, C. Staller, C. Clark, and E. Fossum, "CMOS active pixel sensor star tracker with regional electronic shutter," *IEEE J. Solid-State Circuits*, vol. 32, pp. 285–288, Feb. 1997.
[9] K. Singh, "Noise analysis of a fully integrated CMOS image sensor," in *Proc. SPIE*, vol. 3650, San Jose, CA, Jan. 1999, pp. 44–51.
[10] A. van der Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986.
[11] B. Pain, G. Yang, M. Ortiz, C. Wrigley, B. Hancock, and T. Cunningham, "Analysis and enhancement of low-light-level performance of photodiode-type CMOS active pixel imagers operated with sub-threshold reset," presented at the IEEE Workshop Charge-Coupled Devices and Advanced Image Sensors, Nagano, Japan, June 1999.
[12] H. Tian, B. Fowler, and A. El Gamal, "Analysis of temporal noise in CMOS APS," in *Proc. SPIE*, vol. 3649, San Jose, CA, Jan. 1999, pp. 177–185.

[13] K. K. Thornber, "Theory of noise in charge-transfer devices," *Bell Syst. Tech. J.*, vol. 53, no. 7, pp. 1211–1262, Sept. 1974.

[14] R. Sarpeshkar, T. Delbruck, and C. A. Mead, "White noise in MOS transistors and resistors," *IEEE Circuits Devices Mag.*, vol. 9, pp. 23–29, Nov. 1993.

[15] N. Teranishi, A. Kohono, Y. Ishihara, E. Oda, and K. Arai, "No image lag photodiode structure in the interline CCD image sensor," in *IEDM Tech. Dig.*, 1982, pp. 324–327.

[16] D. Yang, B. Fowler, A. El Gamal, H. Min, M. Beiley, and K. Cham, "Test structures for characterization and comparative analysis of CMOS image sensors," in *Proc. SPIE*, vol. 2950, Berlin, Germany, Oct. 1996, pp. 8–17.

[17] B. Fowler, A. El Gamal, D. Yang, and H. Tian, "A method for estimating quantum efficiency for CMOS image sensors," in *Proc. SPIE*, vol. 3301, San Jose, CA, Jan. 1998, pp. 178–185.

[18] A. El Gamal, B. Fowler, H. Min, and X. Liu, "Modeling and estimation of FPN components in CMOS image sensors," in *Proc. SPIE*, vol. 3301, San Jose, CA, Jan. 1998, pp. 168–177.

[19] C. Mead, *Analog VLSI and Neural Systems*. Reading, MA: Addison Wesley, 1989.

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