Analysis of the Effect of Temperature Variations on Sub-threshold Leakage Current in P3 and P4 SRAM Cells at Deep Sub-micron CMOS Technology

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ABSTRACT
With ever increasing power density and temperature variations within high density VLSI chips, it is very important to study the temperature effects on the devices in a compact way and to predict their scaling. In this paper, the sub-threshold leakage power analysis of the P3 and P4 SRAM cells has been carried out at a temperature range from -25^{0}C to +125^{0}C. It has been observed that the sub-threshold leakage and the standby power dissipation increases with increase in temperature. However, due to the stacked pMOS design used in P4 and P3 SRAM cells, minimum sub-threshold leakage and standby leakage power is observed as compared to the conventional 6T design.

General Terms
SRAM, DSM, VLSI.

Keywords
Temperature Effect, Sub-threshold Leakage, Standby Leakage Power, Conventional 6T SRAM Bit-cell, PP-SRAM, P4-SRAM, P3-SRAM, Stacking.

1. INTRODUCTION
Today's portable devices have become computationally intensive devices as the user interface has migrated to a fully multimedia experience. This migration leads to the growing demand of battery powered portable multimedia applications. So, SRAM plays a critical role in the overall power, performance, stability and area requirements. In order to fulfill the demands, they must be specifically designed for every application. Many devices such as cell phones, have low activity factor, i.e. their idle time is more than active time of device. Even at the idle time, the device battery service is affected by the leakage power loss. Also, with the scaling down of technology, SRAM bit-cell structures are facing serious challenge in maintaining performance because of leakage current issues, both in dynamic and standby modes. According to the International Technology Roadmap (ITRS), 90% of the chip area will be occupied by the memory core by 2014 [1]. Hence, this accumulates a demand for more embedded memory as well as maintaining low-power, stability, performance, speed, standby data retention and less cell area. In standby mode of SRAM bit-cell, there are several sources for leakage current, e.g., the sub-threshold current due to low threshold voltage, etc., while in dynamic mode, the gate leakage current due to very thin gate oxides, is the major contributor [2]. The SRAM leakage current has become a more significant component of total chip current as a large portion of the total chip transistors directly comes from on-die SRAM. Since the activity factor of a large on-die SRAM is relatively low. So, it is demanded to pay more attention towards reducing standby leakage currents. Moreover as most VLSI systems work at elevated temperatures, in this work, the sub-threshold leakage current at various temperatures has been simulated and analyzed in the 6T, PP, P4 and P3 SRAM cells in the standby mode of operation at a temperature ranging from -25^{0}C to 125^{0}C.

The paper is organized as follows. In section 2 a brief functional view of conventional 6T SRAM bit-cell is presented. Basic leakage mechanism due to sub-threshold current and its dependence on temperature is presented in section 3. The section 4 reviews the PP, P4 and P3 SRAM designs followed by the analysis of the four cells and conclusion in section 5 and 6 respectively.

2. CONVENTIONAL 6T SRAM BIT-CELL
The conventional SRAM (CV-SRAM) memory cell, shown here forms the basis for most static random-access memories in CMOS technology. It uses six transistors to store and access one bit. The four transistors in the center form two cross-coupled inverters (N0, N1, P0 and P1). Due to the feedback structure, the two inverters store the logical values 'logic 1' or 'logic 0'. Unlike DRAM it doesn't need to be refreshed as the bit is latched in. It can operate at lower supply voltages and has large noise immunity. However, the six transistors of an SRAM cell take more space than a DRAM cell made of only 1 transistor and 1 capacitor, thereby increasing the complexity of the cell [3].

Two more pass transistors (N2 and N3) are the access transistors controlled by the Word Line (WL), Fig.1.The cell preserves its one of two possible states "0" or "1", as long as power is

available to the bit-cell. Thus the cell draws current from the power supply only during switching and hence the Static power dissipation is very small. But idle mode of the memory is becoming the main problem in the deep–submicron technology due to its concerns in the leakage power and data retention a lower operating voltages. The Bit-cell has three states of operation [4], the Write, Read and Hold states.

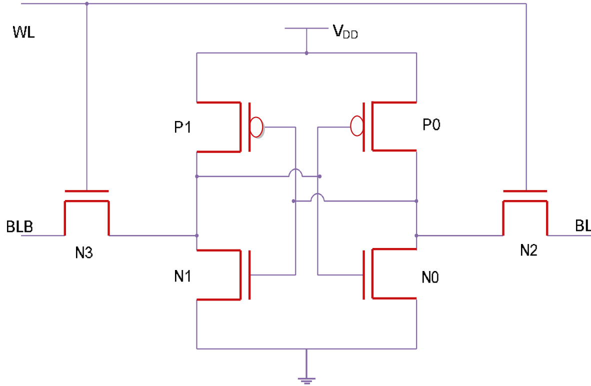

Fig 1: 6T-CMOS SRAM Cell

3. LEAKAGE CURRENT MECHANISMS

High leakage current in deep-submicron regimes is the major contributor of power dissipation of CMOS circuits as the device is being scaled. Various leakage mechanisms are show in Fig. 2, the dominant ones are the gate leakage, sub-threshold leakage, and reverse junction leakage current.

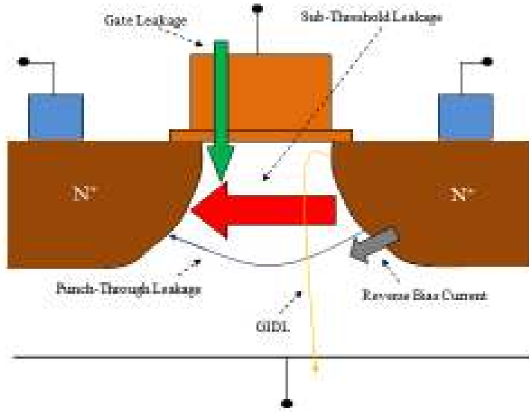

Fig 2: Leakage Current Mechanisms

3.1 Reverse Junction Leakage [5]

Drain and source to well junctions are typically reverse biased, causing p-n junction leakage current. A reverse-bias p-n junction leakage has two main components: one is minority carrier diffusion/drift near the edge of the depletion region; the other is due to electron-hole pair generation in the depletion region of the reverse-biased junction.

3.2 Gate Oxide Leakage [5]

Reduction of gate oxide thickness results in an increase in the field across the oxide. The high electric field coupled with low oxide thickness results in tunnelling of electrons from substrate to gate and also from gate to substrate through the gate oxide, resulting in the gate oxide tunnelling current.

3.3 Gate Induced Drain Leakage (GIDL) [5]

GIDL is due to high field effect in the drain junction of a MOS transistor. When the gate is biased to form an accumulation layer at the silicon surface, the silicon surface under the gate has almost same potential as the p-type substrate. Due to presence of accumulated holes at the surface, the surface behaves like a p region more heavily doped than the substrate. This causes more field crowding and peak field increases, resulting in a dramatic increase of high field effects such as avalanche multiplication and band to band tunneling.

3.4 Punch-through Leakage [5]

In short-channel devices, due to the proximity of the drain and the source, the depletion regions at the drain-substrate and source-substrate junctions extend into the channel. As the channel length is reduced, if the doping is kept constant, the separation between the depletion region boundaries decreases. An increase in the reverse bias across the junctions (with increase in V_{DS}) also pushes the junctions nearer to each other. When the combination of channel length and reverse bias leads to the merging of the depletion regions, punch-through is said to have occurred.

3.5 Sub-Threshold Leakage

The Sub-threshold Leakage Current is the drain-to-source leakage current when the transistor is in the OFF mode. This happens when the applied voltage V_{GS} is less than the threshold voltage V_{th} of the transistor, i.e., weak inversion mode. Subthreshold current flows due to the diffusion current of the minority carriers in the channel of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Equation (1) relates sub-threshold current (weak inversion current) with other device parameters [5].

$$I_{DS} = \frac{\mu_0 W_{eff}}{L_{eff}} C_{ox}.(m-1)V_T^{\,2}.e^{(|V_{GS}|-V_{th})/mV_T}.(1-e^{-|V_{DS}|/V_T}) \qquad \text{Eq. (1)}$$

Where, $$m = 1 + \frac{C'_{dm}}{C_{ox}} = 1 + \frac{\frac{\varepsilon_{si}}{W_{dm}}}{\frac{\varepsilon_{ox}}{t_{ox}}} = 1 + \frac{3t_{ox}}{W_{dm}} \qquad \text{Eq. (2)}$$

'm' is the swing coefficient (also known as the body effect coefficient), μ is mobility, W_{eff} is the channel effective width, W_{dm} is maximum depletion layer width, L_{eff} is the channel effective length, C_{ox} is the gate oxide capacitance, C'_{dm} is capacitance of depletion layer, t_{ox} is the gate oxide thickness, V_T (KT/q) is the thermal voltage, V_{th} is threshold voltage, V_{GS} is the Gate-Source Voltage, V_{DS} is Drain-Source Voltage, K is Boltzmann's Constant, T is Temperature and q is the Charge.

The dependence of subthreshold current on the gate voltage is exponential, Fig. 3 [6]. The inverse of the slope of $\log_{10}(I_{DS})$ versus V_{GS} characteristic is called subthreshold slope (St) [7] and is given as,

$$S_t = \left(\frac{d(\log_{10} I_{DS})}{dV_{GS}} \right)^{-1} \quad \text{Eq. (3)}$$

Subthreshold slope indicates how effectively the transistor can be turned off when V_{GS} is decreased below V_{th}.

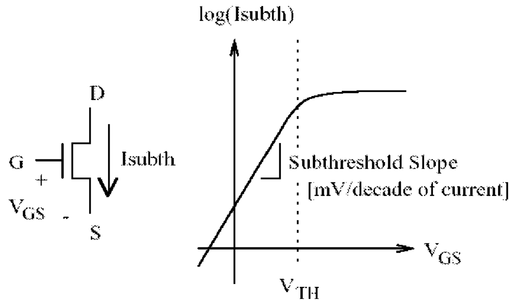

Fig 3: Sub-threshold Leakage in a NMOS transistor.

Effect of Temperature

Temperature dependence of the subthreshold leakage current is important as digital very large scale integrated (VLSI) circuits usually operate at elevated temperatures due to the power dissipation. The variation of the sub-threshold slope with the temperature is shown in Fig 4 as derived from the sub-threshold model in [7].

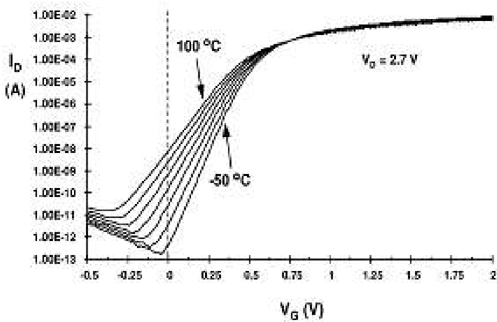

Fig 4: I_D Vs V_G showing temperature sensitivity of I_{OFF} [8].

As the major contributor of this off current is the sub-threshold current [5], the temperature dependence of I_{OFF} represents the temperature variation of the subthreshold current. Two parameters increase the subthreshold leakage as the temperature is increased. Firstly, the subthreshold slope (S_t) increases linearly with temperature and the moreover the threshold voltage (V_{th}) decreases.

4. REVIEW OF RELATED WORK

In this section, we have reviewed some of the previously reported SRAM cell structures, e.g., 6T, PP, P3, and P4 cells.

In [9], a gate leakage current reduction technique based on the pMOS pass-transistor SRAM bit-cell structure as PP-SRAM cell has been proposed at 45nm CMOS technology at V_{DD}=0.8V. In this cell, in order to decrease the gate leakage currents of the SRAM bit cell, nMOS access transistors are replaced by pMOS access transistors. The use of pMOS leads to performance degradation due to different mobility coefficients for the nMOS and pMOS transistors and more dynamic power consumption. To overcome this problem, the width of pMOS pass transistor is selected as 1.8 times of that of the nMOS for technology used in this work. Thus, the design has a significant reduction in the gate leakage, as the barrier height of the holes is more than that of the electrons, i.e., 4.5eV and 3.1eV, respectively, with no access time degradation, and with an area penalty, fig 5.

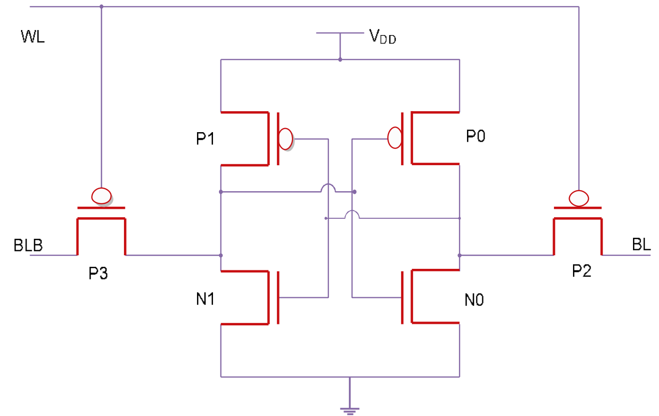

Fig 5: PP-SRAM Bit-Cell

In [10], a P4 SRAM bit-cell structure at 45nm technology has been presented, fig 6. The gate leakage current will be lower in the off state of the pMOS transistors due to stacking effect. The two gated–ground pMOS transistors oppose the flow of leakage current through them by raising the ground level, virtual ground at node V_M. The design presents a significant reduction in the active and standby power, both in the read/write and idle mode. The subthreshold and gate leakage currents have been reduced at the cost of the data retentation and area efficiency.

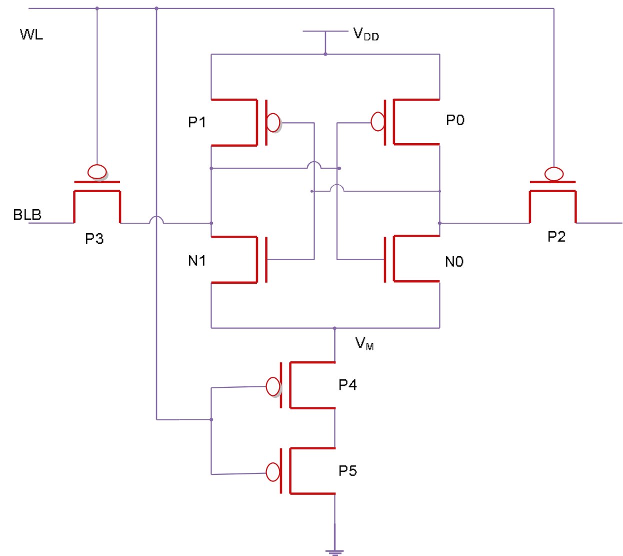

Fig 6: P4-SRAM Bit-Cell

In [11], a P3 SRAM bit-cell structure at 45nm technology has been reported for semiconductor memories with high activity

factor based applications in Deep Sub-Micron (DSM) CMOS technology, fig 7. It has been designed for the reduction of the active and the standby leakage power through the gate and subthreshold leakage reduction in the active and standby mode of the memory operation by adding one pMOS transistor as stacking transistor. The pMOS transistors are used to lower the gate leakage current [9] while full-supply body-biasing and pMOS stacking reduces the sub-threshold leakage current. It made a significant fall in dynamic as well as standby powers in comparison to the conventional 6T SRAM bit-cell, at the cost of small area penalty and reduced Noise Margin.

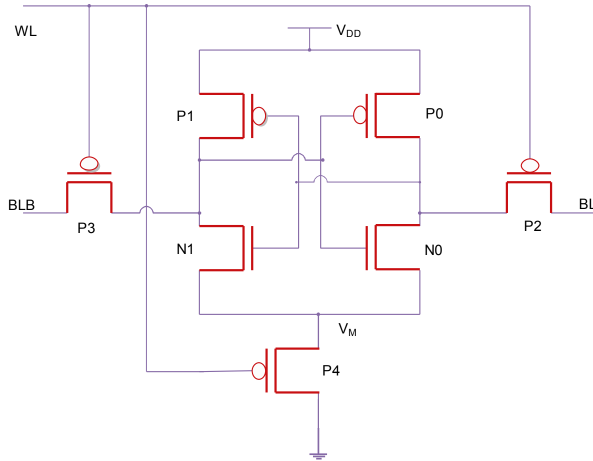

Fig 7: P3-SRAM Bit-Cell

5. TEMPERATURE AND LEAKAGE CURRENT ANALYSIS

To analyze the temperature dependence of subthreshold leakage current and standby leakage power in the Conventional 6T, PP, P4, and P3 SRAM Cells, the simulation has been performed at 45nm CMOS technology with an oxide thickness of 2.4nm at temperature ranging from -25^{0}C to 125^{0}C and the supply voltage of V_{DD}=0.8V and 0.7V.

5.1 Sub-Threshold Leakage (I_{SUB})

Fig 8 and 9 shows the variation of the total sub-threshold leakage in various SRAM bit-cells at temperature ranging from -25^{0}C to 125^{0}C with V_{DD} = 0.8V and V_{DD} = 0.7V, respectively.

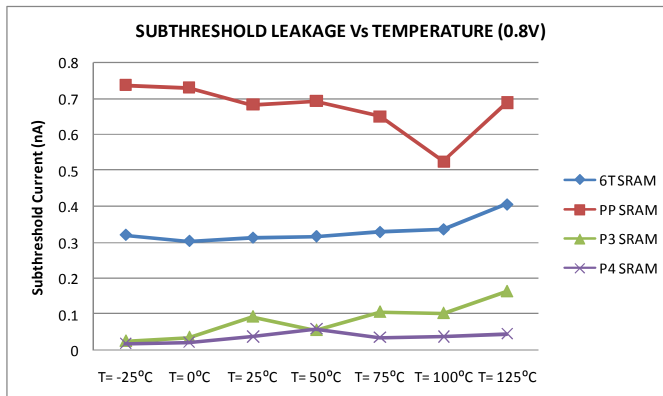

Fig 8: Temperature Vs Sub-threshold Leakage at 0.8V in SRAM cells.

As known in the literature, the sub-threshold current strongly depends upon the temperature, the net sub-threshold leakage increases with the increase in the temperature (fig 8 and fig 9), reaching maximum at T=125^{0}C.

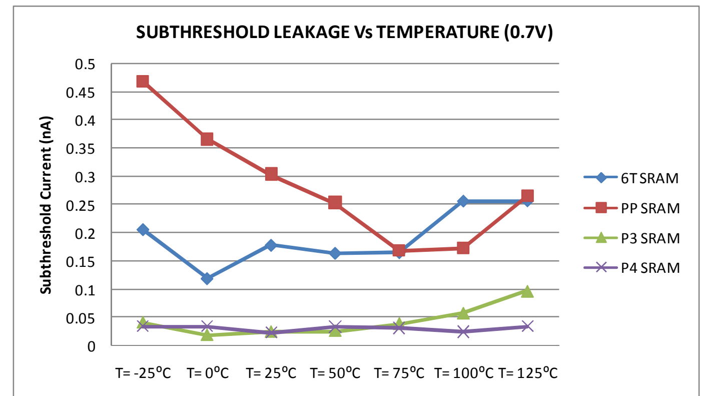

Fig 9: Temperature Vs Sub-threshold Leakage at 0.7V in SRAM cells.

The least subthreshold leakage is observed in the P4 SRAM cell due to the stacking of the two pMOS transistors.

At V_{DD}=0.7V, it has been observed 71%, 87%, 80% and 87% less as compared to the conventional 6T SRAM at 0°C, 25°C, 50°C and 125°C respectively. Moreover, in the P3 cell 84%, 86%, 84% and 62% drop in the leakage current has been recorded at 0°C, 25°C, 50°C and 125°C respectively compared to the 6T cell.

At V_{DD}=0.8V, it has been observed 93%, 88%, 81% and 89% less as compared to the conventional 6T SRAM at 0°C, 25°C, 50°C and 125°C respectively. In the P3 cell 88%, 70%, 82% and 60% drop in the leakage current has been recorded at 0°C, 25°C, 50°C and 125°C respectively compared to the 6T cell.

5.2 Standby Power

Due to the variation of sub-threshold current with temperature, the total standby power also strongly depends upon temperature, increasing exponentially at very high temperatures as seen from Fig 10 and 11.

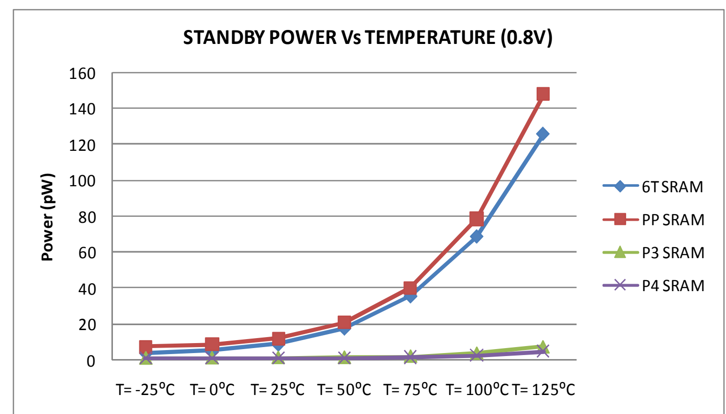

Fig 10: Temperature Vs Standby Power at 0.8V.

Again, as in the case of sub-threshold current, the P4 and the P3 SRAM cells provide the least power dissipation in the standby mode, while the PP SRAM cell has maximum leakage.

In the P4 cell there is a leakage power reduction of about 80%, 87%, 94% and 96% at 0°C, 25°C, 50°C and 125°C respectively w.r.t conventional 6T cell. While in case of P3 cell 77%, 85%, 92% and 93% drops have been observed at 0°C, 25°C, 50°C and 125°C in comparison to the 6T cell design.

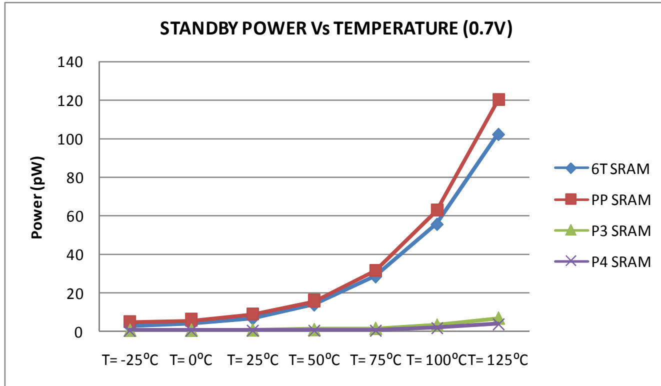

Fig 11: Temperature Vs Standby Power at 0.7V.

6. CONCLUTION

In this paper we have analyzed the effect of temperature variations on the sub-threshold leakage and the total standby leakage power in various SRAM bit-cell structures. It has been observed that there is an increase in the sub-threshold leakage with the temperature rise, due to the increase in the sub-threshold slope (S_t) and the decrease in the threshold voltage (V_{th}) of the transistors with temperature rise. A drop of upto 87% and 60% (w.r.t 6T SRAM cell) has been observed in the P4 and P3 SRAM cells, respectively, even at a high temperature 125°C. Also, due to this increase in the sub-threshold current, there is also an increase in the total standby leakage power consumption. The standby leakage power has also been reduced by almost 96% and 93% in the P4 and P3 SRAM cells, respectively at 125°C. So, besides the cell stability issue and area penalty, the P4 and P3 bit-cells offers significantly less variation in the subthreshold leakage power and the overall standby leakage power due to the pMOS stacking at the deep submicron technology, 45nm.

7. ACKNOWLEDGMENTS

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