Analysis of Threshold Voltage and Drain Induced Barrier Lowering in Junctionless Double Gate MOSFET Using High-κ Gate Oxide

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Abstract—**The change of threshold voltage and Drain Induction Barrier Lowering (DIBL) is observed when high dielectric constant material is used as gate oxide of the junctionless double gate (JLDG) MOSFET. For this purpose, an analytical threshold voltage model is proposed using the first term of the series-type potential model derived from the Poisson equation. The results of the model presented in this paper are in good agreement with threshold voltages derived from TCAD. Using this model, the threshold voltage and DIBL were observed for the channel length, the silicon thickness, and the gate oxide thickness with the dielectric constant as a parameter. As a result, when a high-κ material was used as a gate oxide, the threshold voltage increased but the rate of change with respect to channel size and oxide thickness decreased. The DIBL is inversely proportional to the dielectric constant, and the DIBL was as small as 20 mV/V even at a channel length of 15 nm when the dielectric constant was 30. In the case of using HfO_2/ZrO_2 (κ=25), the rate of change of threshold voltage for oxide thickness was about 1/5 smaller than SiO_2 (κ=3.9). The rate of change of DIBL for oxide thickness in the case of La_2O_3 was about 1/4 smaller than SiO_2 (κ=3.9). The use of the high-κ oxide film may increase the design margin for the oxide thickness variation.**

Index Terms—**Dielectric constant, double gate, junctionless, threshold voltage**

I. Introduction

In the past decade, the transistor size has entered the age of nanotechnology. As the minimum line width of transistors is reduced to nano units, short channel effects and gate parasitic currents have emerged as important factors that hinder transistor performance. In order to solve these problems, a multi-gate structure, various types of channel structures, various types of gate structures, and the like have been proposed [1]-[3]. In particular, as the channel length is reduced in nano units, there are difficulties in the process of changing the doping concentration and the doping pattern between the source and channel, and the drain and channel. The device developed to solve this problem is a junctionless gate structure. The junctionless transistor operates only as an accumulation mode without the inversion that occur in the channel region of the conventional CMOSFET. Not only does it has the advantage of facilitating the process, but it also reduces the gate parasitic current [4], [5]. However it was found that the parasitic current through gate oxide increased due to the reduction of gate oxide thickness even though the junctionless structure. A parasitic current exceeding 1 A/cm^2 at 1 V flows into the gate in the case of a SiO_2 layer. This is known to increase even more if the channel length decreases to 10 nm, and then the on-off current ratio decreases due to the increase of parasitic current [6], [7]. The off-current and applied voltage should be kept as low as possible in order to improve the performance of transistors, such as especially high-speed operation, high drive current, and low power consumption [8]. In order to solve this problem, efforts have been made to reduce the gate parasitic current by using a material that has a high dielectric constant (κ) as the gate oxide film [9]-[12]. In addition, a high-κ gate oxide film can be used to continuously reduce the transistor size while reducing the short channel effect. Furthermore, in the case of SiO_2 with a thickness of 1.5 nm or less, the parasitic current passing directly through the gate oxide film at the gate voltage over 1 V is increased to gate limit, which then greatly affects transistor performance [13]. Priya *et al*. analyzed the subthreshold voltage characteristics when SiO_2, Al_2O_3, Y_2O_3, HfO_2/ZrO_2, La_2O_3, TiO_2, etc. were used as gate oxide films for the junctionless transistor transistors, and Sakshi et al. analyzed the threshold voltages of CMOSFETs when SiO_2, Al_2O_3, HfO_2, and Ta_2O_5 were used as gate oxide films [14], [15]. Xie *et al*. also proposed a potential model using scale length to analyze short channel effects on junctionless double gate (JLDG) MOSFETs but analyzed only the threshold voltage shift [16]. Nirmal *et al*. also suggested that the on-off current ratio is improved in the case of high-κ gate oxide by analyzing the on-off current when various gate oxides are used in the double-gate MOSFET [17]. Singh *et al*. also announced recently for design and analysis of high-κ silicon nanotube tunnel FET [18]. As such, efforts are being made to improve the performance of transistors by using high-κ gate oxide films. In this paper, we use the Xie's potential model to analyze the threshold voltage and drain induced barrier lowering (DIBL) for the transistor

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size when the gate oxides are SiO_2, Al_2O_3, Y_2O_3, HfO_2/ZrO_2, La_2O_3, and TiO_2, respectively. For this purpose, we propose an analytical threshold voltage model using the Xie's potential model.

II. Analytical Threshold Voltage and DIBL Model for JLDG MOSFET

A. Analytical Threshold Voltage Model

Colinge *et al.* presented the fabrication of junctionless transistor [19], and recently Kaharudin *et al*. introduced the process of junctionless double gate vertical MOSFETs [20]. The schematic JLDG MOSFET of Fig. 1 is used to analyze the threshold voltage and DIBL in this paper. The source and drain were heavily doped with *n*+ and the channel was doped with $N_d=10^{19}/cm^3$. The gate is made of metal with a work function of ϕ_m= 4.68 eV. The ε_{ox} is the permittivity of the oxide film and SiO_2, Al_2O_3, Y_2O_3, HfO_2/ZrO_2, La_2O_3, TiO_2 with dielectric constants κ of 3.9, 9, 15, 25, 30, 80, respectively, are used as the gate oxide. In the case of a material having a high dielectric constant, the effective oxide thickness (EOT) is expressed as:

$$\mathrm{EOT}=\frac{\kappa_{\mathrm{SiO_2}}}{\kappa_{\text{high-}\kappa}}t_{\text{high-}\kappa} \tag{1}$$

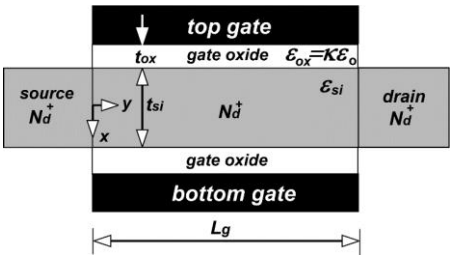


Fig. 1. Schematic cross-sectional diagram of the junctionless double gate (JLDG) MOSFET.

It can be demonstrated that gate leakage current is effectively prevented with the same effect as using a very thin SiO_2. As can be seen from (1), in the case of HfO_2/ZrO_2, when the EOT is 1 nm, the same effect may be obtained as in the case of using SiO_2 of about 3.8 nm thickness may be obtained. The ε_{si} is the permittivity of silicon, L_g is the gate length, t_{si} is the silicon thickness, and t_{ox} is the oxide film thickness. The potential distribution induced by Xie *et al*. can be expressed in the following series form [16].

$$\phi(x,y)=-\frac{qN_d x^2}{2\varepsilon_{si}}+V_{gs}-\Delta\phi+\frac{qN_d t_{si}^2}{8\varepsilon_{si}}\left(1+\frac{4\varepsilon_{si}t_{ox}}{t_{si}\varepsilon_{ox}}\right)+\sum_{n=1}^{\infty}\frac{b_n\sinh\left[\frac{\pi(L_g-y)}{\lambda_n}\right]+c_n\sinh\left[\frac{\pi y}{\lambda_n}\right]}{\sinh\left[\frac{\pi L_g}{\lambda_n}\right]}\times\cos(\pi x/\lambda_n) \tag{2}$$

Here, the E_g is the energy bandgap of silicon; V_{ds} the drain voltage; V_{gs} the gate voltage; $\Delta\phi$ the difference between the work function of the gate metal and the channel; ϕ_0 the center potential at x=y=0. As shown in (2), these variables directly affect the potential distribution. As can be seen from (2), the ε_{ox} has a direct influence on the potential distribution. In addition, the eigenvalue λ_n decreases rapidly as n increases, so that $\sinh(\pi L_g/\lambda_n)$, the denominator value for the last term on the right side of (2), increases rapidly according to n [21]. As a result, the last term on the right side of (2) is expressed using only n = 1 in this paper. In general, such an approximation is known to be valid when $L_g > 1.5\lambda_1$ [3], [15]. Therefore, in this paper, an analytical model of the threshold voltage is derived using the case of n = 1 in (2). In order to use the ϕ_{min} method [22] to find the threshold voltage, the minimum value of $\phi(x, y)$ is found at the conduction center in (2). In other words, if $y = y_{min}$ satisfying $\partial\phi\ (x, y)\ /\partial y = 0$ is obtained and substituted into (2), the value of y_{min} can be obtained as the following equation [21].

$$y_{\min}=\left(\frac{\lambda_1}{\pi}\right)\cosh^{-1}\times\sqrt{\frac{b_1^2}{b_1^2-\left[b_1\coth(\pi L_g/\lambda_1)-c_1\,\mathrm{csch}(\pi L_g/\lambda_1)\right]^2}} \tag{3}$$

By substituting the y_{min} into (2), the minimum potential can be calculated as

$$\phi_{\min}=V_{gs}-\Delta\phi+\frac{qN_d t_{si}^2}{8\varepsilon_{si}}\left(1+\frac{4\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\right)+\frac{b_1\sinh\left[\pi\frac{L_g-y_{\min}}{\lambda_1}\right]+c_1\sinh\left(\pi\frac{y_{\min}}{\lambda_1}\right)}{\sinh\left(\pi\frac{L_g}{\lambda_1}\right)} \tag{4}$$

In the case of JLDG MOSFET in (2), most electrons are transmitted along the central axis, so x = 0 is substituted.

At this time, if V_{gs} satisfying Φ_{min} = 0 is set as the threshold voltage V_{th}, an analytic model of the threshold voltage V_{th} can be obtained as follows:

$$V_{th}=\Delta\phi-\frac{qN_d t_{si}^2}{8\varepsilon_{si}}\left(1+\frac{4\varepsilon_{si}t_{ox}}{\varepsilon_{ox}t_{si}}\right)-\frac{b_1\sinh\left[\pi\frac{L_g-y_{\min}}{\lambda_1}\right]+c_1\sinh\left(\pi\frac{y_{\min}}{\lambda_1}\right)}{\sinh\left(\pi\frac{L_g}{\lambda_1}\right)} \tag{5}$$

B. DIBL and Current-Voltage Relation

In this paper, we will observe the change of the threshold voltage according to the dielectric constant using (5). In addition, the DIBL indicating the change of

the threshold voltage according to the change of the drain voltage can be expressed by

$$\mathrm{DIBL} = V_{\mathrm{th}}(V_{\mathrm{ds}} = 0.1\ V) - V_{\mathrm{th}}(V_{\mathrm{ds}} = 1.1\ V) \qquad (6)$$

To illustrate how the DIBL changes with the dielectric constant, the potential energy distributions are plotted against drain voltage under the conditions given in Fig. 2, with dielectric constants as parameters. As shown in Fig. 2, the potential energy increases as the dielectric constant increases. In addition, it can be seen that the source side potential energy decreases more due to the increase of the drain voltage when the dielectric constant decreases. It can also be seen that as the dielectric constant decreases, the DIBL increases. This phenomenon will be quantitatively analyzed using (6).

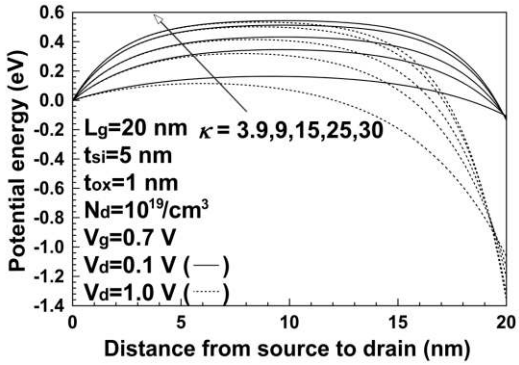


Fig. 2. Potential energy distributions for drain voltages with dielectric constants as parameters.

Fig. 3 shows the result obtained by using the following (7) to observe the relationship between the drain current and the gate voltage in the subthreshold region according to the change of the dielectric constant.

$$I_d = \frac{qn_i\mu_n WkT\left\{1-\exp\left(\frac{-qV_{\mathrm{ds}}}{kT}\right)\right\}}{\int_0^{L_g}\frac{1}{\int_{-t_{\mathrm{si}}/2}^{t_{\mathrm{si}}/2}\exp\left(\frac{-q\phi(x,y)}{kT}\right)dy}dx} \qquad (7)$$

As shown in Fig. 3, it can be seen that as the dielectric constant increases, the subthreshold current decreases significantly. It can also be observed that the subthreshold swing value decreases with increasing dielectric constant [23]. As the threshold voltage is the gate voltage when the drain current is approximately 10^{-7} A, as shown in Fig. 3, it can be seen that the threshold voltage increases with increasing dielectric constant [7]. Increasing the threshold voltage is the disadvantage that appears as an increase in dynamic power consumption due to an increase in the supply voltage, but this can be sufficiently offset by the decrease of static power consumption due to the reduction of the subthreshold drain current in the region below the threshold voltage as shown in Fig. 3 [24]. That is, the increase in the threshold voltage is about 10^{-1} order but the decrease in the drain current is 10^{-6} order at V_{gs}=0.7 V and V_{ds}=0.1 V when the dielectric constants are changed from 3.9 to 80, so the static power consumption may be sufficiently reduced in the high-κ oxide film due to low gate leakage current and low drain current in subthreshold region.

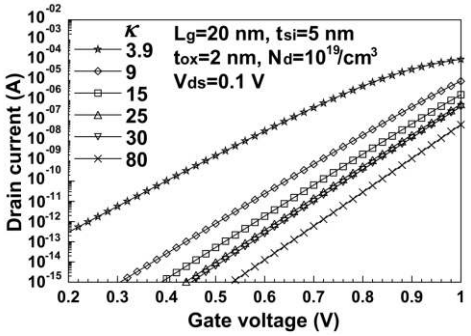


Fig. 3. Drain current vs. gate voltage for dielectric constants.

TABLE I: THE PARAMETERS USED IN THIS PAPER

Parameters	Ranges
Channel length	≤ 50 nm
Silicon thickness	≤ 10 nm
Oxide thickness	≤ 3 nm
Dielectric constant	≤ 80
Doping concentration	10^{19}/cm^3

III. THRESHOLD VOLTAGE AND DIBL FOR THE DIELECTRIC CONSTANT IN JLDG MOSFET

A. Threshold Voltage for the Dielectric Constant

The validity of (5) has been demonstrated by showing good agreement with the TCAD results in the paper already published [21]. Therefore, we use (5) to analyze the threshold voltage and DIBL in the range of the parameters of Table I.

Since the scale length decreases as the dielectric constant increases, the channel length that satisfies the condition of $L_g > 1.5\lambda_1$ decreases further as the dielectric constant increases. This means the approximation using $n = 1$ is valid for the channel length range calculated in this paper. However, since SiO_2 does not satisfy the condition of $L_g > 1.5\lambda_1$ when the oxide thickness is more than 3 nm, this paper is limited to the case where the oxide thickness is less than 3 nm [23].

First, in order to observe the threshold voltage shift phenomenon, the threshold voltage shift obtained by using the dielectric constant as a parameter is shown in Fig. 4. It can be seen in Fig. 4 that the larger the dielectric constant, the lower the threshold voltage shift phenomenon. In (5), the terms related to the oxide dielectric constant are the second and third terms. As can be seen from the second term of (5), increasing the dielectric constant will decrease the value of the second term and increase the threshold voltage. In the case of the third term, it varies not only with the dielectric constant but also with the channel length as shown in the inset of Fig. 4. In the inset of Fig. 4, if the channel length is increased, the third term of (5) does not affect the threshold voltage because it is close to 0, but if the channel length is small, it will act as a factor to decrease the threshold voltage. In particular, when the dielectric constant is small, it can be observed that the variability according to the channel length increases. This affects the threshold voltage shift, so that the smaller the

dielectric constant, the worse the threshold voltage shift phenomenon. As shown in Fig. 4, when the maximum threshold voltage shift is 0.1 V, the channel length decreases to about 25 nm for the oxide film of SiO_2 (κ = 3.9), but the channel length may be reduced to 15 nm for HfO_2/ZrO_2 (κ = 25) with the same threshold voltage shift. In other words, as the dielectric constant increases, short channel effects such as threshold voltage shift may be reduced.

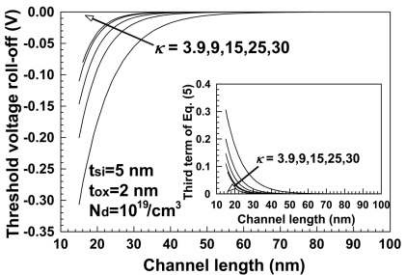


Fig. 4. Threshold voltage shifts for channel length with dielectric constants as parameters.

The threshold voltage is greatly influenced not only by the channel length but also by the thickness of the silicon and the thickness of the oxide film. Fig. 5 shows the threshold voltages with the dielectric constant as a parameter, according to the silicon thickness and oxide film thickness. As shown in Fig. 3, when the dielectric constant increases, the threshold voltage increases [25], [26]. It can be observed that the change of the threshold voltage according to the thickness of the oxide film is larger than the change of the threshold voltage due to the change of silicon thickness when the gate oxide is SiO_2. However, it was observed that when the dielectric constant increases, the change of the threshold voltage according to the change of silicon thickness is almost constant, but the change of the threshold voltage according to the change of the oxide thickness is greatly reduced. Especially for TiO_2 with a dielectric constant of 80, when the thickness of the oxide film changes from 1 nm to 3 nm, the threshold voltage shows a change of about 50 mV, but for SiO_2 with a dielectric constant of 3.9, a large change of about 350 mV occurs. It was observed that the threshold voltage saturates as the dielectric constant increases, as shown in Fig. 5.

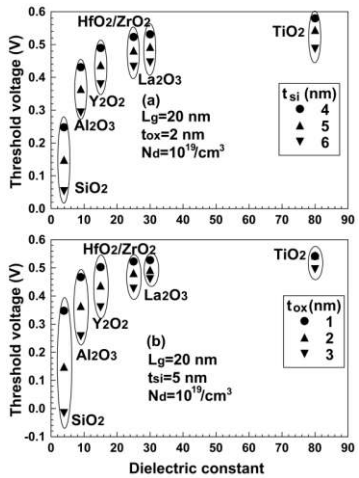


Fig. 5. Threshold voltages for dielectric constants with (a) the silicon thickness and (b) the oxide thickness as parameters.

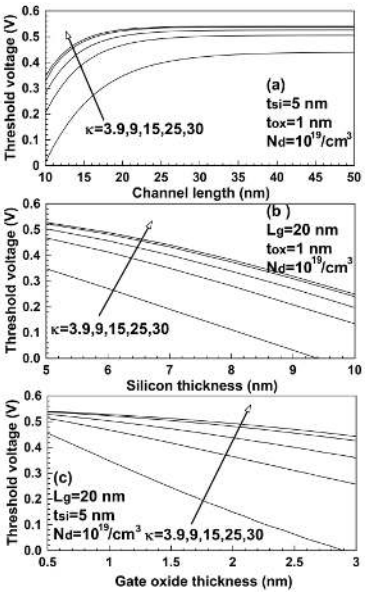


Fig. 6. Threshold voltage for (a) the channel length, (b) silicon thickness, and (c) gate oxide thickness with dielectric constants as parameters.

The variation of the threshold voltage according to the channel size and oxide thickness is shown in Fig. 6 with the dielectric constant as a parameter. As described above, it can be seen that as the dielectric constant increases, the threshold voltage increases. As shown in Fig. 6 (a), as the dielectric constant increases, the channel length at which the threshold voltage shift starts appearing decreases greatly, and the magnitude of the threshold voltage shift also decreases. As shown in Fig. 6 (b), the threshold voltage is very sensitive to the variation of silicon thickness. Unlike conventional CMOSFETs, in the case of JLDG MOSFETs, the silicon bulk used as the channel acts as the conduction path. In particular, when the dielectric constant is small, the change of the threshold voltage with respect to the silicon thickness is more significant. That is, in the case of SiO_2 (κ = 3.9) the change of threshold voltage decreased by $\Delta V_{th}/\Delta t_{si}$ = −79.4 mV/nm, while for HfO_2/ZrO_2 (κ = 25) it decreased by $\Delta V_{th}/\Delta t_{si}$ = −56 mV/nm. The change in the threshold voltage for the change of silicon thickness may reduce when the dielectric constant increases. As observed in Fig. 6 (c), it can be seen that as the gate oxide thickness increases, the threshold voltage decreases. The rate of the decrease was very large when the dielectric constant was small, and as the dielectric constant increased, the change in threshold voltage was greatly decreased. In other words, SiO_2 (κ = 3.9) decreased by $\Delta V_{th}/\Delta t_{ox}$ = −190 mV/nm, while for HfO_2/ZrO_2 (κ = 25) it decreased by $\Delta V_{th}/\Delta t_{ox}$ = −38 mV/nm. Therefore, in the case of SiO_2, the threshold voltage is greatly changed according to the thickness of the oxide film, and it is necessary to pay attention to the design. On the other hand, if the dielectric constant is large, the change of threshold voltage according to the channel size and the thickness of the oxide is small, which affords more the tolerance in transistor design.

B. DIBL for Dielectric Constant

The DIBL calculated using (6) is shown in Fig. 7 for the change of dielectric constant. The gate oxide thickness,

which is most sensitive to the change of threshold voltage, was used as a parameter. In general, the DIBL is expressed as σ_D [27]:

$$\sigma_D \propto \frac{1}{C_{ox}} = \frac{t_{ox}}{\varepsilon_{ox}} \quad (8)$$

In other words, since C_{ox} is proportional to the dielectric constant, the DIBL will be inversely proportional to the dielectric constant. We can see this in Fig. 7. That is, as the dielectric constant increases, the DIBL decreases in inverse proportion to the dielectric constant. As mentioned in Fig. 2, the DIBL decreases as the dielectric constant increases. This is because the source-side potential energy change due to the increase of the drain voltage is almost negligible at high dielectric constant. In the case of SiO_2 (κ = 3.9), it is found that the DIBL also changes greatly with changes in the thickness of the oxide film. As the dielectric constant increases, the change of the DIBL with the change of the oxide film thickness gradually decreases. This is because the DIBL is proportional to the oxide film thickness, but the rate of change decreases as the denominator of (8) increases. In particular, in the case of TiO_2 (κ = 80), the DIBL was very good as 20 mV/V or less regardless of the thickness of the oxide film calculated. In the case of SiO_2 (κ = 3.9), note that this value can be obtained only by fabricating an oxide film which has a thickness of 0.5 nm, and this is difficult to implement.

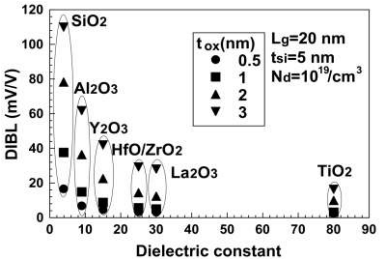


Fig. 7. DIBLs for dielectric constants with gate oxide thicknesses as parameters.

The variation of DIBL according to channel size and oxide film thickness is shown in Fig. 8 using the dielectric constant as a parameter. In Fig. 8 (a), it can be seen that as the dielectric constant increases, the rate of change of DIBL decreases with channel length. If the dielectric constant is increased to 30, the DIBL decreases below 20 mV/V when the channel length is more than 15 nm. It can be seen from Fig. 8 (a) that this DIBL can be obtained when the channel length is more than 25 nm for SiO_2 as gate oxide. In particular, even when the channel length decreases to 10 nm for the dielectric constant of 25 or more, a very good DIBL of 80 mV/V is observed. It can also be observed that the DIBL values are saturated as the dielectric constant increases. This phenomenon can also be observed in Fig. 6 (a). Observing the change of DIBL on silicon thickness, it is shown that the rate of change of DIBL on silicon thickness decreases as the dielectric constant increases. It can be seen that the sensitivity of the DIBL to silicon thickness $\Delta\sigma_D/\Delta t_{si}$ is 14.8 mV/V-nm in case of SiO_2 (κ = 3.9), but it decreases to 10.1 mV/V-nm in La_2O_3 (κ = 30). It can be also observed that the oxide rate of change of DIBL with respect to the variation of the thickness also decreases as the dielectric constant increases. That is, in case of SiO_2, the sensitivity of DIBL to oxide thickness $\Delta\sigma_D/\Delta t_{ox}$ is 38.0 mV/V-nm but it decreases to 9.1 mV/V-nm in La_2O_3 with a dielectric constant of 30. Observing the change of DIBL with the change of dielectric constant, it can be seen that the change of oxide thickness has more influence on DIBL than the change of silicon thickness at small dielectric constant.

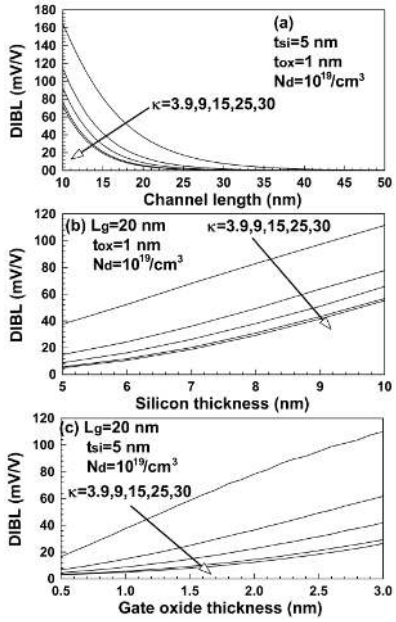


Fig. 8. DIBLs for (a) the channel length, (b) the silicon thickness, and (c) gate oxide thickness with dielectric constants as parameters.

IV. Conclusion

In this paper, in order to investigate the short channel effect that occurs during the scaling of the JLDG MOSFET, the change of threshold voltage and DIBL is observed when a material having a higher-κ than SiO_2 is used. For this purpose, an analytical threshold voltage model was proposed using the potential distribution obtained using the Poisson equation. The analytic threshold voltage model presented in this paper is in good agreement with the results of two dimensional numerical simulations. Using this model, the variation of the threshold voltage for the channel length, silicon thickness, and gate oxide thickness in the JLDG MOSFET was observed using the dielectric constant as a parameter. As a result, as the dielectric constant increased, the threshold voltage increased, but the on-off current decreased significantly, resulting in a significant decrease in static power consumption. In particular, when the gate oxide thickness was increased, the threshold voltage and DIBL changed more significantly according to the dielectric constant. In addition, when the dielectric constant is large, the change of the threshold voltage and the DIBL with respect to the change of the oxide thickness is greatly reduced. That is, when a material with a dielectric constant of 30 or more was used as the gate oxide film, the threshold voltage and the DIBL value was hardly affected by the channel size and the oxide film thickness change. However, in the case of a material having a high

dielectric constant, a problem is exposed such as a defect occurring at an interface with silicon, and thus the techniques related to direct deposition and annealing of high-κ materials for forming an excellent interface should be developed further.

CONFLICT OF INTEREST

The author declares no conflict of interest.

REFERENCES

[1] C. Nistor. (June 2017). Samsung begins mass production of the Exynos I T200 chip for IoT use. [Online]. Available: https://www.notebookcheck.net/Samsung-begins-mass-production-of-the-Exynos-i-T200-chip-for-IoT-use.229970.0.htmlL

[2] D. Schor. (July 2018). VLSI 2018: Samsung's 8 nm 8LPP, a 10 nm extention. [Online]. Available: https://fuse.wikichip.org/news/1443/vlsi-2018-samsungs-8nm-8lpp-a-10nm-extension/

[3] Y. Wang, Y. Tang, L. Sun, and F. Cao, "High performance of junctionless MOSFET with asymmetric gate," *Superlattices and Microstructures*, vol. 97, pp. 8-14, Sep. 2016.

[4] L. Chen, M. Yeh, Y. Lin, *et al.*, "The Physical analysis on electrical junction of junctionless FET," *AIP ADVANCES*, vol. 7, no. 2, pp. 025301-1-5, 2017.

[5] Y. H. Shin, S. Weon, D. Hong, and I. Yun, "Analytical model for junctionless double-gate FET in subthreshold region," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1433-1440, April. 2017.

[6] J. Ajayan, D. Nirmal, P. Prajoon, and J. C. Pravin, "Analysis of nanometer-scale InGaAs/InAs/InGaAs composite channel MOSFETs using high-k dielectric for high speed applications," *International Journal of Electronics and Communications*, vol. 79, pp. 151-157, Sep. 2017.

[7] R. K. Baryah and R. P. Paily, "A dual-material gate junctionless transistor with high-k spacer for enhanced analog performance," *IEEE Trans. Electron. Dev*., vol. 61, no. 1, pp. 123-128, Jan. 2014.

[8] P. S. Raja and R. J. Daniel, "Effect of gate dielectric on threshold voltage of nanoscale MOSFETs," *Int. Journal of Engineering Research and Development*, vol. 5, no. 3, pp. 93-104, 2012.

[9] V. Kumar, R. Gupta, R. P. P. Singh, and R. Vaid, "Performance analysis of double gate n-FinFET using high-k dielectric materials," *Int. Journal of Innovative Research in Science, Engineering and Technology*, vol. 5, no. 7, 13242-13249, 2016.

[10] A. Baidya, S. Baishya, and T. R. Lenka, "Impact of thin high-k dielectric and gate metals on RF characteristics of 3D double gate junctionless transistor," *Materials Science in Semicoductor Processing*, vol. 71, pp. 413-420, 2017.

[11] A. Ali, D. Seo, and I. H. Cho, "Investigation of junction-less tunneling field effect transistor (JL-TFET) with floating gate," *J. of Semiconductor Technology and Science*, vol. 17, no.1, pp. 156-161, Feb. 2017.

[12] J. C. Pravin, D. Nirmal, P. Prajoon, and J. Ajayan, "Implementation of nanoscale circuit using dual metal gate engineered nanowire MOSFET with high-k dielectrics for low power applications," *Physica E*, vol. 83, pp. 95-100, Sep. 2016.

[13] J. Robertson, "High dielectric constant oxides," *Eur. Phys. J. Appl. Phys.*, vol. 28, pp. 265-291, 2004.

[14] G. L. Priya and N. B. Balamurugan, "New dual material double gate junctionless tunnel FET: Subthreshold modeling and simulation," *Int. Journal of Electronics and Communications*, vol. 99, pp. 130-138, Feb. 2019.

[15] Sakshi, S. Dhariwal, and A. Singh, "Analyzing the effect of gate dielectric on the leakage currents," in *Proc. MATEC Web of Conferences*, 2016.

[16] Q. Xie, Z. Wang, and Y. Taur, "Analysis of short-channel effects in junctionless DG MOSFETs," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3511-3514, Aug. 2017.

[17] Nirmal, V. Kumar, P. C. Samuel, Shruthi, D. M. Thomas, and M. Kumar, "Analysis of dual gate MOSFETs using high k dielectrics," in *Proc. 2011 3rd International Conference on Electronics Computer Technology*, Kanyakumari, India, April 2011.

[18] A. Singh, S. Chaudhury, C. K. Pandey, *et al.*, "Design and analysis of high k silicon nanotube tunnel FET device," *IET Circuits, Devices & Systems*, vol. 13, no. 8, pp. 1305-1310, 2019.

[19] J. Colinge, C. Lee, A. Afzalian, *et al.*, "Nanowire transistors without junctions," *Nature Nanotechnology*, vol. 5, no. 3, pp. 225-229, Mar. 2010.

[20] K. E. Kaharudin, F. Salehuddin, A. S. M. Zain, and A. F. Roslan, "Geometric and process design of ultra-thin junctionless double gate vertical MOSFETs," *International Journal of Electrical and Computer Engineering*, vol. 9, no. 4, pp. 2863-2873, Aug. 2019.

[21] H. Jung, "Analysis of threshold voltage roll-off and drain induced barrier lowering in junction-based and junctionless double gate MOSFET," *J. Korean Inst. Electr. Electron. Mater. Eng*., vol. 32, no. 2, pp. 104-109, March 2019.

[22] C. Jiang, R. Liang, J. Wang, and J. Xu, "A two-dimensional analytical model for short channel junctionless double-gate MOSFETs," *AIP Advances*, vol. 5, no. 5, pp. 057122-1-13, 2015.

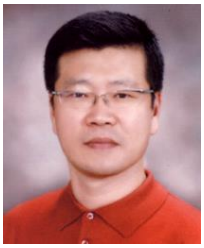
[23] H. Jung, "Analysis of subthreshold swing in symmetric junctionless double gate MOSFET using high-k gate oxides," *International Journal of Electrical and Electronic Engineering & Telecommunications*, vol. 8, no. 6, pp. 334-339, November 2019.

[24] J. Innocenti, L. Welter, F. Julien, *et al.*, "Dynamic power reduction through process and design optimizations on CMOS 80 nm embedded non-volatile memories technology," in *Proc. 2014 IEEE 57th International Midwest Symposium on Circuits and Systems*, 2014.

[25] Ambika and G. Dhiman, "Investigation of junction-less double gate MOSFET with high-k gate-oxide and metal gate layers," *Int. of Innovative Technology and Exploring Engineering*, vol. 8, no. 6S3, April 2019.

[26] S. I. Amin and R. K. Sarin, "Junctionless transistor: A review," in Proc. *Third Int. Conf. on Computational Intelligence and Information Technology*, India, 2013.

[27] S. Dimitrijev, *Principles of Semiconductor Devices*, 2nd ed., New York: Oxford University Press, 2012.



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