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Analytical and experimental evaluation of SiC-inverter nonlinearities for traction drives used in eletric vehicles

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***Abstract*—This paper investigates the inverter nonlinearities in a drive system based on SiC-MOSFETs and compares its performance with that of an equivalent Si-IGBT system. Initially, a novel comprehensive analytical model of the inverter voltage distortion is developed. Not only voltage drops, dead time and output capacitance, but also switching delay times and voltage overshoot of the power devices are taken into account in the model. Such a model yields a more accurate prediction of the inverter's output voltage distortion, and is validated by experimentation. Due to inherent shortcomings of the commonly used double pulse test (DPT), the switching characteristics of both SiC-MOSFETs and Si-IGBTs in the PWM inverter are tested instead, such that the actual performances of the SiC and Si devices in the motor drive system are examined. Then, the switching performance is incorporated into the physical model to quantify the distorted voltages of both the SiC-based and Si-based systems. The results show that, despite its existing nonlinearities, the SiC-based drive has lower voltage distortion compared to the conventional Si-based drive as a result of its shorter switching times and smaller voltage drop, as well as a higher efficiency. Finally, theoverriding operational advantages of the SiC-based drive over its Si-based counterpart is fully demonstrated by comprehensive performance comparisons.**

***Index Terms*—Silicon (Si), Silicon Carbide (SiC), Electric vehicles (EVs), Inverter nonlinearity, Voltage Distortion, Efficiency**

I. INTRODUCTION

DUE to global energy crisis and environmental pollution, the past decade has witnessed the rapid developments of new green energy technologies in Electric Vehicles (EVs), Hybrid Electric Vehicles (HEVs) and Plug-in Hybrid Electric Vehicles (PHEVs). The electrification of transportation is widely accepted as one of the most promising solutions to meet the future challenges, as electrification generally embraces a diversity of energy sources including, importantly, the renewable energy. A wide range of technologies centering around the powertrain of the EV/HEV/PHEV have been reported in the literature [1-11]. The main challenge remains the limited cruising range due to the small battery capacity and the slow charging times due to the available battery charging technologies [3-7]. Therefore, it is important to maximize the efficiency of every component in the powertrain [8]. Meanwhile, it is noteworthy that power semiconductors play key roles in each powertrain subsystem, such as the motor drive and the battery charging unit [1, 9]. Therefore, the overall efficiencies of these vehicles are heavily dependent on the efficiencies of the power electronics in these subsystems.

Currently, conventional silicon (Si) insulated-gate bipolar transistor (IGBT) or Si metal-oxide-semiconductor field-effect transistor (MOSFET) technologies dominate the semiconductor fields in the application of power inverters. However, the Si IGBT is now reaching its theoretical limits due to the demands for higher efficiency, higher power density and higher temperature operations in traction inverters in EVs/HEVs/PHEVs. Recently, wide-bandgap (WBG) silicon carbide (SiC) MOSFET exhibits great potential to replace Si as the dominant transistor technology because of its superior operational characteristics such as faster switching, lower voltage drop, higher blocking voltage, and higher operating temperature [1-2, 12-17]. As a result, a motor drive inverter with SiC devices can produce higher efficiency and higher power density in comparison with their Si counterparts [9-10, 18-21].

Many valuable studies involving SiC have been widely conducted by many researchers [1-2, 9-21]. Most of the work reflects an enormous effort in investigating the switching and conducting losses of SiC [1, 9, 12-23]. For example, the loss model of SiC, in which both the conduction loss and switching loss of SiC are less than that of Si. The efficiency of the inverter based on SiC is 99.1%, while the Si-inverter is 97.1% [22-23]. In addition, the fuel economy of EV/HEV/PHEV is improved because of the lower losses of SiC [2, 10]. The fuel economy in the standard Japanese JC08 test cycle was improved by approximately 5% when the Si IGBTs and diodes in the boost

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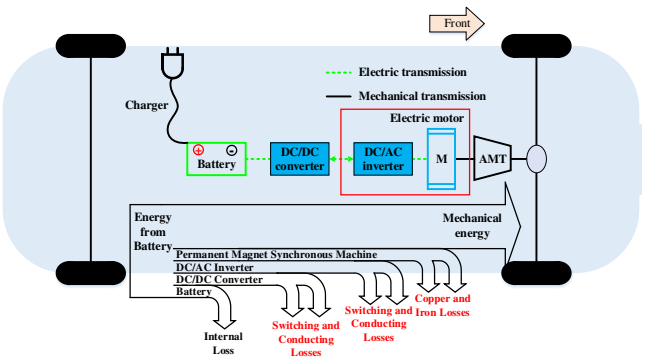


Fig. 1.The components of traction system in EV and corresponding losses.

converter, motor inverter, and generator converter circuit of a third-generation Prius were replaced with SiC MOSFETs and junction barrier Schottky (JBS) diodes [2]. The application of the SiC inverters in the PHEV and conventional HEV improve the fuel economy by 18.1% and 14.7%, respectively [10].

The above work mostly focuses on the losses of SiC and the impact of SiC for the fuel economy. However, according to the literature, the impact of SiC-inverter on the copper and iron losses in the motor has not been explored systematically yet. The components of the traction system in EV and corresponding losses are shown in Fig.1. The losses of the motor are comparable with that of the inverter. The copper and iron losses of the motor are directly related to the output voltage distortion and current distortion of the inverter, namely inverter nonlinearities[24]. Therefore, this paper proposes to investigate the voltage and current distortions in the permanent magnet synchronous motor(PMSM) drive system with a SiC-MOSFET based inverter, and compares it with Si-IGBT based inverter. Furthermore, the overall efficiency of the traction system with the consideration of the inverter nonlinearities is examined.

In the voltage-fed PWM inverter, there are several factors for the distortions in the output voltage and current. The first is the dead time, while other factors originate from the inherent characteristics of the switching devices such as switching time, voltage drop, output capacitance and voltage overshoot [25-30]. The switching time is the time that the switch takes to turn on or off from when it is commanded to do so. The output capacitance causes changes in the slope of the rising and falling edges of the output voltage due to the fact that the current charges up the output capacitance prior to flowing through the freewheel diode [30]. The switching time is also affected by the output capacitance in such a way that switching time and output capacitance combine to produce a distorted voltage, particularly at light load when the phase current is small. Voltage drop is another source of distortion in the output voltage, which can be modeled as a constant voltage plus an equivalent resistor.

The finite turn-off time may cause a short-circuit at the instant of switchover between the two power devices in a phase leg. Dead time, also known as shoot-through delay [31], is employed to prevent the dc link from being short-circuited. Although the dead time guarantees safe operation, it adversely degrades the output voltage of the inverter. For the traction drive inverter with a relative large current, a dead time of a few microseconds ranging from 2-8μs is required to ensure reliable current switchover. The longer the dead time means the more the distortion voltage. Although the length of dead time is set by control command, it also directly depends on the switching time of the device. Meanwhile, the voltage overshoot, or switching oscillation, is also closely related to the fast characteristics of the power devices. Therefore, the switching characteristics of the power devices play an important role in the voltage and current distortions.

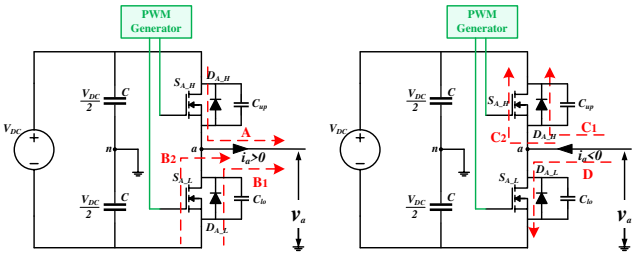
For a systematic study of the voltage distortion in a PMSM drive with SiC-MOSFETs based inverter, this paper will explore both the aspects of modeling and experimentation. First, a comprehensive modeling of the inverter distortion voltage is established by a set of parameters of the switching devices. The model not only considers the impact factors of the voltage drops, dead time and output capacitance, but also takes switching delay times and voltage overshoot into account. As such, the model yields more accurate performance prediction of inverter output. Then detailed evaluation of the real switching characteristics of the devices the PMSM drive system is undertaken through testing them on specifically built experimental benches.

Subsequently, the actual switching performances of the SiC and Si are tested when the devices are used in the traction system, instead of using the conventional switching performance evaluation methodology of double pulse test (DPT), which generally results in overestimations [32-37]. Furthermore, the measured switching performances of both SiC and Si devices are combined with the analytical model to quantify the distorted voltages. The results of this paper show that the SiC-based drive has lower voltage distortion compared to the conventional Si-based drive, especially when the motor operates at light load and low speed. The drive's lower voltage distortion also has positive impacts on both the harmonic components and the amplitude of the phase current. And the motor efficiency is also improved when the same motor is fed by the SiC inverter, resulting in the efficiency of the overall SiC inverter-motor system being much higher than that of Si inverter-motor system.

The remainder of this paper is organized as follows. In Section II, the comprehensive model for describing the inverter voltage distortion is developed. In Section III, experimental setup is illustrated and the characteristics of the switching devices evaluated. In Section IV, the inverter nonlinearities and efficiency of the system are described and analyzed based on experimental results. Conclusions are drawn in the final section.

II. Modeling Voltage Waveform Distortion

There are many previous works related to the voltage distortion of the inverter [24-31]. This paper will highlight the different voltage drop modes between Si IGBT and SiC MOSFET, and additionally considers switching delay times and voltage overshoot effect due to the high dv/dt and high di/dt of SiC. Hence, a more comprehensive model of voltage waveform distortion gives a thorough investigation of



(a) (b)

Fig. 2. One phase leg of an inverter with output capacitances. (a) Positive current flows into the motor. (b) Negative current flows into the phase leg

SiC-inverter.

In order to describe succinctly the voltage distortion in the PMSM drive, it is sufficient to consider only one phase leg of the inverter as shown in Fig. 2. The results of the other legs can be readily deduced.

The circuit in discussion consists of two power devices SA_H and SA_L, two freewheeling diodes DA_H and DA_L, and two output capacitors Cup and Clo. A PWM generator sends out PWM signals to drive the gates of the power switches. Each of the phase leg is connected to the respective motor phase terminal. Its current ia is defined positive when it flows into the motor's phase 'a' as shown in Fig. 2(a). Due to the inductive behavior of the motor, the output current of the leg is assumed constant during the relatively short switching period. Given the differences of the characteristics between SiC and Si devices, the voltage distortions induced by voltage drops, dead times, switching delay times, output capacitance and voltage overshoot are modeled accordingly as follows.

A. *Voltage drop effect*

First an analysis is carried out based on the voltage drop across the power device (Si IGBT or SiC MOSFET) being contingent on the direction of the phase current i_a. The SiC MOSFET is characterized with the third quadrant operation mode, which is distinct with Si IGBT [38-39]. Si IGBT is a unilateral conduction device. Hence, the voltage drops for Si IGBT and SiC MOSFET system should be modeled separately.

The current pathway for Si IGBT is shown in Fig. 2. When the current $i_a>0$, the current follows through pathway A or B_1. B_1 is the freewheeling diode, due to the unilateral conduction of Si. When the current $i_a<0$, the current follows through pathway C_1 or D. The model of voltage drop of Si IGBT is proposed in [25].

The current pathway for SiC is also shown in Fig. 2. When the current flow through pathway A or D, the voltage drop models of SiC MOSFET can be expressed as the same as the models of Si IGBT described in [25].

$$v_a = V_{DC}/2 - V_T,\ i_a > 0 \tag{1}$$

$$v_a = -V_{DC}/2 + V_T,\ i_a < 0 \tag{2}$$

where, V_T is the voltage drop of SiC MOSFET.

$$V_T = V_{T0} + r_T |i_a| \tag{3}$$

where, V_{T0} is threshold voltage of the active switch and r_T is on-state slope resistance of the active switch.

When the current flows through pathway B_1 or C_1, namely the freewheeling diode, in the Si based system, the current will flow through pathway B_2 or C_2, namely the SiC MOSFET, according to the third quadrant operation mode of SiC MOSFET.

As shown in Fig. 2(a), when the current $i_a>0$, S_{A_H} is in turn-off state while S_{A_L} is in conduction state. The SiC works as the third quadrant operation mode. Hence, the current follows through pathway B_2, the output voltage v_a can be calculated as,

$$v_a = -V_{DC}/2 - V_{T1} \tag{4}$$

where, V_{T1} is the reverse voltage drop of the SiC MOSFET.

As shown in Fig. 2(b), when the current $i_a<0$, and the current follows through pathway C_2, the output voltage v_a can be calculated as,

$$v_a = V_{DC}/2 + V_{T1} \tag{5}$$

The output voltage is asymmetric and the voltage drop reduces the output voltage when the phase current is positive, and boosts the output voltage when the phase current is negative as shown in Fig. 3. V_{err} is denoted as distortion of the inverter output voltage, which will be referred to as "distortion voltage". The distortion voltage V_{err} is defined as the difference between the real output voltage v_a and the ideal output voltage v_a^* as follows,

$$V_{err} = v_a - v_a^* \tag{6}$$

Therefore, the distortion voltage of SiC induced by voltage drop V_{err1} could be expressed as follows,

When $i_a>0$, $V_{err1} = -V_T \cdot D - V_{T1} \cdot (1-D)$

When $i_a<0$, $V_{err1} = V_T \cdot D + V_{T1} \cdot (1-D)$

where, D is duty cycle. Therefore,

$$V_{err1} = -\left(V_T \cdot D + V_{T1} \cdot (1-D)\right) \cdot sign(i_a) \tag{7}$$

where,

$$sign(i_n) = \begin{cases} 1, & i_n > 0 \\ -1, & i_n < 0 \end{cases},\quad \text{n=a,b,c} \tag{8}$$

The average distorted voltage of A-phase V_{as1} in the SiC system can be expressed according to the directions of the three phase currents as [25],

$$\begin{aligned} V_{as1} &= -\left(V_T \cdot D + V_{T1} \cdot (1-D)\right) \cdot \left(\left(2sign(i_a) - sign(i_b) - sign(i_c)\right)/3\right) \\ &= \Delta V_1 \cdot \left(\left(2sign(i_a) - sign(i_b) - sign(i_c)\right)/3\right) \end{aligned} \tag{9}$$

B. *Dead time effect*

Since a switching device has a finite switching time, the dead time should be considered in the PWM gating signals in order to prevent the simultaneous conduction of two switching devices in the same leg. Although the dead time is very short, it leads to distortion of the output voltages and currents.

As shown in Fig. 2, during the dead time T_{dt}, both of the switching devices in one phase leg cease to conduct, and one of the diodes conducts. If the current polarity is positive, the lower diode will conduct. Otherwise, the upper diode will conduct. Therefore, the output voltage depends on the direction of the A-phase current i_a, as shown in Fig. 4.

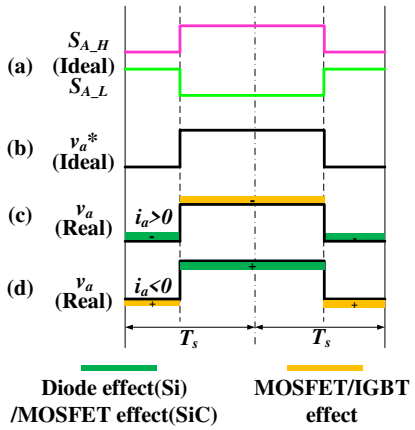


Fig. 3. Output voltage waveforms taking voltage drops effect into account

Fig. 4 shows the gating signals and voltage waveforms in one PWM cycle including the dead time. The voltage gain or loss between ideal and real swichings are highlighted by colored areas and identified by + and – sign, which represents that the corresponding contribution to increase or decrease the output voltage averaged over the switching period T_s. Fig. 4(a) and (b) show the gating signals for the two switches in ideal condition and the presence of a dead time, respectively. The distorted voltage caused by the dead time are described in Fig. 4(d) and Fig. 4(e) according to the direction of the A-phase current.

When i_a>0, and both of the switching devices in one phase leg cease to conduct during the dead time T_{dt}, whereas the lower diode will conduct. The output voltage v_a is pulling down to $-V_{DC}/2$ during dead time till the dead time ends. Therefore, the average distortion voltage induced by the dead time can be expressed as,

$$V_{err2} = -V_{DC} \cdot T_{dt} / (2T_s) \tag{10}$$

where, the diode voltage is neglected due to the short dead time.

When i_a<0, and both of the switching devices in one phase leg cease to conduct during the dead time T_{dt}, the upper diode will conduct. The output voltage v_a is pulling up to $V_{DC}/2$ during dead time till the dead time ends. Therefore, the average distortion voltage induced by dead time can be expressed as,

$$V_{err2} = V_{DC} \cdot T_{dt} / (2T_s) \tag{11}$$

Hence, combining equation (10) and (11), the distortion voltage is rewritten as a function of the phase current sign,

$$V_{err2} = \left(-V_{DC} \cdot T_{dt} / (2T_s)\right) \cdot sign(i_n) \tag{12}$$

The average distorted voltage of A-phase induced by the dead time could be expressed according to the directions of the three phase currents as,

$$\begin{aligned} V_{as2} &= \left(-V_{DC} \cdot T_{dt} / (2T_s)\right) \cdot \left(\left(2sign(i_a) - sign(i_b) - sign(i_c)\right)/3\right) \\ &= \Delta V_2 \cdot \left(\left(2sign(i_a) - sign(i_b) - sign(i_c)\right)/3\right) \end{aligned} \tag{13}$$

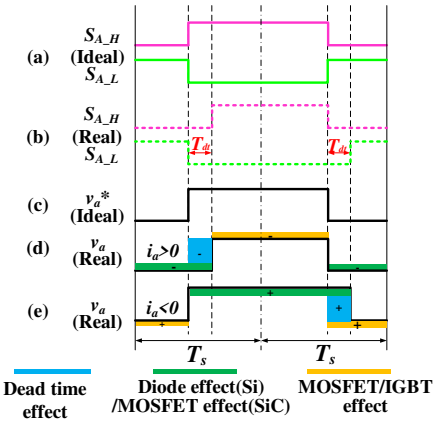


Fig. 4. Output voltage waveform during dead time taking voltage drops and dead time effects into account

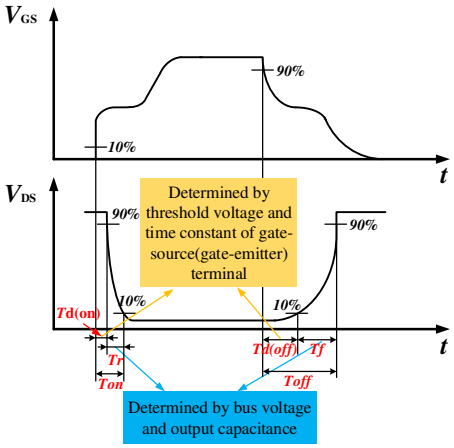


Fig. 5. The definition of switching time

C. *Switching delay times effect*

Apart from the voltage drops and dead time, the switching time also contributes to the distorted voltage (V_{err}). As shown in Fig. 5, the turn on time (T_{on}) is defined as the sum of turn on delay time ($T_{d(on)}$) and rising time (T_r), and the turn off time (T_{off}) is defined as the sum of turn off delay time ($T_{d(off)}$) and falling time (T_f). The switching delay times are associated with threshold voltage and time constant of the gate-source (gate-emitter) terminal, whereas the rising and falling times depend critically on the bus voltage, output capacitance and phase current.

In this section the distorted voltage induced by switching delay times is modeled. After the dead time T_{dt}, when i_a>0 the upper switching device starts to conduct. The output voltage v_a is still equal to $-V_{DC}/2$ until the turn on delay process of switching device ends shown as the red area in Fig. 6(d). After the turn on delay process, the output voltage v_a is pulling up to $V_{DC}/2$. And the purple area is effected by the finite turn off delay process of the upper switching device as well as when i_a>0. Therefore, when i_a>0, the average distortion voltage induced by switching delay time can be expressed as,

$$V_{err3} = \left(-V_{DC} \cdot T_{d(on)} + V_{DC} \cdot T_{d(off)}\right) / (2T_S) = V_{DC} \cdot \left(T_{d(off)} - T_{d(on)}\right) / (2T_S) \tag{14}$$

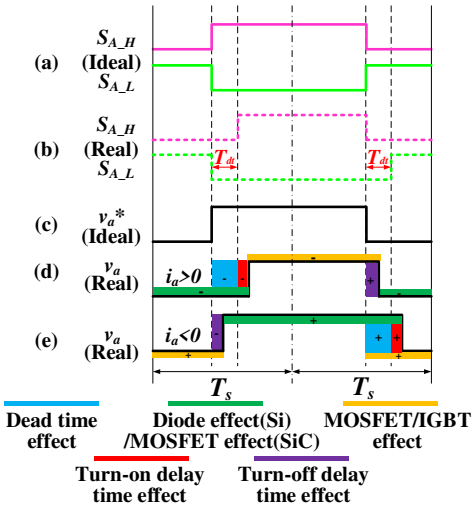


Fig. 6. Output voltage waveform during dead time taking voltage drops, dead time and switching. delay times effects into account

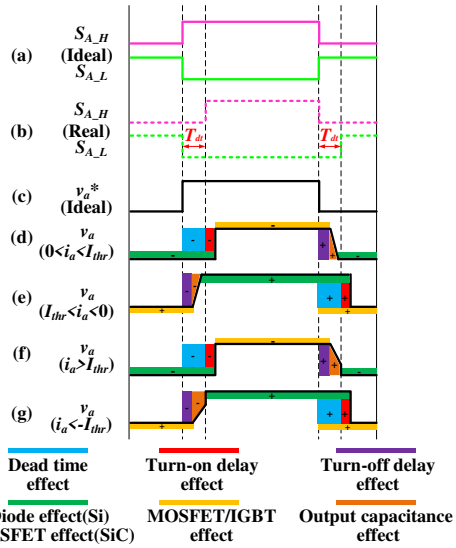


Fig. 7. Output voltage waveform during dead time taking voltage drops, dead time, switching delay times and output capacitance effects into account

When i_a<0, the purple area is effected by the finite turn off delay process of the low switching device as shown in Fig. 6(e). After the dead time T_{dt}, the low switching device starts to conduct. The output voltage v_a is still equal to $V_{DC}/2$ until the turn on delay process of switching device ends shown as red area in Fig. 6(e). After turn on delay process, the output voltage v_a is pulling down to $-V_{DC}/2$. Therefore, when i_a<0, the average distortion voltage induced by switching time could be expressed as,

$$V_{err3}=\left(V_{DC}\cdot T_{d(on)}-V_{DC}\cdot T_{d(off)}\right)/\left(2T_S\right)=-V_{DC}\cdot\left(T_{d(off)}-T_{d(on)}\right)/\left(2T_S\right) \quad (15)$$

Hence, combining equation (14) and (15), the distortion voltage is also rewritten as a function of the phase current sign,

$$V_{err3}=\left(\left(T_{d(off)}-T_{d(on)}\right)/\left(2T_S\right)\right)\cdot V_{DC}\cdot sign(i_a) \quad (16)$$

The average distorted voltage of A-phase induced by switching time can be expressed according to the directions of the three phase currents as,

$$\begin{aligned}V_{as3}&=\left(\left(T_{d(off)}-T_{d(on)}\right)/\left(2T_S\right)\right)\cdot V_{DC}\cdot\left(\left(2sign(i_a)-sign(i_b)-sign(i_c)\right)/3\right)\\&=\Delta V_3\cdot\left(\left(2sign(i_a)-sign(i_b)-sign(i_c)\right)/3\right)\end{aligned} \quad (17)$$

D. Output capacitance effect

The output capacitances of one phase leg are shown in Fig. 2. During the dead time T_{dt}, the output current i_a would charge and discharge the output capacitances due to the freewheeling diodes. Pathway B is one of the possible situations shown in Fig. 2(a). i_a is positive at the instant that S_{A_H} turns off and S_{A_L} ceases to conduct. The current is supposed to flow through D_{A_L} and pull down the output voltage v_a to $-V_{DC}/2$ immediately if no output capacitance is added. In fact, the falling edge of the output voltage v_a is not straight as the lower capacitance C_{lo} has to be discharged and the upper one C_{up} to be charged.

The voltage distortion caused by output capacitance could be classified as two situations, by comparing the charging or discharging time with the dead time. If the absolute value of i_a is high enough to finish the charging (or discharging) before dead time ends, and the influenced edge of v_a is a continuous slope as shown in Fig. 7(d) and (e). Otherwise, if the charging (or discharging) time is longer than the dead time, a discontinuity of v_a would occur at the end of the dead time as shown in Fig. 7(f) and (g). When the charging (or discharging) time equal to the dead time, the output current i_a is defined as a threshold value I_{thr}. Using Pathway B as an example, the threshold current value I_{thr} can be calculated as follows:

The current flowing through the capacitance is given as:

$$I=C\,dv/dt=C\left(V_2-V_1\right)/\left(t_2-t_1\right) \quad (18)$$

where V_1 is the initial voltage at t_1 and V_2 is the final voltage at t_2. At the threshold condition, t_1=0, t_2=T_{dt}, and the initial and final voltage of C_{lo} and C_{up} shown in Fig.2 are listed taking the MOSFET and diode voltage drops into consideration,

$$\begin{cases}V_{clo}(0)=-V_{DC}/2+V_T\\V_{clo}(T_{dt})=-V_{DC}/2+V_D\end{cases} \quad (19)$$

$$\begin{cases}V_{cup}(0)=-V_{DC}/2-(-V_D)\\V_{cup}(T_{dt})=-V_{DC}/2+V_T\end{cases} \quad (20)$$

where, V_D represents the voltage drop of diode, V_D=V_{D0}+$r_D|i_a|$, V_{D0} is threshold voltage of the freewheeling diode and r_T is on-state slope resistance of the freewheeling diode

Combining equations (18) (19) and (20), the threshold current could be written as,

$$I_{thr}=\left(2C_{oss}\left(V_{DC}+V_D-V_T\right)\right)/T_{dt} \quad (21)$$

where, C_{OSS} is the value of the output capacitance.

As shown in Fig. 7, the brown areas represent the voltage distortion caused by output capacitance. Four expressions of the average voltage distortion V_{err4} are derived according to the four brown areas shown in Fig. 7(d), (e), (f) and (g), respectively.

If 0<i_a<I_{thr},

$$V_{err4}=\left(\left(V_{DC}+V_D-V_T\right)\cdot T_{dt}-\left(|i_a|\cdot T_{dt}^2\right)/4C_{oss}\right)/T_s \quad (22)$$

If i_a>I_{thr},

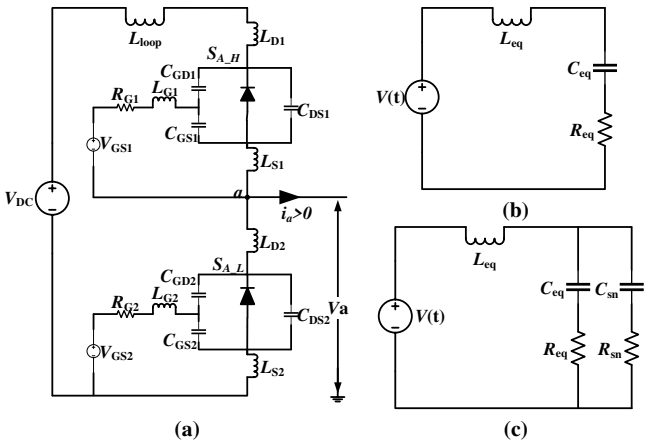


Fig. 8. Inductive load switching circuit for one phase leg. (a) Switching circuit with parasitic elements; (b) *RLC* switching equivalent circuit model; (c) Equivalent circuit with an *RC* snubber

$$V_{err4}=\left(C_{oss}\cdot\left(V_{DC}+V_{TD}-V_T\right)^2/\left|i_a\right|\right)/T_s \tag{23}$$

If $-I_{thr}<i_a<0$,

$$V_{err4}=\left(-\left(V_{DC}+V_D-V_T\right)\cdot T_{dt}+\left(\left|i_a\right|\cdot T_{dt}^2\right)/4C_{oss}\right)/T_s \tag{24}$$

If $i_a<-I_{thr}$,

$$V_{err4}=\left(-C_{oss}\cdot\left(V_{DC}+V_D-V_T\right)^2/\left|i_a\right|\right)/T_s \tag{25}$$

By using $sign(i_a)$, equations (22)-(25) can be rewritten as,

$$V_{err4}=\begin{cases}\left(\left(\left(V_{DC}+V_D-V_T\right)\cdot T_{dt}-\left(\left|i_a\right|\cdot T_{dt}^2\right)/4C_{oss}\right)/T_s\right)\cdot sign(i_a), & \left|i_a\right|<I_{thr}\\ \left(\left(C_{oss}\cdot\left(V_{DC}+V_D-V_T\right)^2/\left|i_a\right|\right)/T_s\right)\cdot sign(i_a), & \left|i_a\right|>I_{thr}\end{cases} \tag{26}$$

In fact, when inverter operating, the amplitude of i_a is far above threshold current I_{thr}. As a result, V_{err4} can be approximately expressed as,

$$V_{err4}=\left(\left(C_{oss}\cdot\left(V_{DC}+V_D-V_T\right)^2/\left|i_a\right|\right)/T_s\right)\cdot sign(i_a) \tag{27}$$

The average distorted phase-to-center voltages are obtained according to the direction of the respective three-phase currents as,

$$V_{as4}=\left(\left(C_{oss}\cdot\left(V_{DC}+V_D-V_T\right)^2\right)/3T_s\right)\cdot\left(2/i_a-1/i_b-1/i_c\right) \tag{28}$$

E. Voltage overshoot effect

The phase voltage waveform is also impacted by the parasitic inductances of the circuit. Fig. 8 (a) shows the switching device's internal parasitic inductances L_G, L_D, L_S, and the switching loop inductance L_{loop}, which represents the equivalent parasitic inductance for the total circuit loop. Hence, the voltage overshoot, or the switching oscillation, is induced and closely related to the fast switching characteristics of the power devices. An *RLC* equivalent circuit model is proposed for the switching transient of one SiC MOSFET [40]. This Section goes further by investigating the phase voltage overshoot of the inverter based on the *RLC* model.

The simplified equivalent circuit for turn off process is shown in Fig.8 (b). The equivalent capacitance C_{ep} is developed as,

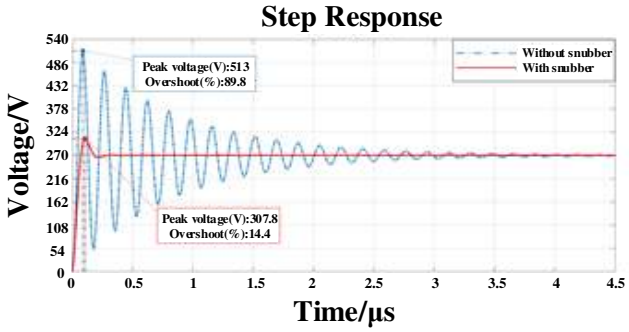


Fig. 9. The drain–source voltage turn off ringing of SiC MOSFET

$$C_{eq}=\frac{C_{DS}C_{GS}+C_{DS}C_{GD}+C_{GS}C_{GD}}{C_{GS}} \tag{29}$$

where, $C_{GD}=C_{rss}$, $C_{DS}=C_{oss}$-C_{GD}, $C_{GS}=C_{iss}$-C_{GD}. The input capacitance C_{iss}, output capacitance C_{oss} and reverse transfer capacitance C_{rss} can be obtained from the corresponding datasheets.

The equivalent resistance R_{ep} can be expressed as [38],

$$R_{eq}=R_G\cdot\frac{(\omega_{OFF}L_S-\frac{1}{\omega_{OFF}C_S})^2}{R_G^2+(\omega_{OFF}L_G+\omega_{OFF}L_S-\frac{1}{\omega_{OFF}C_G}-\frac{1}{\omega_{OFF}C_S})^2} \tag{30}$$

where, R_g is the internal gate resistance,

$C_S=\frac{C_{DS}C_{GS}+C_{DS}C_{GD}+C_{GS}C_{GD}}{C_{GD}}$, $C_G=\frac{C_{DS}C_{GS}+C_{DS}C_{GD}+C_{GS}C_{GD}}{C_{DS}}$,

$\omega_{OFF}\approx\frac{1}{\sqrt{(L_{eq}+L_S)\cdot(C_{GD}+C_{GS})}}$, $L_{eq}=L_{loop}+2L_D+L_S$. L_G, L_D and L_S represent gate inductance, drain inductance and source inductance, respectively.

According to the second-order equivalent circuit model of device turn-off, the transfer function of the output voltage is developed as,

$$G_1(s)=\frac{R_{eq}C_{eq}\cdot s+1}{L_{eq}C_{eq}\cdot s^2+R_{eq}C_{eq}\cdot s+1} \tag{31}$$

The second-order switching circuit is usually in an underdamped situation, which means the phase output voltage contains overshoot and may damage the system performance. Thus, an *RC* snubber circuit is designed to suppress the turn off overshoot as shown in Fig.8 (c). The second-order circuit is converted into a third-order circuit. Through choosing the proper values of R_{sn} and C_{sn} in the third-order circuit, it can be changed from underdamped condition to critically damped or overdamped condition. The transfer function of output voltage in the third-order circuit is derived as,

$$G_2(s)=\frac{R_{eq}R_{sn}C_{eq}C_{sn}\cdot s^2+(R_{eq}C_{eq}+R_{sn}C_{sn})\cdot s+1}{(R_{eq}+R_{sn})L_{eq}C_{eq}C_{sn}\cdot s^3+[(C_{eq}+C_{sn})L_{eq}+R_{eq}R_{sn}C_{eq}C_{sn}]\cdot s^2+(R_{eq}C_{eq}+R_{sn}C_{sn})\cdot s+1} \tag{32}$$

The responses of the two transfer functions for the second-order and third-order circuits are simulated in Matlab. The simulated waveforms with and without the snubber circuit shown in Fig. 9. The results show that the circuit with an *RC* snubber can remove the oscillation phenomenon with a 75.4% reduction in the peak voltage overshoot and a decrease in the number of oscillations. Hence, an *RC* snubber circuit is adopted in our real inverter, which will be shown in the Section III.

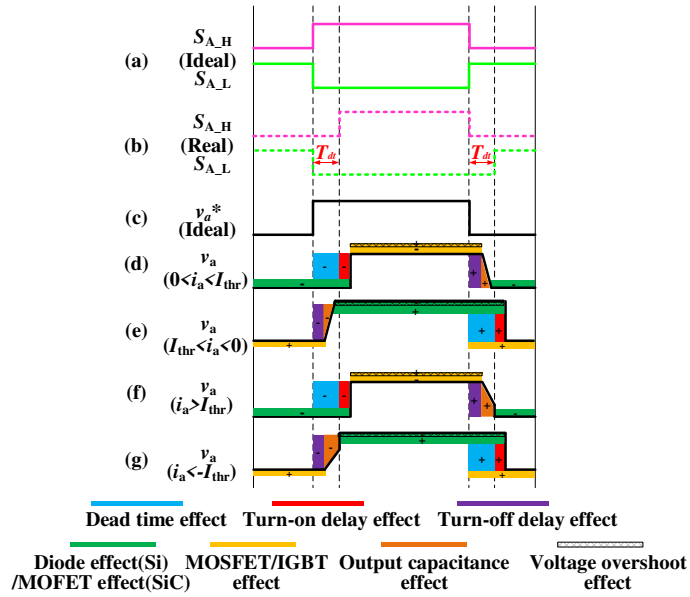


Fig. 10. Output voltage waveform during dead time taking voltage drops, dead time, switching delay times, output capacitance and voltage overshoot effects into account.

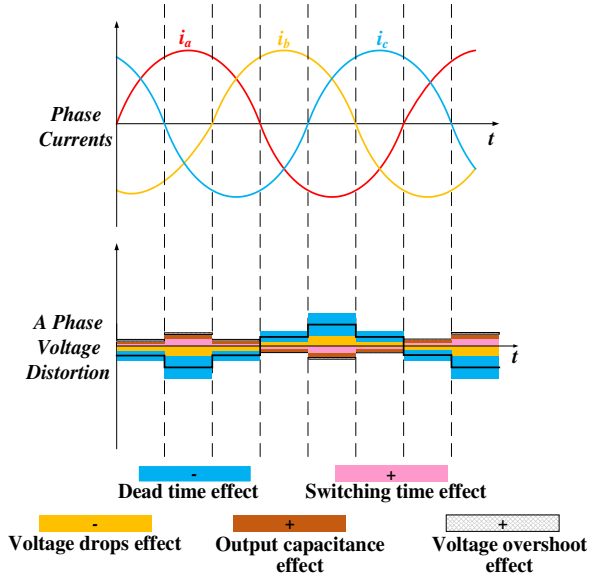


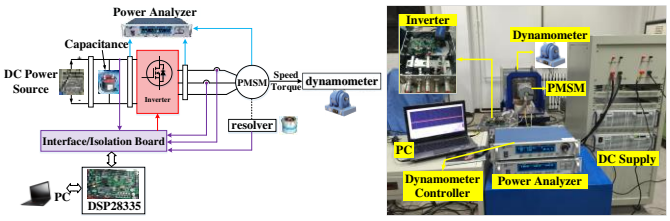
Fig. 11. Average voltage distortion induced by four aspects

Adopting the same analysis methodology used in Section II.A-II.D, the average distortion voltage is similarly developed as a function of the phase current sign,

$$V_{err3} = \left(\Delta V_{os} t_r / \left(4T_S\right)\right) \cdot sign(i_a) \tag{33}$$

The contribution of voltage overshoot is added into the output voltage waveform shown in Fig.10. The average distorted voltage of A-phase induced by voltage overshoot can be expressed according to the directions of the three phase currents as,

$$\begin{aligned} V_{as5} &= \left(\Delta V_{os} t_r / \left(4T_S\right)\right) \cdot \left(\left(2sign\left(i_a\right) - sign\left(i_b\right) - sign\left(i_c\right)\right)/3\right) \\ &= \Delta V_5 \cdot \left(\left(2sign\left(i_a\right) - sign\left(i_b\right) - sign\left(i_c\right)\right)/3\right) \end{aligned} \tag{34}$$



(a) (b)

Fig. 12. General view of the experimental setup. (a) The block diagram of the experimental setup. (b) The picture of the experimental setup.

TABLE I
Main Parameters of the PMSM

Specifications		Dimensions (mm)	
Rated Power	10kW	Stator inner/outer radius	90/160
Speed	3000rpm	Rotor outer radius/length	88/150
Input DC Voltage	270V	Tooth length/width	23/4
Iron laminations	WGT-150	Slot/ Pole Number	36/6
PM material	SMCo24	Strand diameter	1.25
Phases	3	PM height/length	8/26
Direct-axis inductance	2.22mH	Phase winding resistance	0.5Ω
Quadrature-axis inductance	5.19mH	Permanent magnet flux	0.174Wb

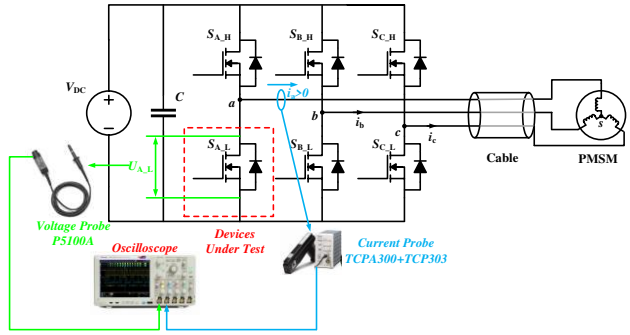


Fig. 13. Layout of the three-phase PMSM drive system.

F. Summary

From Section II.A-II.E，the factors of voltage distortion are analyzed, and the expressions of the phase voltage distortion caused by five contributions are obtained as V_{as1}-V_{as5}. Five expressions illustrate that the phase voltage distortion varies as a function of the phase currents and it has a 6-step waveform. The phase voltage distortion caused by dead time and voltage drops has the opposite phase with the phase current, and distortion caused by switching time, output capacitance and voltage overshoot is in phase with current. Five parts of phase voltage distortion are synthesized as shown in Fig. 11. The area of the blocks represents the absolute value of the phase distorted voltage, and signs are shown in legends.

III. Devices Characteristics Evaluation

A. Experimental setup

To evaluate the actual switching characteristics of SiC and Si in the drive system, and analyze the nonlinearities of SiC and Si inverters experimentally, a complete setup of a PMSM drive system is specifically built as shown in Fig.12. In order to eliminate any unpredictable factors impacting the measurements of the voltage and current waveforms, the same control boards based on DSP28335, same current sensors

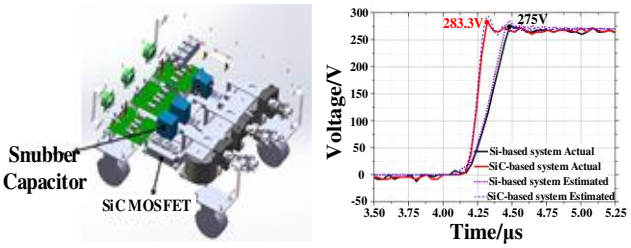


Fig. 14. (a) The inverter with snubber capacitors; (b) Comparison of the voltage overshoots for the Si-based system and SiC-based system.

(LEM DHAB s/14) and one PMSM with a TAMAGAWA resolver (TS2640N321E64) are used in the two test drive systems. Two current sensors are fixed on the cables of Phase A and Phase B, to measure the currents of Phase A and Phase B. The main parameters of the motor used are shown in Table I. With an interior PM rotor, the motor's direct-axis and quadrature-axis inductances are 2.02mH and 5.19mH respectively at rated power.

B. Devices characteristics

Though the parameters of the two devices under study are readily available from the manufacturer's datasheet, they are obtained under special test conditions not usually compatible with the actual motor drive application environments. Moreover, the datasheet often does not provide sufficient information on tolerances. To date, double pulse tester (DPT) is a widely accepted measurement technique to access the switching performance of SiC devices [32-34]. However, according to the intrinsic characteristics of SiC devices, such as small junction capacitance, small on-resistance, and high *di/dt* and *dv/dt* during fast switching transients, their switching behavior becomes more sensitive to parasitics and noise of the application circuit, compared with traditional Si devices [35-37]. It is felt that the DPT may not be adequate for the PWM driven SiC-inverter under study. Therefore, it is decided the real time switching performance of the devices will be measured and systematically evaluated instead, so that factors affecting the voltage distortion can be explored with confidence.

Fig. 13 shows the layout of an overall inverter-PMSM drive system. The voltage and output current of the lower device S_{A_L} are assigned to be tested. The current flowing into the motor is defined as positive, which is same with the definition in Fig. 2. A high precision voltage probe P5100A and current probe TCPA300 plus TCP303 are used to observe the transient process of the voltage and current during turn-on/turn-off of the switching device respectively.

Due to the high *di/dt,* a voltage overshoot could be as high as more than 100V, when the DC voltage is set at 270V. This is not acceptable for a high performance motor drive system. Therefore, the snubber capacitors (EPCOS, B32656A7155) are mounted on the IGBT/MOSFET modules, paralleling with DC source shown in Fig. 14(a). Such capacitors do a good job for voltage overshoot suppression, as shown in Fig. 14(b), in which close agreements between the measurements and the predicted results from the proposed analytical models are also demonstrated. The voltage overshoots of Si- and SiC-based

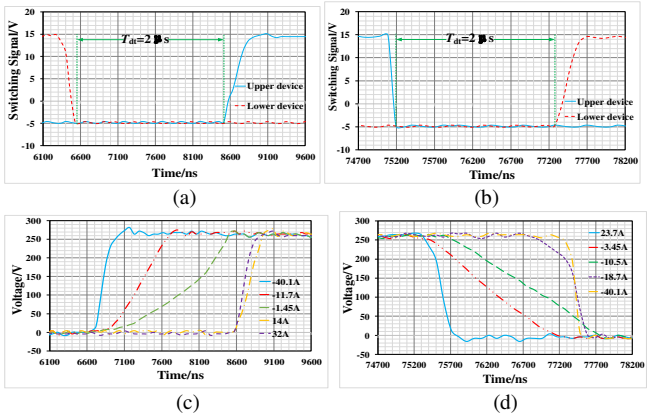


Fig. 15. Rising/Falling edge of output voltage for different current level with output capacitor during dead time in Si drive. (a) Gating signals-turn off low device. (b) Gating signals-turn off upper device. (c) Rising edge of output voltage. (d) Falling edge of output voltage.

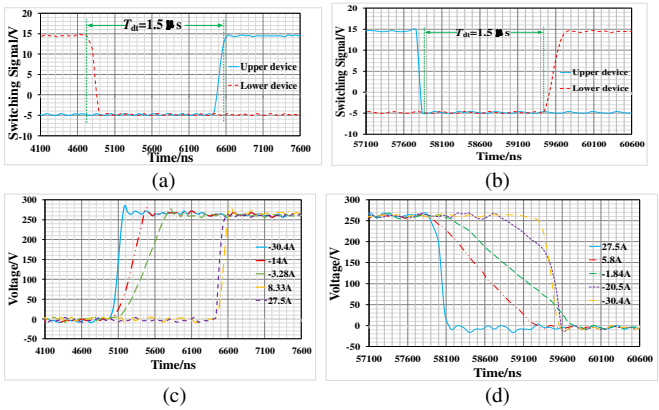


Fig. 16. Rising/Falling edge of output voltage for different current level with output capacitor during dead time in SiC drive. (a) Gating signals-turn off low device. (b) Gating signals-turn off upper device. (c) Rising edge of output voltage. (d) Falling edge of output voltage.

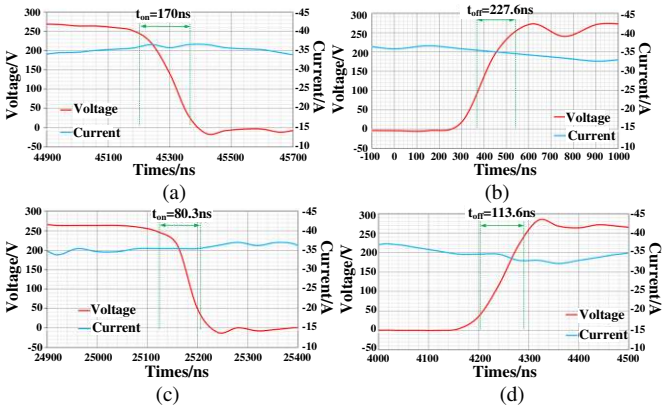


Fig. 17. Turn on/off waveforms of Si and SiC. (a) Turn on waveform of Si with phase current around -35A. (b) Turn off waveform of Si with phase current around -35A. (c) Turn on waveform of SiC with phase current around -35A. (d) Turn off waveform of SiC with phase current around -35A

system are 5V and 13.3V respectively. Furthermore, in order to avoid an occurrence of the reflected wave phenomenon [41], very short feeder cables (0.25m) between the motor and inverter are used in the experiments.

In order to highlight the effect of the phase current on the output voltage and explore the switching time of the devices, the output voltages and corresponding currents are measured simultaneously as shown in Fig. 15 and Fig. 16 for Si and SiC, respectively. When the current is around -40.1A, this large

TABLE II
Datasheet Parameters and Test Parameters

	SiC (Cree CAS300M12BM2)		IGBT (Infineon FF600R12IP4)	
	Datasheet parameters	Experimental results	Datasheet parameters	Experimental results
DC Voltage	600V	270V	600V	270V
Turn on time	144ns	80.3ns	330ns	170ns
Turn off time	211ns	113.6ns	850ns	227.6ns
On State Resistance	5mΩ	6.77mΩ	/	/
Collector-emitter saturation voltage	/	/	1.7V(600A)	1.378V
Diode Forward Voltage	1.7V (300A)	/	1.8V (600A)	/
Output capacitance	/	15.3nf	/	39.7nf
Gate threshold voltage	2.3V	/	5.8V	/
Time constant of gate-source (gate-emitter) terminal	3.5×10^{-8}s	/	6.3×10^{-8}s	/

current begins to charge the lower output capacitance after turning the lower device off as shown in Fig. 15(b), which makes its output voltage rise very fast as shown in the blue line in Fig. 15(c). When the magnitude of the current reduces to -11.7A and -1.45A, the ramp up speeds of the output voltages slow down as shown in the red line and green line, respectively, in Fig. 15(c). When the currents are positive, such as 14A and 32A shown in Fig. 15(c), the voltage stays low till the turning on of the upper device. For the falling edge of the output voltage, similar results are measured as shown in Fig. 15(d). Besides, the rising edge and falling edge of the output voltages for SiC also have similar results as described in Fig. 16(c) and (d). However, both the rising time and the falling time of SiC are shorter than Si due to the small output capacitance, small time constant of gate-source (gate-emitter) terminal and low gate threshold voltage of SiC as shown in Table II. Such parameters promise the quick switching of SiC, which is presented in Section II.C.

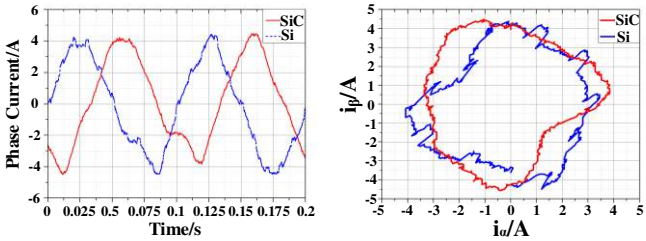
Fig. 17 shows the turn on/off waveforms of Si and SiC with phase current -35A. The voltage falling time of SiC is 113.6ns, which is only half of Si 227.6ns. In addition, the rising time of SiC is 80.3ns, which is also half of Si 170ns. Therefore, it can be concluded that the switching speed of SiC is generally much faster than Si.

The main parameters of the two devices are shown in Table II. The values of the parameters are measured under 600VDC power supply in datasheets while the counterparts are measured under 270VDC power supply in our live experiments.

It can be seen that the switching time of SiC is much smaller than that of Si from the datasheets. The rising time of SiC is half of Si. And the falling time of SiC is only 1/4 of Si. Meanwhile, the resistance of Si is only 5mΩ. Hence, the voltage drops of SiC is much smaller than Si when the phase current is below 100A. Table II also shows the differences between the datasheets and real experimental results. Due to the current and voltage values in experiments are smaller than that in datasheets, both the turn on and turn off time measured from experiments are shorter than the value obtained from datasheets.

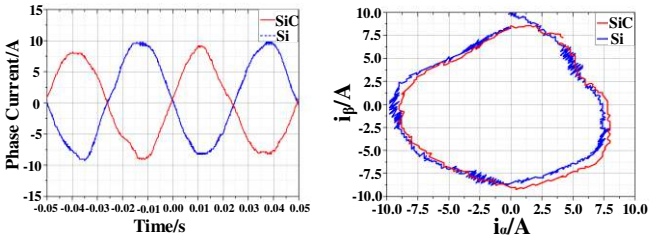
TABLE III
Quantified Distorted Voltages Effected By Four Contributions

	Average distorted voltages of SiC MOSFETs	Average distorted voltages of Si IGBTs	Differences
Dead time effect	-4.05V	-5.40V	-1.35V
Switching delay time effect	0.13V	0.21V	0.08V
Voltage drop effect	-0.24V	-1.59V	-0.64V
Output capacitance effect	0.27V	0.29V	0.02V
Voltage overshoot effect	0.0299V	0.0143V	-0.0156V
Comprehensive effects	-3.86V	-6.48V	-2.62V



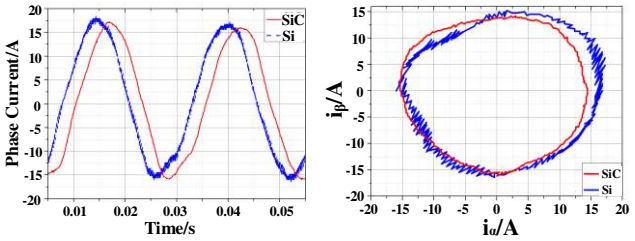
(a) (b)

Fig. 18. Phase current and αβ current waveforms under 200rpm and 1N·m of the motor. (a) Phase current waveforms. (b) αβ current waveforms.



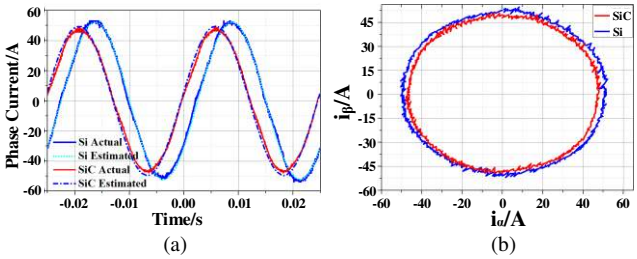
(a) (b)

Fig. 19. Phase current and αβ current waveforms under 400rpm and 4N·m of the motor. (a) Phase current waveforms. (b) αβ current waveforms.



(a) (b)

Fig. 20. Phase current and αβ current waveforms under 800rpm and 8N·m of the motor. (a) Phase current waveforms. (b) αβ current waveforms.



(a) (b)

Fig. 21. Phase current and αβ current waveforms under 800rpm and 24N·m of the motor. (a) Phase current waveforms. (b) αβ current waveforms.

IV. Analyzing Inverter Nonlinearities Experimentally

A. Voltage distortion

In this section, the voltage distortions of both SiC and Si based inverters are quantified and compared. The exact quantities of the voltage distortions can be calculated by substituting the parameters value measured into the models of the voltage distortions developed. The value of voltage distortions due to the different contributions are listed as shown in Table III. It is worth mentioning that the dead times of Si and SiC based inverters are assigned as 2μs and 1.5μs, respectively, due to the turn off times of Si and SiC are 1.56μs at -1.45A and 0.7μs at -3.28A separately.

The dead time and voltage drop have negative distorted voltages, while the switching time, output capacitance and voltage overshoot have positive distorted voltages. And the dead time presents a dominant role, as well as the voltage drop in the comprehensive effects. Compared with Si, the distorted voltages of SiC manifest a smaller value, which benefits from the short switching time, small voltage drop and small output capacitance of SiC.

Due to the relatively low switching frequency (15kHz) used in the current study, the effects of switching delay time, output capacitance and voltage overshoot are really small and could be neglected in this scenario. However, it is known that SiC-MOSFET can operate as an extremely high switching frequency, which is very useful for high speed motors and high speed accuracy motors, etc. The switching delay time, output capacitance and voltage overshoot will have higher impact on the inverter non-linearity.

B. Phase current distortion

The phase current is directly related with the phase voltage. Hence, the inverter nonlinearities could also be observed by the current waveform. Fig. 18-Fig. 21 show the measured phase currents when the system operates at different speeds and different torques. The switching frequency is set to 15kHz for both SiC and Si drive systems. It can be seen that the current waveforms of Si-inverter have more harmonics than its counterparts in SiC-inverter. The less current harmonics of SiC-inverter benefits from the smaller voltage distortion as analyzed in SectionIV.A. In turn, the smaller voltage distortion of SiC-inverter, calculated by the proposed model, is effectively validated by the less harmonics in phase current measured by experiments.

It is also observed that the relative voltage deviation is more significant at small output voltage. As a result, the current distortion different is more severe at low output fundamental phase current. For example, comparing Fig. 18(a) and (b), the harmonic components of the phase current within Si-drive are more than SiC. However, comparing Fig. 21(a) and (b), the current harmonic components in comparison to the large amplitude of fundamental phase current of Si-drive is small and could be comparable to the counterpart of SiC-drive. Therefore, SiC-drive manifests its advantage more apparently when the motor operates at low power rating. Such a conclusion will be further confirmed by the efficiency analysis in Section IV.C.

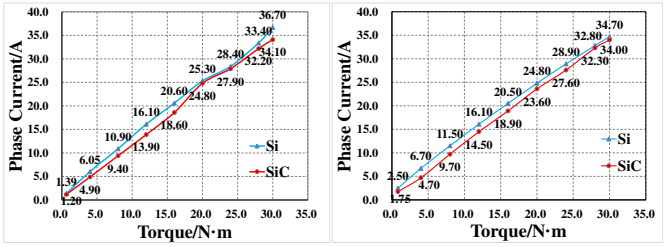


Fig. 22. Comparison of phase current amplitude between Si-drive and SiC-drive systems. (a) The amplitudes of phase current under 200rpm of the motor. (b) The amplitudes of phase current under 800rpm of the motor.

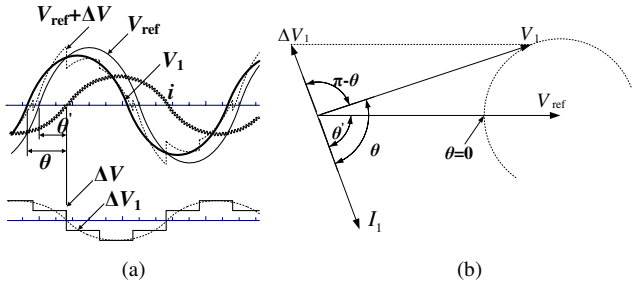


Fig. 23. The distortion voltage and its impact on current. (a) Representation of waveforms of the voltage and current. (b) Representation of phasor diagram.

As the current distortion of the SiC-inverter is smaller than that of the Si-inverter, the amplitudes of the phase currents in SiC-inverter are also smaller under same output power condition as shown in Fig. 22. Such an interesting phenomenon would also be a conclusion as the effect results of the distortion voltage. In Fig. 23, the deviation appears in the waveform of the inverter output voltage. V_{ref} represents the ideal fundamental output voltage of the inverter that would result if there were no distortion voltage effects. As the motor is an inductive load, the current waveform i lags behind V_{ref} by an angle θ'. Since the distortion voltage increases (decreases) the inverter output voltage for the negative (positive) half cycle of the current shown in Section II, the average voltage distortion over an entire cycle could be represented by the square wave in Fig. 23(a).

The average voltage distortion is the superposition of ΔV on the ideal voltage V_{ref} shown as broken line in Fig. 23(a). Therefore, the fundamental output voltage with distortion voltage V_1 is the sum of V_{ref} and ΔV_1, which is described as a heavy solid curve. When the harmonic components of the current are ignored, the phase displacement between V_1 and i corresponds to the fundamental power factor angle of the load. It can be seen that the real fundamental output voltage differs from the reference one in both the phase and magnitude. These relationships are also described by a phasor diagram shown in Fig. 23(b). Therefore, when the fundamental output voltage reduces and power factor angle increases, the current should increase to maintain a constant output power as shown in Fig. 22.

C. Effect of inverter nonlinearities on efficiency

Table IV shows the comprehensive comparisons of Si and SiC based drive system. The amplitude of phase voltage for Si based system is smaller than the value of SiC based system,

TABLE IV
Measured Efficiency For Si and SiC Based Drive Systems

Speed /rpm	Load torque /N · m	Phase voltage/V		Phase current/A		Inverter efficiency/%		Motor efficiency/%		System efficiency/%	
		SiC	Si	SiC	Si	SiC	Si	SiC	Si	SiC	Si
200	1	15.4	13.5	1.2	1.4	18.2	4.8	96.4	19.2	17.6	0.9
400	4	29.9	28.5	4.9	6.1	71.2	67.8	92.0	71.1	65.5	58.4
	4	51.3	50.1	4.7	6.7	84.9	83.3	93.7	72.2	79.5	60.1
	8	51.6	50.6	9.7	11.5	92.5	87.7	90.8	79.4	84.0	69.6
	12	54.0	53.6	14.5	16.1	95.0	91.0	88.2	80.5	83.7	73.2
800	16	56.8	55.8	18.9	20.5	96.2	92.5	86.4	80.9	83.1	74.9
	20	59.8	57.9	23.6	24.8	97.1	92.7	84.7	81.1	82.3	75.2
	24	62.5	60.0	27.6	28.9	97.4	93.7	83.2	80.3	81.0	75.2
	28	64.8	62.0	32.3	32.8	97.0	93.6	81.9	79.6	79.4	74.5

while the amplitude of phase current for Si based system is bigger than the counterpart of SiC based system. It is obvious that the distorted voltage will reduce the amplitude of the phase voltage shown in Fig. 23. In addition, the distorted voltage of Si is more than that of SiC. Therefore, compared with SiC based system, the amplitude of the phase voltage for Si based system is smaller. In order to achieve the same output power with SiC system, the phase current of Si-system should increase to compensate for the more loss of the phase voltage and power factor.

Due to the quicker switching and lower voltage drop of SiC compared with Si, the inverter based on SiC has higher efficiency than Si based inverter, as shown in Table IV. Meanwhile, the efficiency of the motor driven by SiC based inverter is also higher than the motor driven by Si based system.

This efficiency advantage of SiC based system is a result of the smaller amplitude of phase current and the lower harmonic components in the phase current. It is known that the motor losses, such as copper and iron losses, directly depend on the phase current. In addition, the motor driven by SiC based inverter demonstrates extremely high efficiency when it operates at low power ratings as shown in Table IV and Fig. 24. It is due to the fact that the inverter nonlinearity effect is more significant for small fundamental phase current of inverter. Meanwhile, the estimated results for the proposed model are validated by the experimental results shown in Fig. 24 (d).

V. Conclusion

This paper offers a detailed and systematic investigation of the nonlinearities of inverters based on SiC MOSFETs and Si IGBTs for PMSM traction drives used in electric vehicles. A novel comprehensive model of voltage distortion in the inverters is proposed and validated by experimentation. This has been made possible as actual switching performances of the SiC and Si PMSM drive systems have been measured rather than resorting to the conventional DPT test, which would not have captured essential switching characteristics of the power devices exhibited in these drive applications. Compared with Si-IGBTs based inverter, the voltage distortion of the inverter based on SiC-MOSFETs is smaller due to higher switching speed, lower on-resistance and smaller output capacitance. The overall results show comprehensively the overriding efficiency and other operational advantages of SiC-based inverters over Si-based ones, which appear even more prominent at light loads. It is clear that the SiC technology presents a significant advantage in the use of inverters for the electric vehicle industry.

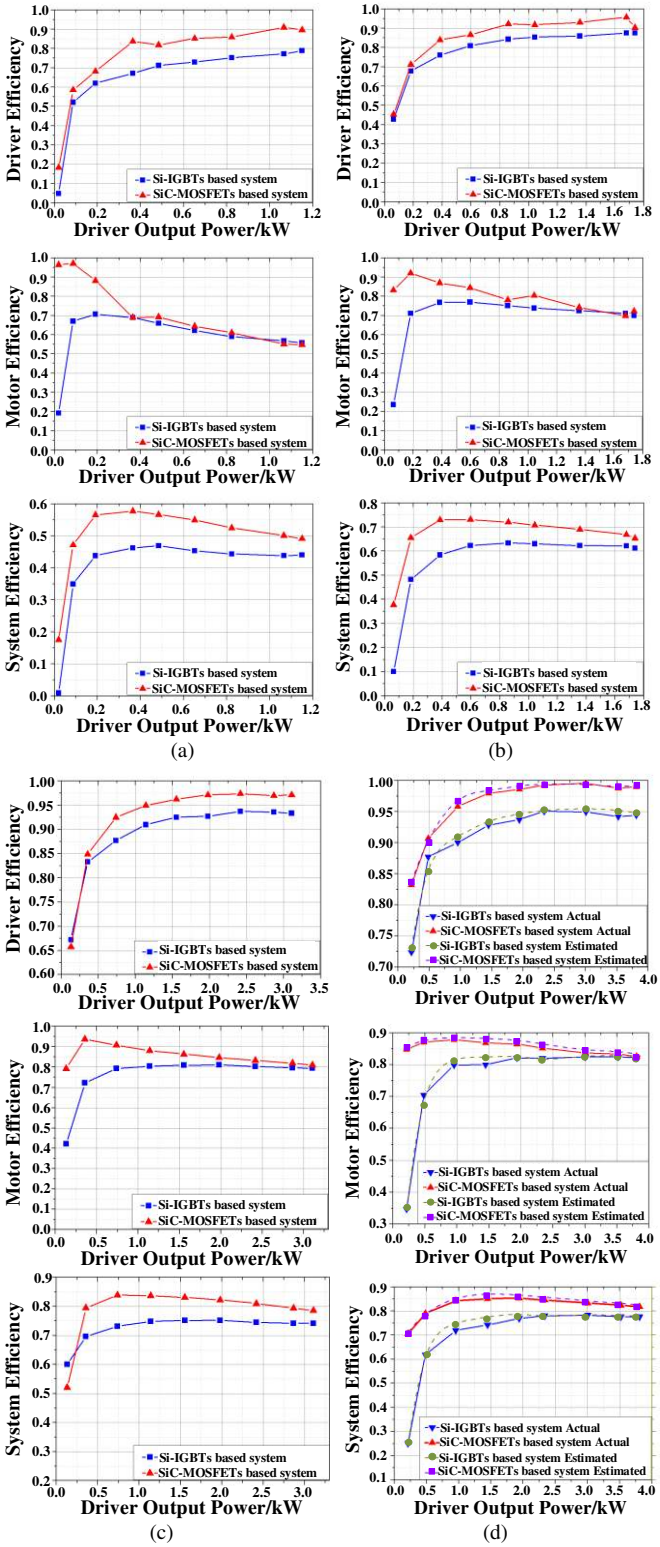


Fig. 24. Efficiency comparison of Si and SiC based drive systems under different speeds. (a) 200rpm; (b) 400rpm; (c) 800rpm; (d) 1000rpm.

Future work will include further development of the validated analytical model of voltage distortion by taking into account other effects such as the reflected wave phenomenon and temperature. This will lead to a more precise and general-purpose model of voltage distortion so that the full potential of the wide-bandgap technology in traction drives can be fully appreciated.

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REFERENCES

[1] P. Shamsi, M.McDonough and B. Fahimi, Wide-Bandgap Semiconductor Technology: Its impact on the electrification of the transportation industry., in IEEE Electrification Magazine, vol. 1, no. 2, pp. 59-63, Dec. 2013.

[2] K. Hamada, M. Nagao, M. Ajioka and F. Kawai, SiC—Emerging Power Device Technology for Next-Generation Electrically Powered Environmentally Friendly Vehicles, in IEEE Transactions on Electron Devices, vol. 62, no. 2, pp. 278-285, Feb. 2015.

[3] R. Xiong, F Sun.and Z. Chen, A data-driven multi-scale extended Kalman filtering based parameter and state estimation approach of lithium-ion polymer battery in electric vehicles. Applied Energy, 2014, 113:463–476.

[4] J. Ruan, P. Walker andN. Zhang, A comparative study energy consumption and costs of battery electric vehicle transmissions, Applied Energy, 2016; 165(Mar.): 119-134.

[5] F. Sun andR. Xiong, A novel dual-scale cell state-of-charge estimation approach for series-connected battery pack used in electric vehicles. J. Power Sources, 2015, 274, 582–594.

[6] J. Jaguemont, L. Boulon andY. Dubé, A comprehensive review of lithium-ion batteries used in hybrid and electric vehicles at cold temperatures, Applied Energy, 2016;164(Feb.), 99-114

[7] F. Sun, R. Xiong and H. He, A systematic state-of-charge estimation framework for multi-cell battery pack in electric vehicles using bias correction technique, Applied Energy, 2016; 162 (Jan.), 1399-1409.

[8] D. Pohlenz and J. Böcker, Efficiency improvement of an IPMSM using Maximum Efficiency operating strategy, Power Electronics and Motion Control Conference (EPE/PEMC), 2010 14th International, Ohrid, 2010, pp. 15-19.

[9] F. Shang, A. P. Arribas and M. Krishnamurthy, A comprehensive evaluation of SiC devices in traction applications, Transportation Electrification Conference and Expo (ITEC), 2014 IEEE, Dearborn, MI, 2014, pp. 1-5.

[10] H. Zhang, L. M. Tolbert and B. Ozpineci, Impact of SiC Devices on Hybrid Electric and Plug-In Hybrid Electric Vehicles, in IEEE Transactions on Industry Applications, vol. 47, no. 2, pp. 912-921, March-April 2011.

[11] S. Jahdi, O. Alatise, C. Fisher, Li Ran and P. Mawby, An Evaluation of Silicon Carbide Unipolar Technologies for Electric Vehicle Drive-Trains, in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 3, pp. 517-528, Sept. 2014

[12] J. G. Kassakian and T. M. Jahns, Evolving and Emerging Applications of Power Electronics in Systems, in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 1, no. 2, pp. 47-58, June 2013.

[13] F. Wang, Z. Zhang, T. Ericsen, R. Raju, R. Burgos and D. Boroyevich, Advances in Power Conversion and Drives for Shipboard Systems, in Proceedings of the IEEE, vol. 103, no. 12, pp. 2285-2311, Dec. 2015.

[14] S. Tanimoto and K. Matsui, High Junction Temperature and Low Parasitic Inductance Power Module Technology for Compact Power Conversion Systems, in IEEE Transactions on Electron Devices, vol. 62, no. 2, pp. 258-269, Feb. 2015.

[15] F. Xu, B. Guo, Z. Xu, L. M. Tolbert, F. Wang and B. J. Blalock, Paralleled Three-Phase Current-Source Rectifiers for High-Efficiency Power Supply Applications, in IEEE Transactions on Industry Applications, vol. 51, no. 3, pp. 2388-2397, May-June 2015.

[16] I. Josifović, J. Popović-Gerber and J. A. Ferreira, Improving SiC JFET Switching Behavior Under Influence of Circuit Parasitics, in IEEE Transactions on Power Electronics, vol. 27, no. 8, pp. 3843-3854, Aug. 2012.

[17] K. Sun, H. Wu, J. Lu, Y. Xing and L. Huang, Improved Modeling of Medium Voltage SiC MOSFET Within Wide Temperature Range, in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2229-2237, May 2014.

[18] C. D. Brown and B. Sarlioglu, Reducing Switching Losses in BLDC Motor Drives by Reducing Body Diode Conduction of MOSFETs, in IEEE Transactions on Industry Applications, vol. 51, no. 2, pp. 1864-1871, March-April 2015.

[19] M. M. Swamy, Jun-Koo Kang and K. Shirabe, Power Loss, System Efficiency, and Leakage Current Comparison Between Si IGBT VFD and SiC FET VFD With Various Filtering Options, in IEEE Transactions on Industry Applications, vol. 51, no. 5, pp. 3858-3866, Sept.-Oct. 2015.

[20] K. Shirabe, M. Swamy, J. K. Kang and M. Hisatsune, Design of 400V class inverter drive using SiC 6-in-1 power module, Energy Conversion Congress and Exposition (ECCE), 2013 IEEE, Denver, CO, 2013, pp. 2363-2370.

[21] A. Merkert, T. Krone and A. Mertens, Characterization and Scalable Modeling of Power Semiconductors for Optimized Design of Traction Inverters with Si- and SiC-Devices, in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2238-2245, May 2014.

[22] T. Zhao, J. Wang, A. Q. Huang and A. Agarwal, Comparisons of SiC MOSFET and Si IGBT Based Motor Drive Systems, Industry Applications Conference, 2007. 42nd IAS Annual Meeting. Conference Record of the 2007 IEEE, New Orleans, LA, 2007, pp. 331-335.

[23] J. K. Reed, J. McFarland, J. Tangudu, E. Vinot, R. Trigui, G. Venkataramanan, S. Gupta, T. Jahns, Modeling power semiconductor losses in HEV powertrains using Si and SiC devices, Vehicle Power and Propulsion Conference (VPPC), 2010 IEEE, Lille, 2010, pp. 1-6.

[24] Hyun-Soo Kim, Hag-Wone Kim and Myung-Joong Youn, A new on-line dead-time compensation method based on time delay control, Industrial Electronics Society, 2001. IECON '01. The 27th Annual Conference of the IEEE, Denver, CO, 2001, pp. 1184-1189 vol.2.

[25] Jong-Woo Choi and Seung-Ki Sul, Inverter output voltage synthesis using novel dead time compensation, in IEEE Transactions on Power Electronics, vol. 11, no. 2, pp. 221-227, Mar 1996.

[26] J. M. Guerrero, M. Leetmaa, F. Briz, A. Zamarron and R. D. Lorenz, Inverter nonlinearity effects in high-frequency signal-injection-based sensorless control methods, in IEEE Transactions on Industry Applications, vol. 41, no. 2, pp. 618-626, March-April 2005.

[27] Y. Wang, Q. Gao and X. Cai, Mixed PWM for Dead-Time Elimination and Compensation in a Grid-Tied Inverter, in IEEE Transactions on Industrial Electronics, vol. 58, no. 10, pp. 4797-4803, Oct. 2011.

[28] N. Bedetti, S. Calligaro and R. Petrella, Self-Commissioning of Inverter Dead-Time Compensation by Multiple Linear Regression Based on a Physical Model, in IEEE Transactions on Industry Applications, vol. 51, no. 5, pp. 3954-3964, Sept.-Oct. 2015.

[29] S. H. Hwang and J. M. Kim, Dead Time Compensation Method for Voltage-Fed PWM Inverter, in IEEE Transactions on Energy Conversion, vol. 25, no. 1, pp. 1-10, March 2010.

[30] Z. Zhang and L. Xu, Dead-Time Compensation of Inverters Considering Snubber and Parasitic Capacitance, in IEEE Transactions on Power Electronics, vol. 29, no. 6, pp. 3179-3187, June 2014.

[31] R. B. Sepe and J. H. Lang, Inverter nonlinearities and discrete-time vector current control, in IEEE Transactions on Industry Applications, vol. 30, no. 1, pp. 62-70, Jan/Feb 1994.

[32] Z. Zhang, B. Guo, Z. Zhang, W. Zhang, F. Wang,L. M. Tolbert, B. J. Blalock, Z. Liang, and P. Ning, Methodology for switching characterization evaluation of wide band-gap devices in a phase-leg configuration, in Proc. IEEE Applied Power Electronics Conference and Exposition, March 2013, pp. 2534-2541.

[33] C. Zhen, Characterization and modeling of high-switching-speed behavior of SiC active devices, M.S thesis, Dept. Electrical Engineering. Eng., Virginia Polytechnic Institute and State Univ., Blacksburg, USA, 2009.

https://vtechworks.lib.vt.edu/bitstream/handle/10919/30778/Chen_Z_T_2009.pdf?sequence=1
[34] J. B. Witcher, Methodology for switching characterization of power devices and modules, M.S thesis, Dept. Electrical Engineering. Eng., Virginia Polytechnic Institute and State Univ., Blacksburg, USA, 2003. https://vtechworks.lib.vt.edu/bitstream/handle/10919/31205/thesis.pdf?sequence=1&isAllowed=y
[35] C. J. Cass, Y. Wang, R. Burgos, T. P. Chow, F. Wang and D. Boroyevich, Evaluation of SiC JFETs for a Three-Phase Current-Source Rectifier with High Switching Frequency, Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE, Anaheim, CA, USA, 2007, pp. 345-351.
[36] I. Josifović, J. Popović-Gerber and J. A. Ferreira, Improving SiC JFET Switching Behavior Under Influence of Circuit Parasitics, in IEEE Transactions on Power Electronics, vol. 27, no. 8, pp. 3843-3854, Aug. 2012.
[37] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock and D. J. Costinett, Evaluation of Switching Performance of SiC Devices in PWM Inverter-Fed Induction Motor Drives, in IEEE Transactions on Power Electronics, vol. 30, no. 10, pp. 5701-5711, Oct. 2015.
[38] http://pdf1.alldatasheetcn.com/datasheet-pdf/view/588672/CREE/CAS300M12BM2.html
[39] http://pdf1.alldatasheetcn.com/datasheet-pdf/view/396515/INFINEON/FF600R12IP4.html
[40] T Liu, R Ning, T. T. Y. Wong, and Z. J. Shen. Modeling and Analysis of SiC MOSFET Switching Oscillations. IEEE Journal of Emerging & Selected Topics in Power Electronics, vol. 4, no. 3, pp. 747-756, 2016.
[41] M. J. Scott, J. Brockman, B. Hu, L. Fu, L. Xu, J. Wang and R. D. Zamora, Reflected wave phenomenon in motor drive systems using wide bandgap devices, 2014 IEEE Workshop on Wide Bandgap Power Devices and Applications, Knoxville, TN, pp. 164-168, 2014.

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