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Analytical and Experimental Investigation of Neutral Point Clamped Quasi-Impedance-Source Inverter

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***Abstract* – In this paper a new modification of a three-level neutral-point-clamped inverter is presented. The proposed topology combines the advantages of the three-level neutral-point-clamped full-bridge inverter with those of the quasi-impedance-source inverter. The neutral-point-clamped quasi-impedance-source inverter is especially suitable for renewable energy sources.**

The steady-state analysis of a neutral-point-clamped quasi-impedance-source inverter in the continuous conduction mode is presented. The presented models as well as deduced equations are verified by an experimental prototype.

***Keywords* – Three-level neutral-point-clamped inverter, quasi-impedance source inverter.**

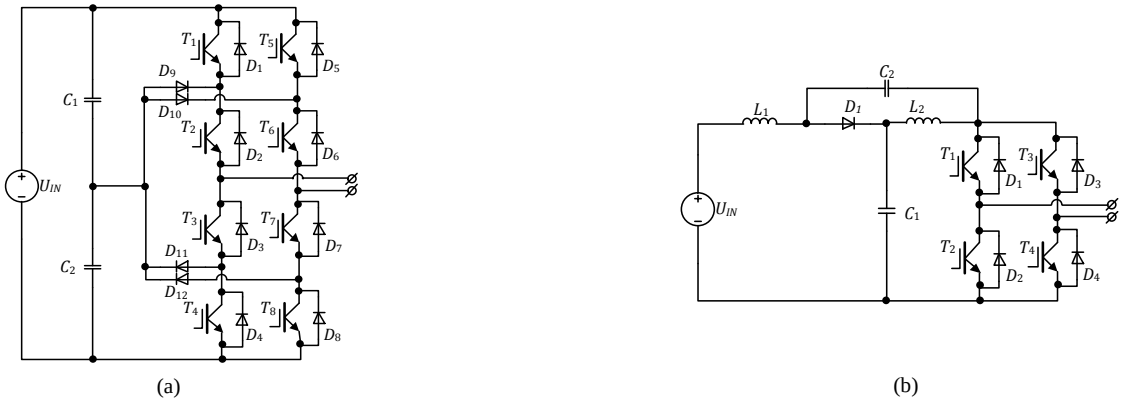
I. Introduction

A three-level neutral-point-clamped full-bridge (NPCFB) inverter (Fig. 1*a*) has many advantages over a two-level voltage source inverter, such as lower semiconductor voltage stress, lower required blocking voltage capability, decreased *dv/dt*, better harmonic performance, soft switching possibilities without additional components, higher switching frequency due to lower switching losses and balanced neutral-point voltage. As a drawback, it has two additional clamping diodes per phase-leg and more controlled semiconductor switches per phase-leg than the two-level voltage source inverter. The three-level NPCFB can normally perform only the voltage buck operation. In order to ensure voltage boost operation an additional DC/DC boost converter should be used in the input stage [1-2].

To obtain buck and boost performance the focus is on a quasi-impedance-source (qZS) inverter (Fig. 1*b*). The qZS inverter was first introduced in [3]. The qZS inverter consists of two inductors (L_1, L_2), two capacitors (C_1, C_2), a diode (D_1) and a full-bridge (T_1, T_2, T_3, T_4), as shown in Fig. 1*b*. The qZS inverter can buck and boost DC-link voltage in a single stage without additional switches.

The qZS inverter can boost the input voltage by introducing a special shoot-through switching state, which is the simultaneous conduction (cross conduction) of both switches of the same phase leg of the inverter. This switching state is forbidden for traditional voltage source inverters because it causes a short circuit of the DC-link capacitors. Thus, the qZS inverter has excellent immunity against the cross conduction of top and bottom-side inverter switches. The possibility of using shoot-through eliminates the need for dead-times without having the risk of damaging the inverter circuit. The input voltage is regulated only by adjusting the shoot-through duty cycle. In addition, the qZS inverter has a continuous mode input current (input current never drops to zero), which makes it especially suitable for renewable energy sources (e.g. fuel cells, solar energy, wind energy etc.). The main drawback of the qZS inverter is its poor performance in the case of small loads and relatively low switching frequency. In these conditions the qZS inverter starts to work in the discontinuous conduction mode, which causes an over-boost effect and leads to instabilities [3-7].

In this paper a new inverter topology is proposed: a three-level neutral-point-clamped (NPC) qZS inverter Fig. 2). The proposed inverter combines the advantages of the two topologies described above. The static models of the proposed topology in the case of the continuous conduction mode will be analyzed and verified.



(a) (b)

Fig. 1. Three-level neutral-point-clamped full-bridge inverter (a), quasi-impedance-source inverter (b).

II. NEUTRAL-POINT-CLAMPED QZS INVERTER

Fig. 2 illustrates the proposed topology of a single-phase three-level NPC qZS inverter. Each leg of the three-level NPC qZS inverter consists of two complementary switching pairs and four anti-parallel diodes. As an advantage, this topology has continuous input current, the possibility to use shoot-through, lower switching losses and balanced neutral-point voltage in comparison with the traditional two-level voltage source inverter.

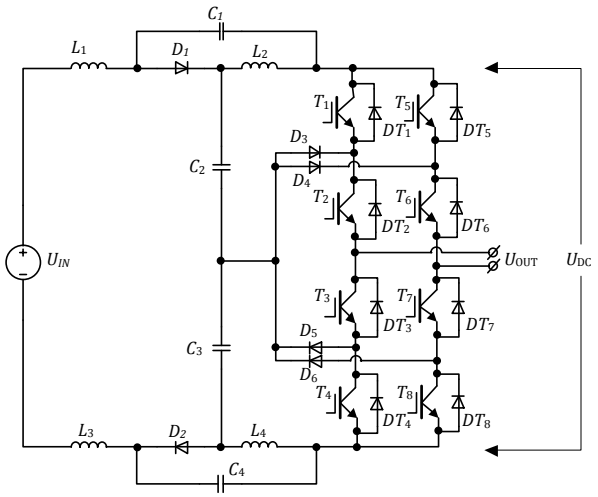


Fig. 2. Three-level NPC quasi-impedance-source inverter.

Pulse width modulation with simple boost control has been used, as shown in Fig. 3.

Fig. 3 shows inverter switching states during one period. Shoot-through is generated during zero states. The zero and shoot-through states are spread over the switching period, so the number of higher harmonics can be reduced. In order to reduce the switching losses of the transistors, the number of shoot-through states per period was limited by two. Moreover, in order to decrease the conduction losses of the transistors, the shoot-through current is distributed between both inverter legs, i.e. all switches conducting. As can be seen in Table I, the operating frequencies, thus switching losses of transistors are different. The switching frequency of T_1, T_4, T_5 and T_8 is three times higher and the switching frequency of T_2, T_3, T_6 and T_7, is twice higher than the frequency of the output voltage.

The inverter output voltage has three different levels: 0, $B\cdot(U_{IN}/2)$ and $B\cdot U_{IN}$ in the positive and negative directions, where B is the inverter boost factor.

Four reference signals (REF1, REF2, REF3 and REF4) and two compare values (CMPR1 and CMPR2) are used to generate pulse width control signals for the switches (T1…T8), as shown in Fig. 3. The shoot-through vector is generated separately using reference signal REF5 and two compare values, Vp and Vn. Finally, the shoot-though vector is mixed together with other control signals using OR-gates.

TABLE I.

INVERTER SWITCHING STATES DURING ONE PERIOD

	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8
Zero-state	0	1	0	0	0	0	1	0
Shoot-through	1	1	1	1	1	1	1	1
Zero-state	0	1	0	0	0	0	1	0
Active state	1	1	0	0	0	0	1	0
Active state	1	1	0	0	0	0	1	1
Active state	0	1	0	0	0	0	1	1
Zero-state	0	0	1	0	0	1	0	0
Shoot-through	1	1	1	1	1	1	1	1
Zero-state	0	0	1	0	0	1	0	0
Active state	0	0	1	0	1	1	0	0
Active state	0	0	1	1	1	1	0	0
Active state	0	0	1	1	0	1	0	0

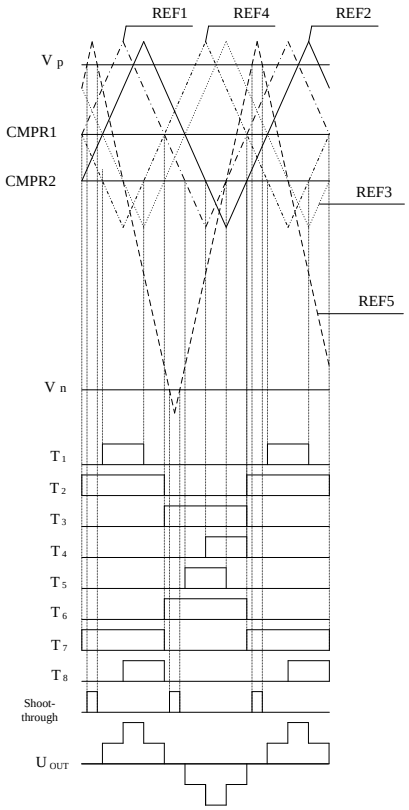
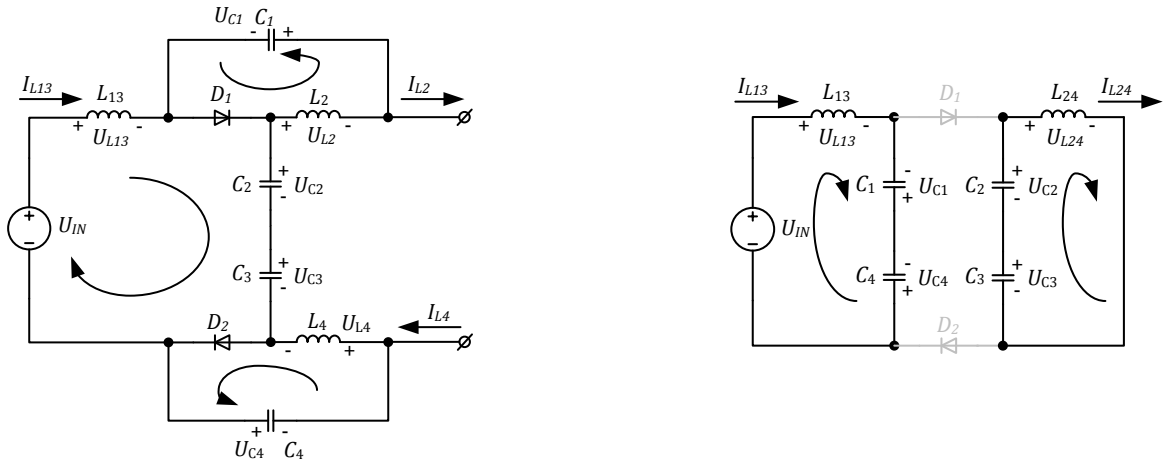


Fig. 3. Sketch of pulse width modulation with simple boost control (D_S = 0.25)

III. STEADY-STATE ANALYSIS OF A THREE-LEVEL NPC QZS INVERTER

In general, the operating period of the three-level NPC qZS inverter in the continuous conduction mode may be divided into two states: non-shoot-through (t_N) and shoot-through state (t_S):

$$T = t_N + t_S. \quad (1)$$



(a) (b)

Fig. 4. Equivalent circuit of a three-level NPC qZS inverter during the non-shoot-through state (a) and the shoot-through state (b).

Equation (1) could be represented in the form:

$$\frac{t_N}{T}+\frac{t_S}{T}=D_N+D_S=1, \tag{2}$$

where D_N is the duty cycle of non-shoot-through and D_S is the shoot-through duty cycle. The equivalent schemes of the qZS inverter during the shoot-through and non-shoot-through modes are presented in Fig. 4.

Input capacitors and inductors are identical, thus:

$$L_1=L_2, \qquad L_2=L_4; \tag{3}$$

$$C_1=C_4, \qquad C_2=C_3; \tag{4}$$

Considering that during the non-shoot-through state inductors L_1 and L_3 are connected in a series, they can be replaced by an equivalent inductor, L_{13}. From Fig. 4*a* inductor voltages during the non-shoot-through mode can be found as follows:

$$u_{L2}=-U_{C1}; \tag{5}$$

$$u_{L4}=-U_{C4}; \tag{6}$$

$$u_{L13}=U_{IN}-U_{C2}-U_{C3}, \tag{7}$$

where u_{L13} is the voltage of the equivalent inductance, L_{13}. Inductor voltages u_{L1} and u_{L3} can be found as:

$$u_{L1}=u_{L3}=\frac{u_{L13}}{2}. \tag{8}$$

On the basis of an equivalent circuit of a three-level NPC qZS inverter during the shoot-through state (Fig. 4*b*), the inductor voltages could be presented as:

$$u_{L13}=U_{IN}+U_{C1}+U_{C4}; \tag{9}$$

$$u_{L24}=U_{C2}+U_{C3}, \tag{10}$$

where u_{L24} is the voltage of the equivalent inductance, L_{24}. Inductor voltages u_{L2} and u_{L4} can be found as:

$$u_{L2}=u_{L4}=\frac{u_{L24}}{2}. \tag{11}$$

In the steady state the average voltage of the inductor over one switching period is zero. Thus, from (5) to (11) we can obtain:

$$\begin{cases} U_{L1}=D_S\cdot\left(\frac{U_{IN}+U_{C1}+U_{C4}}{2}\right)+(1-D_S)\cdot\left(\frac{U_{IN}-U_{C2}-U_{C3}}{2}\right) \\ U_{L2}=D_S\cdot\left(\frac{U_{C2}+U_{C3}}{2}\right)+(1-D_S)\cdot(-U_{C1})=0 \\ U_{L3}=D_S\cdot\left(\frac{U_{IN}+U_{C1}+U_{C4}}{2}\right)+(1-D_S)\cdot\left(\frac{U_{IN}-U_{C2}-U_{C3}}{2}\right)=0 \\ U_{L4}=D_S\cdot\left(\frac{U_{C2}+U_{C3}}{2}\right)+(1-D_S)\cdot(-U_{C4})=0 \end{cases} \tag{12}$$

By solving the equation system (12) the voltages across capacitors can be found:

$$U_{C1}=U_{C4}=\frac{D_S\cdot U_{IN}}{2-4\cdot D_S}; \tag{13}$$

$$U_{C2}=U_{C3}=\frac{U_{IN}\cdot(D_S-1)}{4\cdot D_S-2}. \tag{14}$$

The peak DC-link voltage U_{DC_p} is the sum of all capacitor voltages:

$$U_{DC\_p} = U_{C1} + U_{C2} + U_{C3} + U_{C4} = \frac{U_{IN}}{1 - 2 \cdot D_S}. \quad (15)$$

The boost factor (B) of the three-level NPC qZS inverter equals:

$$B = \frac{U_{DC\_p}}{U_{IN}} = \frac{1}{1 - 2 \cdot D_S}. \quad (16)$$

The boost factor of the three-level NPC qZS inverter is as high as that of the traditional qZS inverter.

Fig. 5 shows the dependence between the boost factor and the shoot-through duty cycle.

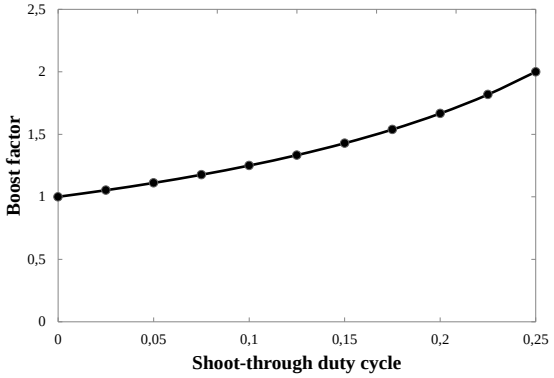


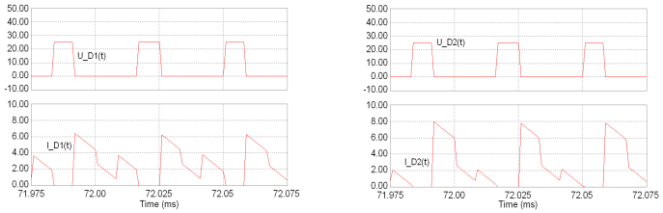
Fig. 5. Dependence between the boost factor and the shoot-through duty cycle.

IV. Simulation and Experimental Results

To verify the mathematical analysis a model in the PSIM simulation software as well as a prototype of the three-level NPC qZSI were developed.

First, a general analysis of simulation results with the shoot-through duty cycle D_S=0.25 was carried out. Then some simulation and experimental results of the most critical parameters of the converter were analyzed in three operating points: D_S = 0, D_S = 0.1 and D_S = 0.25.

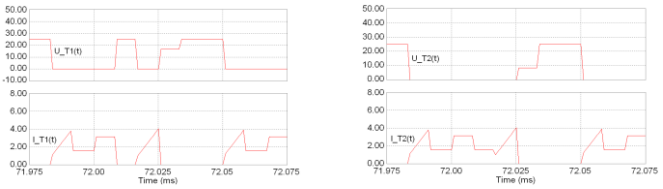
Fig. 6 presents operating current and voltage waveforms of qZS diodes D_1 and D_2. As the diodes are loaded similarly, it is possible to use two diodes in single housing.



(a) (b)

Fig. 6. Operating voltage- and -current waveforms of D_1 (a) and D_2 (b).

The collector-emitter currents and voltages of switches T_1 and T_2 are presented in Fig. 7. The collector-emitter voltages of switches illustrate clearly the different switching frequency of the switches as well as the presence of the shoot-through vector.



(a) (b)

Fig. 7. Collector-emitter voltage and current waveforms across the switches T_1 (a) and T_2 (b).

By incrementing the length of the shoot-through vector, the amplitude value of the output voltage will be boosted, but the voltage shape remains. Fig. 8 shows the output voltage and current of a single-phase three-level NPC qZS inverter when D_S=0.25.

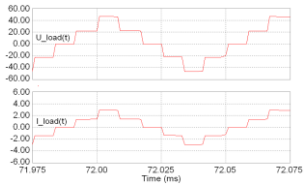
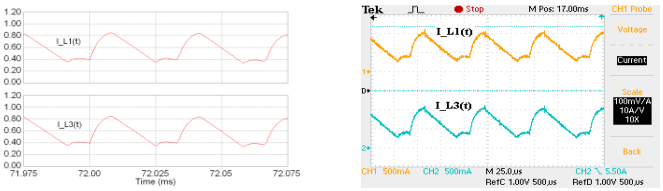


Fig. 8. Output voltage and current of a single-phase three-level NPC qZS inverter.

A. *Operation with no shoot-through: D_S = 0*

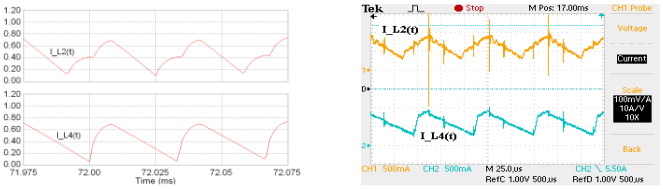
Fig. 9 presents the simulated and measured current waveforms of inductors L_1 and L_3. Simulated and measured waveform shapes are identical and in the continuous conduction mode, as desired. However, the operating period of the three-level NPC qZS inverter in the continuous conduction mode consists of four states. In the steady state analysis (1) just two states were assumed. Therefore the derived mathematical models cannot be applied in the current situation.



(a) (b)

Fig. 9. Simulated (a) and measured current waveforms of inductors L_1 and L_3 (b), D_S = 0.

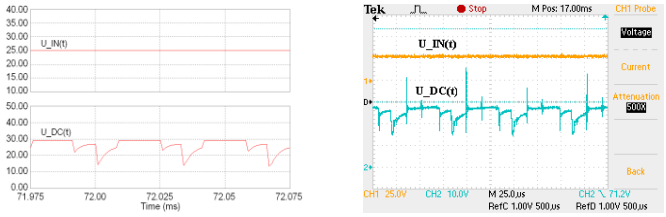
Fig. 10 presents the simulated and measured current waveforms of inductors L_2 and L_4. The simulated and measured waveform shapes are identical and in the continuous conduction mode. However, the inductor currents are not equal to each other, as predicted by the steady state analysis.



(a) (b)

Fig. 10. Simulated (a) and measured (b) current waveforms of inductors L_2 and L_4, D_S = 0.

Fig. 11 illustrates the waveforms of the input and the DC-link voltage. The simulated and measured waveform shapes are identical. However, some abnormal behavior of the three-level NPC qZS inverter can be seen. The steady state analysis predicted straight DC-link voltage without boost and higher harmonics. In the current case the DC-link voltage is disturbed and also shows a small boost.

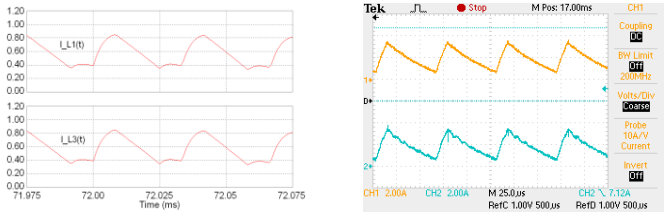


(a) (b)

Fig. 11. Simulated (a) and measured waveforms of the input and the DC-link voltage of a single-phase thee-level NPC qZSI (b), $D_S = 0$.

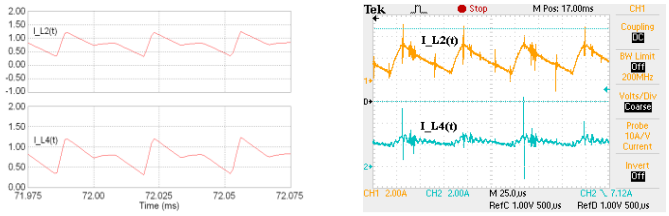
B. Operation with shoot-through: $D_S = 0.1$

In Fig. 12 and 14 simulated and measured current waveforms of inductors L_1, L_3 L_2 and L_4 are shown. The simulated and measured waveform shapes are in the continuous conduction mode. Simulation and experimental results are different, as shown in Figs. 13 and 14. Experimental results correspond to the steady state analysis while simulations predict some abnormal behavior of the converter. The difference is caused by the semiconductor losses that were not taken into account in the simulation.



(a) (b)

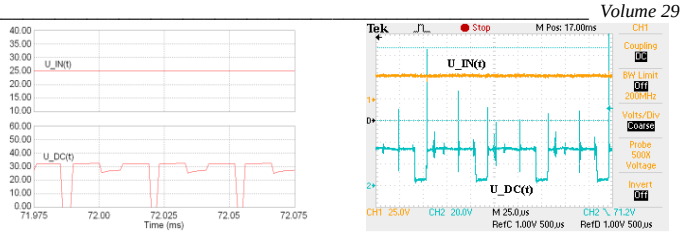
Fig. 12. Simulated-(a) and measured current waveforms of inductors L_1 and L_3 (b), $D_S = 0.1$.



(a) (b)

Fig. 13. Simulated (a) and measured current waveforms of inductors L_2 and L_4 (b), $D_S = 0.1$.

Fig. 14 illustrates the waveforms of the input and the DC-link voltage. The simulated and measured waveform shapes are similar. The amplitude value of the DC-link voltage U_{DC} is boosted up to 32 V, which is as expected.

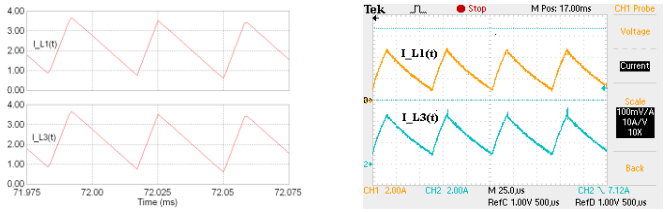


(a) (b)

Fig. 14. Simulated (a) and measured waveforms of the input- and the DC-link voltage of a single-phase thee-level NPC qZSI (b), $D_S = 0.1$.

C. Operation with shoot-through: $D_S = 0.25$

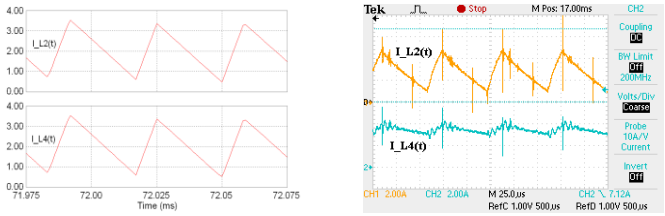
In Fig. 15 simulated and measured current waveforms of inductors L_1 and L_3 are shown. The simulated and measured waveform shapes are identical in the continuous conduction mode and correspond to the steady state analysis.



(a) (b)

Fig. 15. Simulated (a) and measured current waveforms of inductors L_1 and L_3 (b), $D_S = 0.25$.

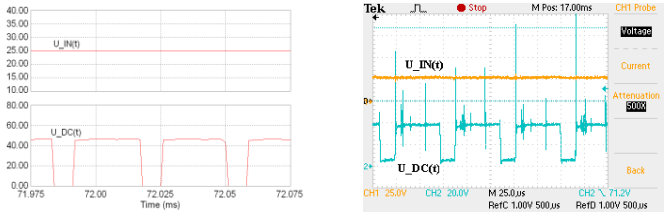
In Fig. 11 simulated and measured current waveforms of inductors L_2 and L_4 are shown. Measured values differ from simulation results. The current ripple of L_4 is twice lower than expected. This effect is caused by the unbalance of the input capacitor.



(a) (b)

Fig. 16. Simulated (a) and measured current waveforms of inductors L_2 and L_4 (b), $D_S = 0.25$.

Fig. 17 illustrates the waveforms of the input and the DC-link voltage. The simulated and measured waveform shapes are identical. The amplitude value of the DC-link voltage U_{DC} is boosted up to 40 V, which is 10 V less than expected. The voltage drop is mainly caused by the losses in semiconductors.



(a) (b)

Fig. 17. Simulated (a) and measured waveforms of the input- and the DC-link voltage of a single-phase thee-level NPC qZSI (b), $D_S = 0.25$.

V. GENERALIZATIONS

Simulations and experiments revealed some abnormal behavior of the proposed converter in the case of small shoot-through duty cycles. The steady state analysis carried out in this paper assumed that the operating period can be divided into two parts: shoot-through and non shoot-through. However, simulations showed that in the case of small shoot-through duty cycles the operating period has four states. Thus, in this operating mode a different steady state analysis has to be carried out. It was also found that the boundary condition between those two operating modes is as follows:

$$I_L > \frac{U_{DC\_p}}{2 \cdot R_{load}}, \qquad (17)$$

where I_L is the inductor current. According to (17), if the inductor current decreases below the boundary value, two additional states occur inside the operating period and mathematical models derived in this paper can not be used in that situation.

CONCLUSION

The NPC qZS inverter is a combination of the quasi-impedance-source inverter and the three-level NPC full-bridge. The three-level NPC qZS comprises advantages from both topologies: it can buck and boost the input voltage, it has excellent short circuit immunity, due to the multilevel topology high energy density is achievable, etc. The steady-state analysis in the case of the continuous conduction mode was carried out and the equation of the boost factor was derived.

The NPC qZS inverter operates similarly to the qZSI in the case of large shoot-through duty-cycles or high loads. If the inductor currents are below the boundary condition (17), new mathematical models should be derived to describe the converter working states. Focus in the future work will be on the NPC qZS inverter under the named conditions.

ACKNOWLEDGEMENT

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