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Keywords

radiation hard CMOS, noise measurement.

Disciplines

Electrical and Computer Engineering

Comments

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Analytical and Experimental Studies of Thermal Noise in MOSFET's

Suharli Tedja, *Student Member, IEEE,* Jan Van der Spiegel, *Senior Member, IEEE,* and Hugh H. Williams

***Abstract*—An analysis of the channel thermal noise in MOSFET's, based on the one-dimensional charge sheet model, is presented. The analytical expression is valid in the strong, moderate, and weak inversion regions. The body effect on the device parameters relevant to the thermal noise is discussed. A measurement technique as well as experimental results of P- and N-MOSFET's of a 1.2 μm radiation hard CMOS process are presented. The calculated channel thermal noise coefficient γ as in $i_d^2/\Delta f = 4kT\gamma g_{do}$ agrees well with experimental data for effective device channel length as short as 1.7 μm.**

I. Introduction

Analog CMOS integrated circuits have gained considerable importance over the last 10 years. The ever-decreasing dimensions of the transistors have often made CMOS a technology of choice for low power, low noise, and moderately high speed applications. The optimum operating region to minimize noise and power is often moderate inversion, at least for the input transistor which generally dominates the noise [1]. Studies of thermal noise in MOSFET's have mainly been limited to the two cases of strong and weak inversion [2]–[9]. To the best of our knowledge, few results have been reported on the noise behavior of transistors in the moderate inversion region [1].

The objective of this work is to study, both analytically and experimentally, the MOSFET channel thermal noise in saturation for all three regions of inversion. The analytical study shows that under thermal equilibrium, the noise expression can be obtained either from drift or diffusion carrier transport mechanisms. Noise measurements in all regions of inversion were conducted to verify the analytical model. These measurements were done for several transistors with an effective channel length of L = 3.0, 2.0, 1.7, 1.5, 1.3, 1.1, 1.0, and 0.8 μm. It is of interest to find the channel length at which the experimental results start to deviate from the analytical model.

II. Noise Analysis

In this section, analyses for drift current thermal noise (i.e., MOSFET in strong inversion) and diffusion current noise (i.e., MOSFET in weak inversion) are reviewed. The analyses are for "long" channel devices where the effects of the drain and source electric fields on the charges under the oxide (both bulk charge and inversion layer charge) can be neglected. It is shown that in thermal equilibrium, the diffusion current noise is reduced to thermal noise [9]. From these two analytical results and the thermal equilibrium assumption, a noise expression valid for all regions of inversion is deduced.

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A. Drift Current Noise

The long channel thermal noise is derived with the assumption that only drift current is present [8]. Consider a cross section of an NMOS device shown in Fig. 1, where x represents the coordinate along the channel and y is the coordinate perpendicular to the silicon surface. According to the charge sheet model [8], the drain drift current (assumed noiseless) can be written as

$$I_D = \mu W Q_I'(\psi_s)\frac{d\psi_s}{dx} \tag{1}$$

where μ is the carrier mobility, W is the width of the channel, $Q_I'(\psi_s)$ is the inversion layer charge/density, and ψ_s is the channel surface potential with respect to the neutral bulk. According to (1), a small element of the channel of length Δx has a resistance

$$\Delta R(x) = \frac{\Delta x}{\mu W Q_I'(\psi_s(x))}. \tag{2}$$

Assuming the charge carriers are in thermal equilibrium with the silicon, the current spectral density corresponding to this elemental resistance is

$$\Delta\frac{i^2}{\Delta f} = 4kT\frac{\mu W Q_I'(\psi_s(x))}{\Delta x} \tag{3}$$

where k is the Boltzmann's constant and T is the absolute temperature. The elemental drain current spectral density is obtained by applying to (3) a current division between the elemental resistance and the total channel resistance, yielding

$$\Delta\frac{i_d^2}{\Delta f} = 4kT\frac{\mu}{L^2}W Q_I'(\psi_s(x))\Delta x. \tag{4}$$

The total channel thermal noise current is simply the integral of (4) over the whole length of the channel L,

$$\frac{i_d^2}{\Delta f} = 4kT\frac{\mu}{L^2}Q_I \tag{5}$$

where Q_I is the total inversion layer charge. Later in this paper, we will show a precise representation of $(\mu/L^2)\, Q_I$ in terms of the MOS device noise parameters.

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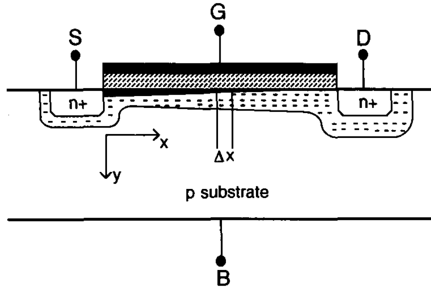

Fig. 1. Cross section of a NMOSFET used for calculating the thermal noise of the inversion layer. The coordinates used for the calculations are indicated. An elemental inversion layer with length Δx is shown.

B. Diffusion Current Noise

Consider the inversion layer of a MOS device with a charge density gradient dQ'_I/dx. The inversion layer is divided into rectangular slices of length Δx and width W identified by an index i. Due to collisions, charges make independently random jumps from one slice to an adjacent slice. Consider two adjacent slices i and $i+1$ with charge density $Q'_I(i)$ and $Q'_I(i+1)$, respectively. The net diffusion current is

$$I = I_{i\to i+1} - I_{i+1\to i} = -DW\left.\frac{dQ'_I}{dx}\right|_i \quad (6)$$

where D is the diffusion constant. Each of the independent currents $I_{i\to i+1}$ and $I_{i+1\to i}$ should show full shot noise [6]. Thus the spectral density of the diffusion noise of a slice Δx is

$$\Delta\frac{i^2}{\Delta f} = 2qI_{i\to i+1} + 2qI_{i+1\to i} \quad (7a)$$

$$\Delta\frac{i^2}{\Delta f} \approx 4qDW\frac{Q'_I}{\Delta x}. \quad (7b)$$

Assuming thermal equilibrium, one substitutes the Einstein's relation

$$D = \mu\frac{kT}{q} \quad (8)$$

into (7b), yielding

$$\Delta\frac{i^2}{\Delta f} = 4kT\frac{\mu W Q'_I}{\Delta x} \quad (9)$$

which is identical to the thermal noise of the elemental resistance derived in the previous subsection (see (3)). The diffusion noise is reduced to thermal noise when the charge carriers are in thermal equilibrium with the semiconductor lattice. Therefore (5) is also applicable for diffusion noise. Thus under thermal equilibrium assumption, both drift current noise and diffusion current noise are equivalent. This implies that the noise for all regions of inversion is described by (5).

Strictly speaking, the above arguments are only valid when the charge carriers are in thermal equilibrium with the lattice (i.e., the lateral electric field $E = 0$). In fact, the Einstein's relation expressed in (8) is only valid when $E = 0$. In this paper, thermal equilibrium is assumed to apply for $E \neq 0$. One objective of this paper is to find experimentally at what electric field (or equivalently at what channel length) the above model starts to deviate from measurements.

C. Channel Thermal Noise in Terms of MOSFET Device Parameters

The total inversion layer charge Q_I in (5), valid in all regions of inversion, is expressed in the Appendix. It was derived from the solution of the Poisson's equation for the MOS system and one dimensional charge sheet model [8], [10]–[12]. Using (A.1) and the drain current I_D of (A.3), the channel noise can be written as

$$\frac{i_d^2}{\Delta f} = 4kT\,\mu C_{\mathrm{ox}}\frac{W}{L}V_1(V_{\mathrm{GB}}, \psi_{\mathrm{so}}, \psi_{\mathrm{sL}}) \quad (10)$$

where $V_1(V_{\mathrm{GB}}, \psi_{\mathrm{so}}, \psi_{\mathrm{sL}})$ is the ratio of the square bracket in (A.1) to that of (A.3), V_{GB} is the gate-bulk voltage, ψ_{so} is the surface potential at the source end, and ψ_{sL} is the surface potential at the drain end. Note that $V_1(V_{\mathrm{GB}}, \psi_{\mathrm{so}}, \psi_{\mathrm{sL}})$ is in volts and it represents the degree of inversion along the channel.

D. MOSFET Thermal Noise Model in Circuit Applications

In literature dealing with noise in circuits (see for example [13]), the channel noise in saturation is often written as

$$\frac{i_d^2}{\Delta f} = 4kT\varepsilon g_m \quad (11)$$

where ε is a bias dependent parameter ($\varepsilon = 2/3$ for strong inversion and $\varepsilon = 1/2$ for weak inversion) and g_m is the transconductance of the device. This representation is only correct for devices with negligible body effect [1], [3], [8]. Otherwise, in order to satisfy (10), ε will have to be larger than 2/3 and 1/2 in the strong and weak inversions, respectively.

A more direct and precise way of writing the channel noise in MOSFET's is [6]

$$\frac{i_d^2}{\Delta f} = 4kT\gamma g_{\mathrm{do}} \quad (12)$$

where γ is the noise coefficient and g_{do} is the channel conductance at $V_{\mathrm{DS}} = 0$. In general, γ depends on all the terminal bias voltages; however, for devices in saturation, γ depends only on the degree of channel inversion at the source end (or equivalently on bias current). The expression for g_{do} is shown in the Appendix which can be written as

$$g_{\mathrm{do}} = \mu C_{\mathrm{ox}}\frac{W}{L}V_2(V_{\mathrm{GB}}, \psi_{\mathrm{so}}). \quad (13)$$

Note that, similar to $V_1(V_{\mathrm{GB}}, \psi_{\mathrm{so}}, \psi_{\mathrm{sL}})$ in (10), $V_2(V_{\mathrm{GB}}, \psi_{\mathrm{so}})$ is also in volts, however, it represents the degree of channel inversion at $V_{\mathrm{DS}} = 0$. In practice, g_{do} is difficult to measure because at $V_{\mathrm{DS}} = 0$, the drain current $I_D = 0$. It can be shown that the source conductance in saturation defined as follows:

$$g_s = \left.\frac{\partial I_D}{\partial V_S}\right|_{V_{\mathrm{GB}}=\text{ constant and } V_D \geq \text{ saturation voltage}} \quad (14)$$

is equal to $-g_{\mathrm{do}}$. Thus one can measure g_s as a function of drain current and replace g_{do} by $|g_s|$. This is a better way of characterizing the noise because both the noise and g_{do} (actually $|g_s|$) are measured at exactly the same operating point.

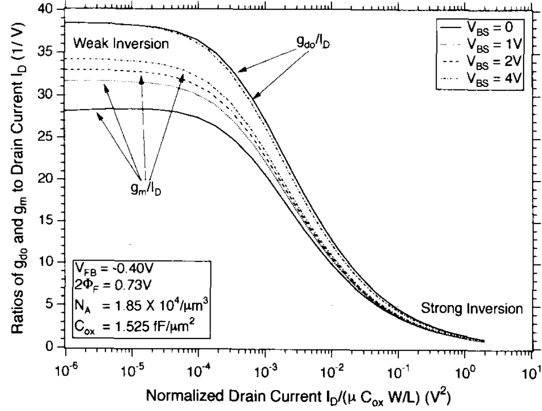

Fig. 2. Calculated ratios of the channel conductance g_{do} (or $|g_s|$) and transconductance g_m over the drain current I_D in saturation ($|V_{DS}| = 2$ V) as functions of normalized drain current $I_D/(\mu C_{ox} W/L)$ with $|V_{SB}|$ as a parameter.

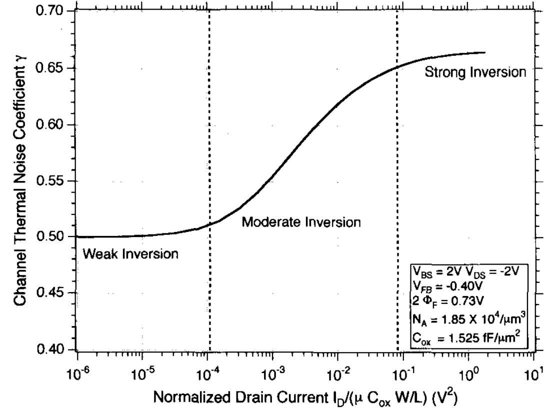

Fig. 3. Noise coefficient γ in saturation ($|V_{DS}| = 2$ V) as a function of normalized drain current for $|V_{SB}| = 2$ V. Regions of weak, moderate, and strong inversion are indicated.

Fig. 2 shows g_{do}/I_D (or $|g_s|/I_D$) as functions of I_D in saturation ($|V_{DS}| = 2$ V) with $|V_{SB}|$ as a parameter. The device parameters used in this figure and the subsequent figure belong to the PMOSFET of the United Technology Microelectronics Center (UTMC) CMOS P-well radiation hard technology. From the figure, the more inverted the channel is (i.e., drift current becomes dominant), the smaller the ratio g_{do}/I_D becomes. For a given current, g_{do}/I_D is a very weak function of $|V_{SB}|$. The dependence is noticeable in the moderate inversion where the amount of the inversion layer charge is of the same order of magnitude as the depletion charge. In this region, as $|V_{SB}|$ increases for a fixed I_D, the charge at the gate is balanced more and more by the inversion charge instead of by the depletion charge. Thus g_{do}/I_D decreases because the inversion layer is slightly more inverted. This means that even though one maintains the same I_D, the drift current increases while the diffusion current decreases by the same amount. For very large currents, the dependence on $|V_{SB}|$ is less because the channel is strongly inverted. For small currents, the channel charge is much less than the depletion charge; consequently, g_{do}/I_D is insensitive to the change in $|V_{SB}|$.

Using (10), (12), and (13), γ can be written as

$$\gamma(V_{GB}, \psi_{so}, \psi_{sL}) = \frac{V_1(V_{GB}, \psi_{so}, \psi_{sL})}{V_2(V_{GB}, \psi_{so})}. \tag{15}$$

Fig. 3 shows γ as a function of I_D in saturation ($|V_{DS}| = 2$ V) for $|V_{SB}| = 2$ V. Since g_{do} for a given current is a weak function of $|V_{SB}|$, so is γ. The figure also shows the range of γ values in the three regions of inversion.

In analog circuit applications, it is useful to refer the noise to the gate as the equivalent gate voltage noise source. This is done by dividing (12) by $g_m{}^2$. Thus the gate referred noise voltage is

$$\frac{v_g^2}{\Delta f} = 4kT\gamma \frac{g_{do}}{g_m}\frac{1}{g_m} \tag{16a}$$
$$= 4kT\ R_{eq} \tag{16b}$$

where R_{eq} is the gate-referred equivalent noise resistance. R_{eq} will be used in Section IV to characterize the noise. The expression for g_m is shown in the Appendix. Fig. 2 also shows the ratios g_m/I_D as functions of I_D in saturation with $|V_{SB}|$ as a parameter. For a given current, a rather significant increase in g_m/I_D is shown (unlike the ratio g_{do}/I_D) in weak and moderate inversions as one increases $|V_{SB}|$. At $|V_{SB}| = 0$, the ratio g_{do}/g_m is considerably larger than 1, especially in the weak and moderate inversion regions. When $|V_{SB}|$ increases, the difference between g_m and g_{do} gets smaller as a result of the reduced body effect. For lightly doped bulk, the ratio will be even closer to 1. Thus with an applied $|V_{SB}|$ (say 2 V), the combination of a reduced g_{do}/g_m and an increase g_m/I_D for a given current results in a reduction of the gate referred noise voltage. In our experimental study discussed later, all measurements are done at $|V_{SB}| = 2$ V.

E. Other Thermal Noise Sources in MOSFET's

In order to accurately characterize the channel thermal noise in MOSFET's, one needs to be aware of the existence of other thermal noise sources in the MOS system. Two additional thermal noise sources are the gate poly resistance and the bulk resistance [1], [14]–[17]. The total noise referred to the gate is then

$$\frac{v_g^2}{\Delta f} = 4kT\left(R_{eq} + R_G + \frac{g_{mb}^2}{g_m^2}R_B\right) \tag{17a}$$
$$= 4kT\ R_{eq}{}' \tag{17b}$$

where R_G is the poly gate resistance, R_B is the bulk resistance, and g_{mb} is the bulk transconductance. With a proper layout, R_G is a small constant of order Ωs [1]. For $|V_{SB}| \geq 2$ V, the effective bulk resistance $(g_{mb}^2/g_m^2)R_B$ is much smaller than R_{eq} and thus can be treated as a small constant [1], [8]. Thus the slope of R_{eq}' as a function of (g_{do}/g_m^2) is essentially equal to γ.

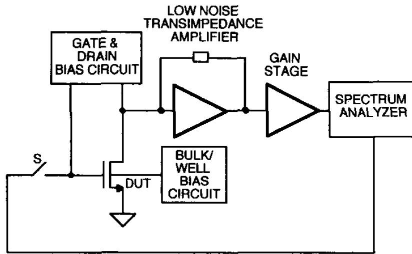

Fig. 4. Schematic of the noise measurement setup. The device under test (DUT) terminal voltages are set by the biasing circuits. The noise current at the drain terminal is amplified and converted to a voltage noise by the transimpedance amplifier. The amplified voltage noise at the output of the gain stage is fed into the spectrum analyzer. The switch S is closed only for measurement of the transfer function of the whole system.

III. Measurement Technique

A. Noise Spectral Density Measurement

The noise power spectral densities were measured using an HP 4195A spectrum analyzer. Fig. 4 shows the simplified schematic of the measurement setup. It is designed to have a large enough bandwidth (1 KHz to 50 MHz) to allow clear separation of the $1/f$ and white noise, and a low enough noise floor to allow accurate measurements [1]. The voltages at the terminals of the device under test (DUT) were independently set to obtain the desired operating points. The drain-source voltage $|V_{DS}|$ for all measurements was set at 2 V to ensure saturation condition for the range of drain currents considered in this work. To minimize the noise contribution from the bulk resistance, the source-bulk voltage $|V_{SB}|$ was set at 2 V.

For accurate measurements in the weak and moderate inversion regions, it is necessary to have very large W/L devices so that (a) the drain current noise is much larger than the noise floor, (b) a wide range of current spans each region, and (c) the noise contributions from the source/drain series and contact resistances are negligible. In addition, large gate areas are necessary to minimize the $1/f$ noise [1], [8], [13]. The devices (both P- and N-MOSFET's) measured have $W/L = 3000$ with an effective channel length $L = 3.0, 2.0, 1.7, 1.5, 1.3, 1.1,$ and 1.0 μm. In addition, $L = 0.8$ μm N-MOSFET's are also available. They were fabricated in a UTMC radiation hard CMOS 1.2 μm P-well technology. The gate structure of the transistors is of the interdigitated finger type in order to minimize the total area as well as the gate resistance.

B. Device Electrical Parameters Measurement

The key electrical parameters for characterizing the channel thermal noise are g_{do} and g_m. The channel conductance g_{do} was determined indirectly by measuring the source conductance g_s, as explained in Section II-D. These parameters were measured for each DUT using an HP 4145B semiconductor parametric analyzer at the same operating points as those used for the noise measurements.

IV. Results and Discussion

Fig. 5 shows a typical gate-referred noise spectral density for frequency spanning 1 MHz to 10 MHz. The thermal noise was extracted by averaging the spectral density over this frequency range. The value of R'_{eq}, as in (17), was obtained by dividing this average (squared) by $4kT$. This procedure was repeated for drain currents spanning the weak, moderate, and the beginning of the strong inversion regions. For our devices ($W/L \approx 3000$), the drain current ranged from 50 μA to 1.4 mA.

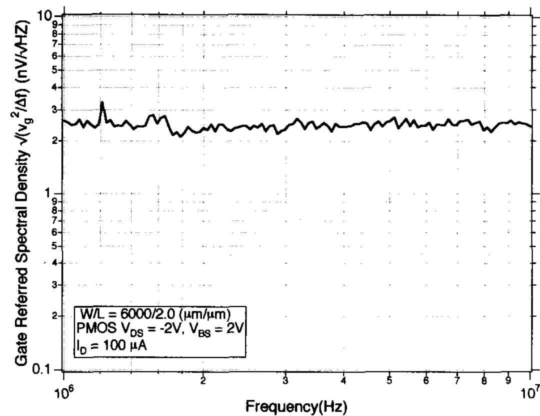

Fig. 5. Typical gate-referred noise spectral density. The gate referred noise equivalent resistance, R'_{eq} as in (17) is obtained by averaging the spectral density over the frequency range, squaring the average, and dividing by $4kT$.

Fig. 6 shows R'_{eq} as functions of the measured g_{do}/g_m^2 for P and N MOSFET's with $W/L = 6000/2.0$. The slope of these plots essentially correspond to the γ in (16a). The solid and dashed curves in Fig. 6 correspond to the theoretical calculations discussed in Section II. To better fit the data, the theoretical curves are shifted up by a resistance of 10 Ω to take into account the small noise due to the gate, the bulk resistances, and any other residual noise sources. It can be concluded that the experimental results agree well with the theoretical calculations (i.e., the slopes γ from the measurement agree well with those of the theory). For $I_D = 50$ μA (weak inversion) and the same $|V_{SB}|$, the N-MOSFET has larger noise because it resides in the well and therefore has larger body effect. On the other hand, in strong inversion, where body effect becomes less significant, the N-MOSFET has lower noise as expected.

To further test the theory, the noise for shorter channel lengths was measured for the same current range as before. For this range of currents, it was found that the corresponding g_m values were practically the same from channel length to channel length. This implies that the shorter channel devices do not suffer mobility degradation. Fig. 7 shows the measurement results for P-MOSFET's with $L = 3.0, 2.0, 1.7, 1.3,$ and 1.0 μm. For clarity, the data points for $L = 1.5$ and 1.1 μm are not shown in the figure since they are very similar to those for $L = 1.3$ and 1.0 μm, respectively. The solid curves on the figure are not based on any theoretical calculation but are solely to trace the data points. Fig. 8 shows results for N-MOSFET's. Figs. 7 and 8 also show the theoretical calculations (not shifted up this time). By comparing the slopes of the theoretical curves (dashed) to those of the experimental results, we see that the experimental results start to deviate

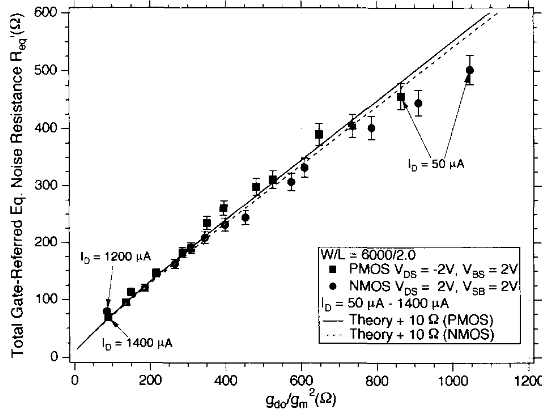

Fig. 6. The measured and calculated R'_{eq} as functions of g_{do}/g_m^2 for P- and N-MOSFET's in saturation. An additional resistance of 10 Ω is added to the theoretical curves to take into account the small thermal noise contributions due to the poly gate resistance and the bulk resistance.

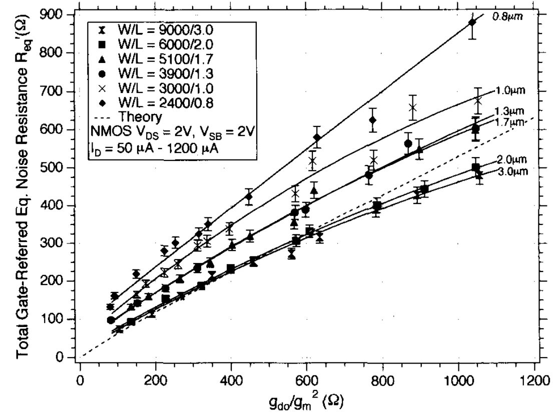

Fig. 8. The measured R'_{eq} as a function of g_{do}/g_m^2 for NMOS devices with different channel lengths.

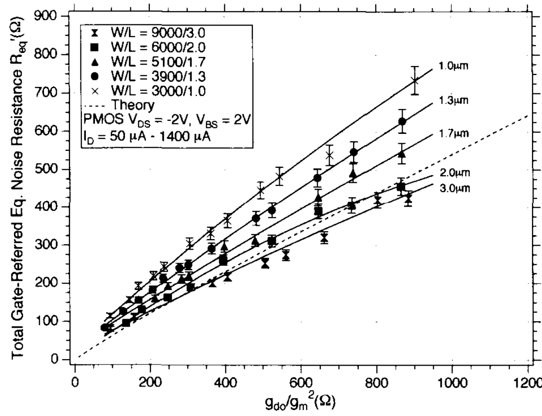

Fig. 7. The measured R'_{eq} as a function of g_{do}/g_m^2 for PMOS devices with different channel lengths. W/L is equal to 3000 for all devices. The solid curves are to trace the data points and not based on any theoretical calculation. The theoretical calculation is the dashed curve.

from the theory for devices with $L < 1.7$ μm. That is the slopes γ for $L < 1.7$ μm are larger than expected from the theory. The validity of the one dimensional long channel charge sheet model and the thermal equilibrium assumption is questionable for $L < 1.7$ μm. This limit is in agreement with the empirical curve by Brews *et al.* [18], which predicts that for this CMOS process, the long channel one dimensional charge sheet model is not valid anymore for L less than about 1.6 μm.

V. Conclusion

In this paper, analytical and experimental studies of the channel thermal noise for MOSFET's were presented. All regions of inversion in saturation were considered. The analytical study was based on the one dimensional charge sheet model. Under thermal equilibrium, the noise expression can be obtained from either drift or diffusion carrier transport mechanisms.

The noise of devices with a wide range of channel lengths was measured. The channel lengths were chosen to cover the "long" channel region (where the noise agrees with the theoretical analysis) as well as the "short" channel region (where the analytical model is insufficient to describe the noise behavior). The experimental results agree very well with the analytical model for devices with $L \geq 1.7$ μm. Assumptions made such as low lateral electric field, low charge gradient, field-independent Einstein's relation (transport related phenomena), and negligible effects of source and drain fields to the inversion and bulk charges (geometrical phenomena) for $L < 1.7$ μm are most likely to be violated.

The influence of bulk/well bias, $|V_{SB}|$ (i.e., body effect) on the properties of the device and noise parameters such as γ, g_{do}, and g_m was presented. It was also explained that due to the body effect, the most precise way to represent the drain current noise is to use the parameters γ and g_{do} as in (12). The parameter g_m is significant only when one refers the drain current noise to the gate terminal as in (16). Significant improvement in noise performance for arbitrary channel length and a fixed current is obtained by biasing the bulk/well by about 2 V. This bias reduces the bulk resistance noise and, more importantly, increases the value of g_m such that the gate referred noise voltage in (16) is minimized.

Appendix

A. Expressions of Total Inversion Layer Charge Q_I and Current I_D

$$Q_I = \frac{\mu W^2 C_{ox}^2}{I_D}\left[\phi_t \gamma_T (V_{GB} - V_{FB})\left(\psi_{sL}^{1/2} - \psi_{so}^{1/2}\right) + \left((V_{GB} - V_{FB})^2 + \phi_t\left(V_{GB} - V_{FB} - \frac{\gamma_T^2}{2}\right)\right) \times (\psi_{sL} - \psi_{so})\right.$$

$$- \left(\frac{4}{3}\gamma_T(V_{\rm GB} - V_{\rm FB}) + \phi_t\gamma_T\right)\left(\psi_{\rm sL}^{3/2} - \psi_{\rm so}^{3/2}\right) - \left(V_{\rm GB} - V_{\rm FB} - \frac{\gamma_T^2}{2} + \frac{\phi_t}{2}\right)\left(\psi_{\rm sL}^2 - \psi_{\rm so}^2\right) + \frac{4}{5}\gamma_T\left(\psi_{\rm sL}^{5/2} - \psi_{\rm so}^{5/2}\right) + \frac{1}{3}\left(\psi_{\rm sL}^3 - \psi_{\rm so}^3\right)\Bigg] \quad (A.1)$$

where ϕ_t is the thermal voltage kT/q, $V_{\rm GB}$ is the gate-bulk voltage, $V_{\rm FB}$ is the flatband voltage, $\psi_{\rm so}$ is the surface potential at the source end, $\psi_{\rm sL}$ is the surface potential at the drain end, and γ_T is the body effect parameter

$$\gamma_T = \frac{\sqrt{2\, q\, \varepsilon_s\, N_A}}{C_{\rm ox}}. \quad (A.2)$$

ε_s is the permitivity of silicon, N_A is the bulk doping concentration, $C_{\rm ox}$ is the oxide capacitance/gate area [8]. The current I_D in (A.1) is [8]

$$I_D = \mu\, C_{\rm ox}\frac{W}{L}\left[(V_{\rm GB} - V_{\rm FB})(\psi_{\rm sL} - \psi_{\rm so}) - \frac{1}{2}(\psi_{\rm sL}^2 - \psi_{\rm so}^2) - \frac{2}{3}\gamma_T(\psi_{\rm sL}^{3/2} - \psi_{\rm so}^{3/2}) + \phi_t(\psi_{\rm sL} - \psi_{\rm so}) + \phi_t\gamma_T(\psi_{\rm sL}^{1/2} - \psi_{\rm so}^{1/2})\right]. \quad (A.3)$$

B. Expression of Channel Conductance $g_{\rm do}$

The channel conductance at $V_{\rm DS} = 0$ is obtained by taking the partial derivative of (A.3) with respect to $V_{\rm DS}$ and evaluating the derivative at $V_{\rm DS} = 0$. The result is

$$g_{\rm do} = \mu\, C_{\rm ox}\frac{W}{L} \times \left.\frac{\partial\psi_{\rm sL}}{\partial V_{\rm DS}}\right|_{V_{\rm DS}=0}\left(V_{\rm GB} - V_{\rm FB} - \psi_{\rm so} - \gamma_T\psi_{\rm so}^{1/2} + \phi_t + \frac{1}{2}\gamma_T\phi_t\psi_{\rm so}^{-1/2}\right) \quad (A.4)$$

where

$$\left.\frac{\partial\psi_{\rm sL}}{\partial V_{\rm DS}}\right|_{V_{\rm DS}=0} = \frac{\frac{\gamma_T^2}{2}e^{(\psi_{\rm so} - 2\phi_F - V_{\rm SB})/\phi_t}}{V_{\rm GB} - V_{\rm FB} - \psi_{\rm so} + \frac{\gamma_T^2}{2}(1 + e^{(\psi_{\rm so} - 2\phi_F - V_{\rm SB})/\phi_t})}. \quad (A.5)$$

C. Expression of Transconductance g_m

The transconductance is obtained by taking the partial derivative of (A.3) with respect to $V_{\rm GS}$. The result is

$$g_m = \mu\, C_{\rm ox}\frac{W}{L}\left[\frac{\partial\psi_{\rm sL}}{\partial V_{\rm GS}}\left(V_{\rm GB} - V_{\rm FB} - \psi_{\rm sL} - \gamma_T\psi_{\rm sL}^{1/2} + \phi_t + \frac{1}{2}\gamma_T\phi_t\psi_{\rm sL}^{-1/2}\right) - \frac{\partial\psi_{\rm so}}{\partial V_{\rm GS}}\left(V_{\rm GB} - V_{\rm FB} - \psi_{\rm so} - \gamma_T\psi_{\rm so}^{1/2} + \phi_t + \frac{1}{2}\gamma_T\phi_t\psi_{\rm so}^{-1/2}\right) + \psi_{\rm sL} - \psi_{\rm so}\right] \quad (A.6)$$

where

$$\frac{\partial\psi_{\rm sL}}{\partial V_{\rm GS}} = \frac{V_{\rm GB} - V_{\rm FB} - \psi_{\rm sL}}{V_{\rm GB} - V_{\rm FB} - \psi_{\rm sL} + \frac{\gamma_T^2}{2}\left(1 + e^{(\psi_{\rm sL} - 2\phi_F - V_{\rm DB})/\phi_t}\right)} \quad (A.7)$$

and

$$\frac{\partial\psi_{\rm so}}{\partial V_{\rm GS}} = \frac{V_{\rm GB} - V_{\rm FB} - \psi_{\rm so}}{V_{\rm GB} - V_{\rm FB} - \psi_{\rm so} + \frac{\gamma_T^2}{2}\left(1 + e^{(\psi_{\rm so} - 2\phi_F - V_{\rm SB})/\phi_t}\right)}. \quad (A.8)$$

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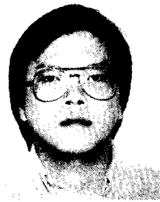

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