Analytical design considerations for MVDC solid-state circuit breakers

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Abstract

This paper investigates the design principles of a solid-state circuit breaker (SS CB) for medium voltage direct current (MVDC) grids. The emphasis is given on the design of the required active and passive components that employed in a SS DCCB based on analytic methodology. Several cases related to the characteristics of the current technology of power semiconductor devices have been investigated and evaluated in terms of maximum short-circuit current, maximum switch current, maximum switch voltage, clearance time, as well as, passive elements requirements. It has been shown that potential improvements of the current power semiconductor technology could lead to improved performance of SS DCCB with lower requirements for passive elements. In particular, the most significant characteristic that improves the overall SS breaker performance was found to be a potential reduce of the falling time (or increase of power dissipation) of the switches used in SS breaker.

Introduction

Medium Voltage (MV) direct current (DC) systems are usually used for distribution or collector systems whose requirements has previously hindered the implementation of DC grids [1]. The reasons to these hindrances are particularly related to insufficient ratings and performance of power semiconductor devices, as well as to their price. With the recent and future technological advances, however, this trend seems to reach a turning point. Recently, the integration of MVDC in a vast variety of applications such as micro grids [1], collector grids for offshore wind generation and solar power [2], marine vessels [3] and other industrial applications such as a mine site islanded micro grid [4] have been considered. For such applications, MVDC may enable advantages, such as easy interconnection of decentralized generation and storage devices, reduced number of electric power conversion stages, no need for synchronization, reduced ratings of cables and switch gears, no reactive voltage drop, easier implementation of high speed and variable frequency operation, no need for bulky low frequency AC transformers and fully controlled power flow [3].

One of the main challenges of implementing MVDC systems that still impedes their development is the design of proper and high-performance fault handling technology. Due to the inherently low cable inductances in the short distances related to MVDC applications, fault currents quickly rise to unacceptable values and impose the need of very fast fault breaking mechanisms. Traditional mechanical AC circuit breakers (AC CB) are too slow to perform this action that depends on the AC systems natural zero crossing, which is not present in DC counterparts.

Several different DCCB topologies have been proposed in literature. They can be categorized into, mechanical DCCB with active/passive resonance circuit, solid-state CBs and hybrid CBs [5, 6]. The first

configuration achieves slow clearance time, requires high maintenance but it minimizes the conduction losses. On the other hand, the solid-state CB topology achieves high clearance speed and hence, it minimizes the fault current and the thermal stress of voltage-source converters (VSCs). Today, the challenges of this CB type are the minimization of the conduction losses and the increase of their reliability. Last but not least, the hybrid CB, which has been commercialized by ABB for HVDC [7], exhibits a higher efficiency than solid-state counterpart, but lower than mechanical CB. However, it clears the short-circuit current faster than mechanical but slower than solid-state CBs. For MVDC grids, the solid-state CBs seem to suit better compared to other types due to their fast clearance times.

Many new solid-state CBs have been proposed in literature to provide fast current interruption and isolation and may be suitable for MVDC systems. Available literature on solid-state CBs suggests that much like in the case of VSCs technologies, the SS CBs may all have their suitable application [8, 9, 10]. It should, thus, be interesting to investigate the particularities of the breaker topologies and how these may fulfill different requirements and application specific needs. A solid-state CB consists of a current limiting inductor, power semiconductor devices and snubber circuits along with residual energy dissipative elements such as surge arresters. The importance of fault sensing and coordination and their direct impact on the SSCBs performance has been observed and will be further investigated by using their contrinution as a parameter in analytical expressions and simulations.

The contribution of this paper is to analyze an MVDC solid-state CB using parameters relevant for the future MVDC grids, as well as, to investigate the future potential of this breaker. In particular, the analytical investigation of the active and passive elements of the interrupting solid-state breaker topology along with potential design and operating trade-offs are analyzed and evaluated in details. Several different cases related to the current technology of the high power semiconductor devices have been considered. Last but not least, the impact of the delay due to the fault sensing and protection coordination on the design principles of a solid-state CB is also investigated and presented.

Solid-state DC Circuit Breakers for MVDC power grids

The main current showstopper for the development of solid-state breakers is the high on-state losses associated with the power electronic devices used. A literature review reveals four types of SS DCCBs based on the way they handle the residual inductive energy from the fault or how they clear the fault. These SS CBs are the interrupting, the current limiting, the resistive and the resonant CBs. The interrupting topology has been adopted in this study due to its design simplicity and therefore to the easiness in the controllability. Fig. 1 illustrates a schematic diagram of an interrupting solid-state DC CB, composed by a current limiting inductor L_s, n-series connected high power semiconductor devices S_1,...S_n along with snubber circuits and metal oxide varistors (MOVs). A short analysis of each subsystem follows.

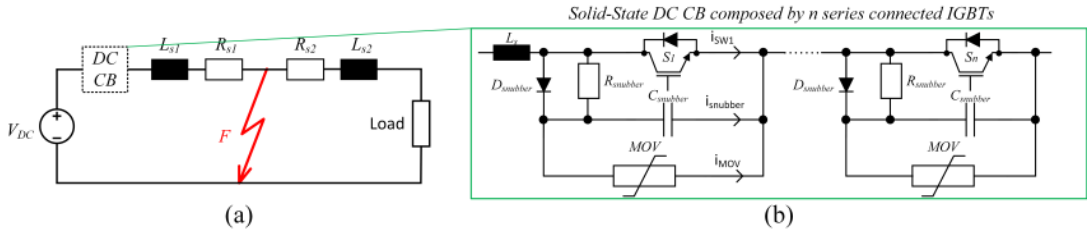

Fig. 1: a) Schematic diagram of simplified DC power grid and b) solid-state DCCB

- **Current limiting inductor:** The expected short DC cables/lines of an MVDC grid along with the absence of low frequency transformers lead to low line inductances. Therefore, when a short-circuit occurs, the fault current increases rapidly, and thus, a current-limiting inductor must be connected to the grid in order to limit both the rate of the current rise and its peak value.
- **Power semiconductor devices employed in SS DCCBs:** High power semiconductor devices are the fundamental components of a solid-state DC breaker. Insulated Gate Bipolar Transistors

(IGBTs) have gained momentum the last two decades due to their inherent advantageous characteristics compared to other devices. Apart from IGBTs, thyristor-based high power switches, such Gate Turn-Off (GTO) thyristors [11] and Gate-Commutated Thyristors (GCTs) [12] have also been proposed for solid-state DC breakers. The main advantage of these devices is the low on-state resistance. In this study, press-pack silicon-based IGBTs have been considered [13]. Commercial press-pack IGBTs have ratings up to 6.5 kV and 3 kA and enable an easy series connection of multiple devices in order to withstand high blocking voltages. Taking into account the fact that the voltage level of the future MVDC grids is foreseen to be in the range of 1-69 kV, series connection of multiple power semiconductor devices is inevitable. In addition to that, parallel connection of multiple IGBTs may be required if the load current exceeds the ratings of a single module. Consequently, the complexity of the breaker in terms of gate drive design, will increase. The challenging design of series connection and/or parallel of multiple devices is beyond the scope of the presented study.

- **Snubber circuit:** The control of the voltage rise (dv/dt) during the turn-off transient of the IGBT is performed using snubber circuits. In addition to this, snubber circuits are also used to achieve a uniform distribution of transient voltage across series-connected IGBTs. One of the most commonly used turn-off snubber circuit proposed in literature is the resistor capacitor diode (RCD) snubber (Fig. 1b).
- **Metal Oxide Varistor (MOV):** The overvoltage protection of the power semiconductors is usually performed by connecting varistors/surge arresters in parallel to the devices. The residual energy of the DC line is also dissipated in MOVs.

Analytical investigation

Fig. 1 shows the schematic diagram of the interrupting breaker connected in a test circuit. The test circuit is a simplified DC transmission line with a DC power source V_{DC} and a load. The DC cables are simplified and modelled as line inductances, L_1 and L_2, prior and after the fault point, respectively. It is assumed that the ohmic resistance of the line (R_1 and R_2) is negligible. The current limiting inductor is denoted as L_s and the total inductance seen by the breaker in case of faults equals $L_t = L_s + L_1$.

In Fig. 2, $C_{snubber}$, $R_{snubber}$ and $D_{snubber}$ are the snubber capacitor, resistance and diode respectively. Figs. 2b-e illustrate the operating stages of the interrupting SS DCCB when a short-circuit occurs which will be further elaborated below.

- **Stage 1: Occurrence of the fault.** Stage 1 starts at the time instant that the short-circuit occurs (t_f) and it lasts until the fault has been sensed and the information communicated to the breaker and the breaker has initiated the opening process (t_b). The initiation of the opening process will cause some extra delay depending on the turn-off delay time of the power semiconductor device. The time until the fault has been sensed and communicated to the breaker will depend on the fault sensing method and coordination strategy of the protection scheme. Stage 1 will behave as a simple $1^s t$ order system with a DC voltage source V_{DC} and a total inductance of $L_s + L_1$. The rate of rise of the short-circuit current and the maximum current through the breaker is given by:

$$\frac{di_{(t)}}{dt} = \frac{1}{(L_s + L_1)} V_{DC} \rightarrow I_{peak1} = i_{(t_f)} + \frac{V_{DC}}{L_s + L_1} t_b \tag{1}$$

Now suppose the power semiconductor device used in the switch has maximum rated rate of rise current $\frac{di_{sw}}{dt}_{rated}$, as well as a maximum turn-off current $I_{swrated}$. In order to stay within rated limits with some margin, the designer must define $I_{sw_{max}} < I_{swrated}$ and $\frac{di_{sw}}{dt}_{max} < \frac{di_{sw}}{dt}_{rated}$ which will be the maximum values seen by the switching device in a worst case scenario. Considering the worst case being when the fault happens close to the breaker with $L_1 = 0$, the current limiting inductor

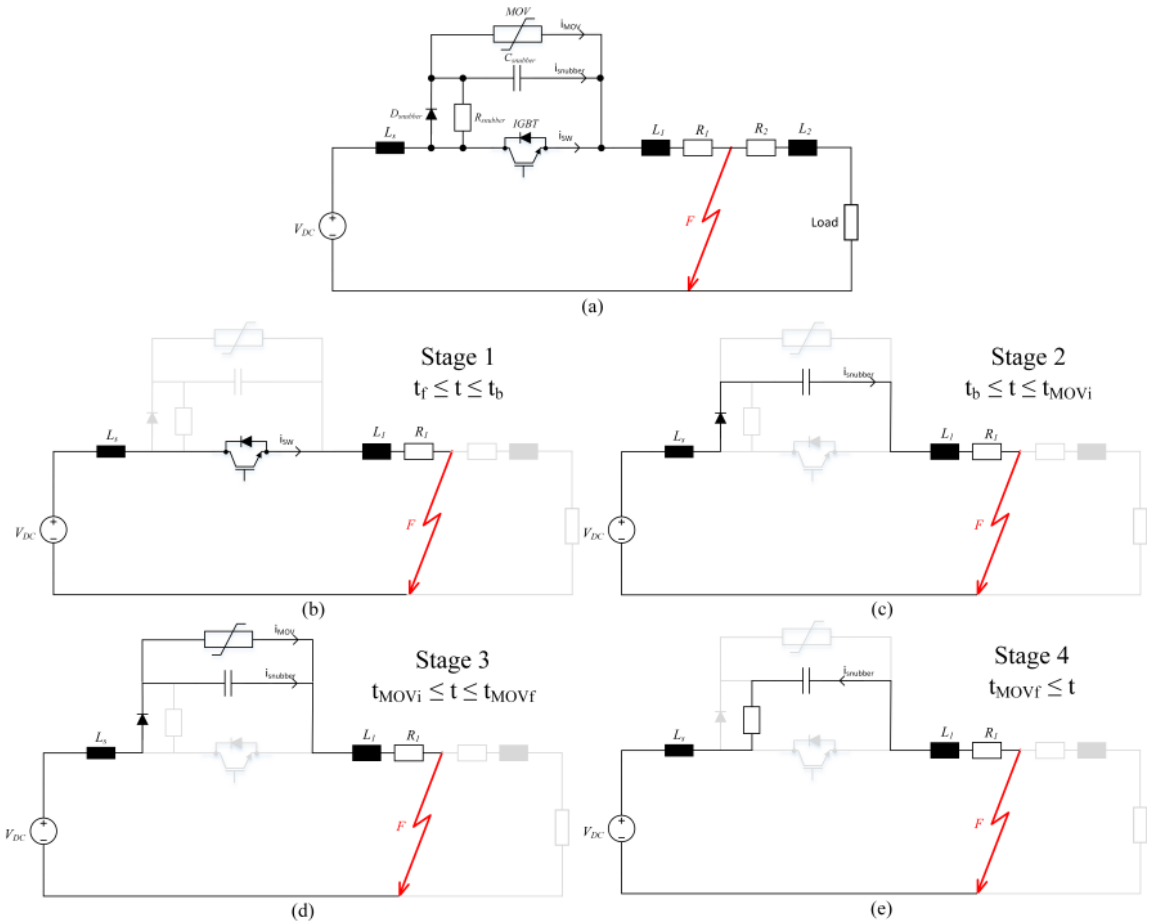

Fig. 2: Operating stages of the interrupting SS DCCB; a) schematic diagram of the breaker, b) stage 1, c) stage 2, d) stage 3 and e) stage 4

L_s must be designed such that:

$$L_s \geq \frac{V_{DC}}{min[\frac{di_{sw}}{dt}_{max}, \frac{I_{swmax} - i_{(t_f)}}{t_b}]} \tag{2}$$

- **Commutation between stage 1 and 2.** After the fault is detected, there will be a commutation stage where the fault current is commutated through the snubber capacitor as seen in Fig. 2(c). This commutation process will depend on the current falling time, t_{fall} of the chosen semiconductor devices used as the main switch in the breakers. Assuming that the current through the semiconductor device is linearly dependent on the falling time, the current and the voltage over the capacitor can be given by [14]:

$$i_{sw(t)} = i_{(t_b)}[1 - \frac{t}{t_{fall}}] \rightarrow i_{C(t)} = \frac{i_{(t_b)}}{t_{fall}} t \rightarrow v_{C(t)} = \frac{1}{C_{snubber}} \int_{t_b}^{t} i_{c(t)} dt = \frac{i_{(t_b)}}{2C_{snubber} t_{fall}} t^2 \tag{3}$$

Where $i_{(t_b)}$ is the short-circuit current at time instant t_b and v_C and i_C are the voltage over and current through the snubber capacitor. In order to limit the maximum power dissipation in the switching device to be lower than its maximum rating, the snubber capacitor must be designed according to the following criterion;

$$\frac{d(i_{sw(t)} v_{C(t)})}{dt} = 0, \quad P_{swmax} < P_{swrated} \rightarrow C_{snubber} \geq \frac{2i^2_{(t_b)}}{27 P_{swrated} t_{fall}} \tag{4}$$

Where P_{swmax} is the peak dissipated power in the power semiconductor device during turn-off and $P_{swrated}$ is the maximum allowed power dissipation in the switching device.

- **Stage 2: Current flow through the snubber circuit.** Stage 2 starts after the current completely commutates from switch to snubber path, and finishes at the time that the MOV starts to conduct the current, t_{MOVi}. The equivalent circuit is an RLC circuit as it can be seen in Fig. 2c. The following differential equations governs the system during stage 2:

$$V_{DC} = L_t \frac{di_{(t)}}{dt} + v_{C(t)} + R_f i_{(t)} \tag{5}$$

$$i_{(t)} = C_{snubber} \frac{dv_{C(t)}}{dt} \tag{6}$$

Where R_f includes all the resistances involved in the circuit (line resistance, capacitor resistance, diode resistance, inductor resistance, fault resistance). This leads to the following transfer function representation:

$$\begin{bmatrix} V_c \\ I \end{bmatrix} = G_n \begin{bmatrix} \frac{1}{\omega_0^2} v_{C(t_b)} & L_t i_{(t_b)} + C_{snubber} R_f v_{C(t_b)} & V_{DC} \\ \frac{1}{\omega_0^2} i_{(t_b)} & C_{snubber}(V_{DC} - v_{C(t_b)}) & 0 \end{bmatrix} \begin{bmatrix} s \\ 1 \\ \frac{1}{s} \end{bmatrix} \tag{7}$$

Where;

$$G_n = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2}, \quad \omega_0 = \frac{1}{\sqrt{L_t C_{snubber}}}, \quad \zeta = \frac{R_f}{2}\sqrt{\frac{C_{snubber}}{L_t}},$$

It is assumed that $v_{C(t_b)}$ is zero. In the worst case scenario, the fault is located close to the breaker where the fault resistance is approximately 0 and the inductance is equal to the current limiting inductance, $L_t = L_s$. The current will thus be given by:

$$I_{(s)} = G_n[\frac{1}{\omega_0^2} I_{(t_b)} s + C_{snubber} V_{DC}] = G_n(\frac{1}{\omega_0^2} i_{(t_b)} s + C_{snubber} V_{DC}) \tag{8}$$

A negligible R_f results in an undamped system. The solution of (8) and the maximum current will thus be given by:

$$i_{(t)} = i_{(t_b)} cos(\omega_0 t) + \sqrt{\frac{C_{snubber}}{L_t}} V_{DC} sin(\omega_0 t) \rightarrow I_{peak2} = \sqrt{i_{(t_b)}^2 + \frac{C_{snubber}}{L_t} V_{DC}^2} \tag{9}$$

Depending on the application, the maximum fault current may be subjected to certain constraints. These could be line ratings or maximum current ratings of components in the source, such as diodes in a voltage source inverter. If I_{peak2} reaches these constraints, the current limiting inductor can be further increased such that:

$$L_s = \frac{C_{snubber} V_{DC}^2}{I_{peak2}^2 - i_{(t_b)}^2} \tag{10}$$

From Eq. (5), it appears that the maximum current occurs as the capacitor voltage v_C reaches V_{DC}.

- **Stage 3: Activation of MOV.** Once the clamping voltage of the MOV (V_{cl}) is reached (at time instant, t_{MOVi}), stage 3 will be initiated as the MOV starts conducting. The current will then have decreased slightly. The initial current of stage 3 can be found by solving Eq. (7) for $v_C = V_{cl}$. Fig.

2d shows the schematic diagram of the circuit when the MOV is activated. It is assumed that the MOV can be modeled as a diode with internal resistance R_{MOV} in series with a forward voltage source V_{MOV}, which represent the voltage over the MOV. In this simplification, the MOV internal resistance is assumed linear which will be valid for small over-voltages compared to the clamping voltage. The differential equations describing the system can then be given by:

$$V_{DC} = L\frac{di_{(t)}}{dt} + v_{C(t)} \tag{11}$$

$$v_{C(t)} = (i_{(t)} - C_{snubber}\frac{dv_{C(t)}}{dt})R_{MOV} + V_{cl} \tag{12}$$

The Laplace transformation will lead to:

$$\begin{bmatrix} i \\ v_C \end{bmatrix} = G_n \begin{bmatrix} \frac{1}{\omega_0^2} I_{peak2} & \frac{L_t}{R_{MOV}} I_{peak2} + C_{snubber}(V_{DC} - V_{cl}) & \frac{1}{R_{MOV}}(V_{DC} - V_{cl}) \\ \frac{1}{\omega_0^2} V_{cl} & \frac{L_t}{R_{MOV}} V_{cl} + L_t I_{peak2} & V_{DC} \end{bmatrix} \begin{bmatrix} s \\ 1 \\ \frac{1}{s} \end{bmatrix} \tag{13}$$

Where;

$$G_n = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2}, \quad \omega_0 = \frac{1}{\sqrt{L_t C_{snubber}}}, \quad \zeta = \frac{1}{2R_{MOV}}\sqrt{\frac{L_t}{C_{snubber}}},$$

Initial current is I_{peak2} and initial voltage of the capacitor is V_{cl} from stage 2. The maximum voltage over the switch can be derived from Eq. (12) and is given by:

$$V_{max} = V_{cl} + R_{MOV} i_{(t_{max})} \tag{14}$$

Where t_{max} is the time of maximum voltage. The maximum voltage can thus be found by solving equation system of Eqs. (13) and (14). Now suppose the maximum voltage V_{max} is defined by the application, the chosen power electronic switch and the required margins. In order not to exceed this maximum voltage, from Eq. (14) the clamping voltage must be:

$$V_{cl} \leq V_{max} - R_{MOV} i_{(t_{max})} \tag{15}$$

The relationship of Eq. (15) also imposes a restriction on the MOV resistance R_{MOV} because the clamping voltage cannot possibly be chosen to be lower than the system voltage V_{DC}. The MOV resistance R_{MOV} must thus satisfy the following:

$$R_{MOV} < \frac{V_{cl} - V_{DC}}{i_{(t_{max})}} \tag{16}$$

If Eq. (16) cannot be satisfied, the maximum allowed voltage over the switching device must be increased.

From Eq. (13) it also becomes apparent that a higher clamping voltage will reduce the time until the clamping voltage is again reached (at time instant t_{MOVf}) and the MOV stops to conduct. Stage 3 is the longest stage and composes the bulk of time spent breaking the current.

- **Stage 4: MOV deactivated.** Once the voltage has dropped to the clamping voltage V_{cl}, the MOV will stop conducting and the system can again be described by the RLC circuit seen in stage 2 and given by Eq. (7), only this time with a non negligible resistance given by the snubber resistance $R_{snubber}$ because of reverse current in the snubber capacitor $C_{snubber}$. Thus, revisiting Eq. (7), it can

be seen that the voltage response is reduced to the sum of a step response of magnitude V_{sw}, an impulse response of magnitude $\sqrt{\frac{C_{snubber}}{L_s}}R_{snubber}V_{cl}$ and a zero-impulse response of magnitude V_{cl} of the second order system given by;

$$\omega_0 = \frac{1}{\sqrt{L_t C_{snubber}}},\ \ \zeta = \frac{R_{snubber}}{2}\sqrt{\frac{C_{snubber}}{L_t}},\ \ \omega_d = \omega_0\sqrt{1-\zeta^2} \tag{17}$$

From Eq. (7), it can be seen that the current is reduced to the impulse response of the same second order system with magnitude $\frac{V_{sw}-V_{cl}}{L_t}$.

From these relationships it becomes apparent that $R_{snubber}$ first of all decides the damping factor ζ and thus the main form of the response, as well as, the damped frequency ω_d. Secondly, the amplitude of the voltage, as well as, the current is a strictly increasing function of V_{cl}. It should be noted that if $R_{snubber}$ is chosen to be critically-, or over damped, there will in practice be no ringing and thus no amplitudes to consider. If, on the other hand, $R_{snubber}$ is chosen so that the system is under damped, there will be ringing, causing the current through the capacitor to go positive. If the current through the capacitor is positive, the snubber resistance is shorted and the system will be characterized in the same way as in stage 2. Thus during ringing, the characteristics of the system will alternate between characteristics given by stages 2 and 4. To avoid unnecessary ringing, a good strategy for the design of the snubber resistance $R_{snubber}$ is to design it so that the system is critically damped in the worst case. Since the loop inductance L_1 may vary depending on fault location, from Eq. (17) it is obvious that the worst case occurs when the fault point is close to the load and not close to CB point (i.e. $L_2 = 0$). This yields the lowest damping factor ζ. Following this strategy, the following design criteria will guarantee the final response to be critically- or over damped for all situations, eliminating all ringing;

$$R_{snubber} = 2\sqrt{\frac{(L_s + L_1)}{C_{snubber}}} \tag{18}$$

Case study

Five study cases have been investigated and presented below. The purpose of these investigations is to evaluate the impact of the current semiconductor technology on the design of a SS DCCB and how this technology can improve the corresponding technology of solid-state breakers. In particular, the impact of the blocking voltage, the maximum turn-off current and the maximum power dissipation of the high-power IGBTs on the SS DCCB design are examined. The strategy for the performed simulations is as follows;

- **Base case**: The *ABB 5SNA 3000K452300 StakPak IGBT Module* (with blocking voltage $V_{swrated} = 4.5kV$, maximum turn-off current $I_{swrated} = 6kA$, turn-off delay time $t_{d(off)} = 5.13\ \mu s$, fall time $t_{fall} = 1.5\ \mu s$ and maximum power dissipation $P_{swrated} = 31.2kW$) [15] has been used to create a basis with realistic parameters. The *base case* has also assumed an additional turn-off delay time of 5 µs associated with the sensing of the fault condition and communication delays. The relevant characteristics of the equivalent switching device that has been used to cover the *base case*, considering a safety margin of 20% compared to rated values, are $V_{swmax} = 3.6kV$, $I_{swmax} = 4.8kA$, $P_{swmax} = 24.96kW$ and $t_b = 10.13$µs.
- **Case 1**: This case investigates the impact of higher blocking voltage of the power semiconductor device used on the overall breaker design. This improvement could be achieved by using a single switching device with higher voltage blocking characteristics or by over-dimensioning the breaker using more power semiconductor devices in series connection. In particular, 50% increase of the $V_{swrated}$ has been considered.
- **Case 2**: This case investigates the impact of higher current capability of the power semiconductor device used on the overall breaker design. The improvement of the maximum turn-off current of

the power semiconductor device can be achieved by over-dimensioning of the breaker by parallel-connected of multiple power electronic devices. In particular, 50% increase of the $I_{swrated}$ has been considered.

- **Case 3**: The breaking delay time t_b can also affect the design of the SS DCCB. This case emulates the improvement of the power semiconductor device turn-off delay time or the improvement in sensing and coordination equipment related to the breaker by reducing the corresponding time of the *base case*. In particular, 50% decrease of the t_b has been considered.
- **Case 4**: The impact of either the maximum power dissipation P_{max} or the falling time t_{fall} of a power semiconductor device is investigated. Simulations with a reduction in the snubber capacitor compared to the *base case* have, thus, emulated a higher maximum power rating or a reduction in the falling time (or both) of the power semiconductor device. In particular, 50% increase of the $P_{swrated}$ has been considered. This will be referred to as *Case 4*.

For all cases 1-4, the MOV resistance has been assumed to be $R_{MOV} = 0.03\ \Omega$ based on the above discussion of simplified MOV modeling.

The test circuit considered in Fig. 1 consist of $V_{DC} = 2.8kV$, $R_f \approx 0$, $L_1 = L_2 = 100\ \mu H$, $I_N = 1.5kA$ and the rest of the parameters are calculated using the aforementioned analysis.

Simulation results

Fig. 3 illustrates the SS breaker response when a short-circuit occurs under the *base case*. In particular, Fig. 3a shows the various currents of the SS DCCB during the fault-clearing process. The commutation of the fault current between the three branches, namely, switch, snubber and MOV branch can be observed. Fig. 3b depicts the current and the voltage over the switch. It can be seen that both the current and the voltage are within the considered limits, taking into account a safety margin of 20% compared to rated voltage value of the power semiconductor switch used.

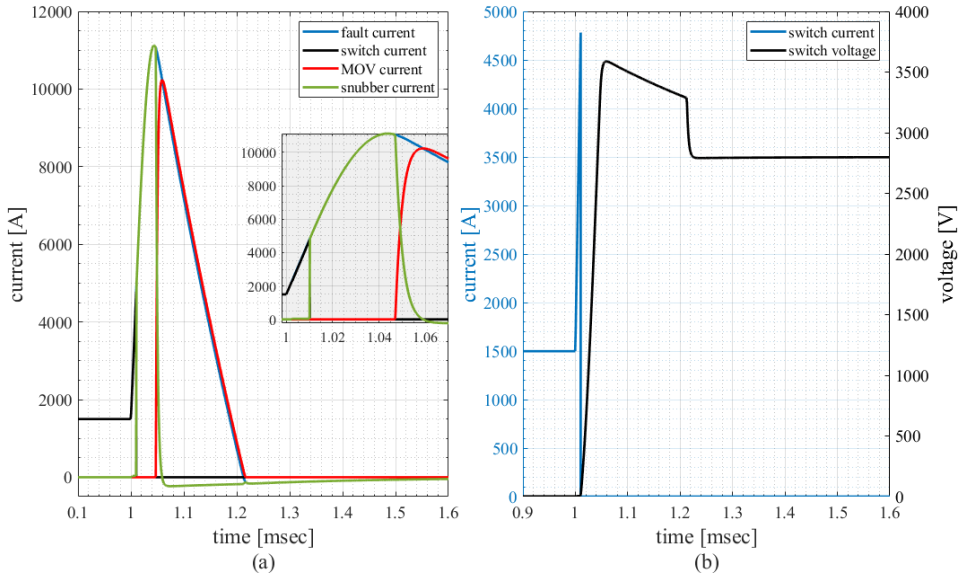

Fig. 3: a) Various currents in the SS DCCB configuration and b) current and switch over the switch at short-circuit condition in the *base case.*

Tables I and II summarize the results of the different case studies that have been simulated. The parameters examined are the expected peak values for the short-circuit current, the current that flows through the switch, the voltage over the switch, the clearance time of the breaker and also, the requirements for passive elements. In particular, the required values for the current-limiting inductor, along with the design parameters of the snubber circuit are depicted in Table I for each investigation case. Table II presents the requirements for the diode used in the snubber circuit for all cases.

In *case 1*, the majority of the evaluated parameters remain constant, apart from the voltage over the switch. It should, however, be noted that the fault current reaches for the first time the zero point significantly faster than in *base case*, while the time to reach steady-state zero value is increasing.

Increasing the maximum allowable current through the switching device, $I_{swrated}$, as illustrated by *case 2* in Tables I and II does not seem to have other positive effects than slightly decreasing the current limiting inductance L_s. All other parameters are worsened except for a decrease in required blocking voltage capability for the diode. In particular, the required size of the snubber capacitance $C_{snubber}$ and the peak fault current I_{peak2} are increased significantly.

The most prominent effect of decreasing the total delay time t_b (switching device delay time + sensing/coordination delay) as illustrated by *case 3* in Tables I and II is the reduction of required current limiting inductance, which is reduced linearly with the reduction of t_b. Total breaking time is reduced slightly and the voltage requirement of the diode is mostly increased. The maximum fault current I_{peak2} is also increased slightly.

The increase of the switching device power capabilities modeled by an increase in $P_{swrated}$ as illustrated by *case 4* in Tables I and II, decreases all parameters except for the slight increase in both required diode voltage characteristics and the snubber resistance. In particular, the peak fault current I_{peak2}, the clearance time t_{cl} and the snubber capacitance $C_{snubber}$ are improved significantly.

Table I: Summary of results for the SS DCCB for each case study

	$V_{swpeak}[kV]$	$I_{swpeak}[kA]$	$I_{peak2}[kA]$	$t_{cl}[ms]$	L_s $[\mu H]$	$C_{snubber}$ $[\mu F]$	$R_{snubber}$ $[\Omega]$
Base Case	3.59	4.78	11.1	1.03	8.6	102.6	2.85
Case 1	5.37	4.79	11.1	1.38	8.6	102.6	2.85
Case 2	3.53	7.05	20.4	1.3	4.98	230.8	1.89
Case 3	3.54	4.72	14.1	0.88	4.29	102.6	2.83
Case 4	3.59	4.78	9.34	0.81	8.6	68.4	3.49

Table II: Snubber diode requirements for each case study

	$I_{dmax}[kA]$	$V_{dmax}[kV]$	di/dt_{dmax} [kA/μs]	dv/dt_{dmax} [kV/μs]	$\int i^2dt[A^2s]$
Base Case	11.12	0.47	0.33	0.11	9521
Case 1	11.12	2.33	0.33	0.11	5723
Case 2	20.36	0.19	0.56	0.09	35625
Case 3	14.09	0.36	0.65	0.14	9262
Case 4	9.34	0.51	0.33	0.14	5171

Conclusion

In this paper, an analytic methodology for designing an interrupting SS breaker for MVDC grids has been discussed and presented. The focus was on the design of the active and passive required elements employed in such a breaker. In particular, the design of the current limiting inductor, the power semiconductor devices and the snubber circuit of the SS DCCB were analyzed in details. Furthermore, potential operating trade-offs related to the current technology of the high power semiconductor devices were evaluated. Several characteristics of a commercialized high power IGBT have been evaluated, namely, the blocking voltage, the turn-off current, the turn-off delay time and the falling time (or power dissipation). Potential improvements of the SS breaker performance in terms of minimizing the required passive elements and the short-circuit current were examined. Based on the several design cases that have been investigated, it is revealed that the most promising characteristic that can improve the performance of the breaker is found to be the turn-off switching behaviour of the device used. In particular, a potential 50% reduction of the falling time (or 50% power dissipation increase) led to the decrease of the peak short-circuit current and simultaneously, to the reduction of the required active and passive elements used in the snubber circuit.

References

[1] G. F. Reed, B. M. Grainger, A. R. Sparacino, R. J. Kerestes, and M. J. Korytowski, "Advancements in medium voltage dc architecture development with applications for powering electric vehicle charging stations," in *2012 IEEE Energytech*, pp. 1–8, May 2012.

[2] M. S. Carmeli, F. Castelli-Dezza, D. Rosati, G. Marchegiani, and M. Mauri, "Mvdc connection of offshore wind farms to the transmission system," in *SPEEDAM 2010*, pp. 1201–1206, June 2010.

[3] "Ieee recommended practice for 1 kv to 35 kv medium-voltage dc power systems on ships," *IEEE Std 1709-2010*, pp. 1–54, Nov 2010.

[4] C. Yuan, M. A. Haj-ahmed, and M. S. Illindala, "Protection strategies for medium-voltage direct-current microgrid at a remote area mine site," *IEEE Transactions on Industry Applications*, vol. 51, pp. 2846–2853, July 2015.

[5] X. Pei, O. Cwikowski, D. S. Vilchis-Rodriguez, M. Barnes, A. C. Smith, and R. Shuttleworth, "A review of technologies for mvdc circuit breakers," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, pp. 3799–3805, Oct 2016.

[6] A. Giannakis and D. Peftitsis, "Mvdc distribution grids and potential applications: Future trends and protection challenges," in *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, pp. P.1–P.9, Sep. 2018.

[7] J. H. M. Callavik, A. Blomberg and B. Jacobson, "The hybrid hvdc breaker. an innovation breakthrough enabling reliable hvdc grids," in *white paper, ABB*.

[8] H. Li, J. Zhou, Z. Liu, and D. Xu, "Solid state dc circuit breaker for super uninterruptible power supply," in *2014 International Power Electronics and Application Conference and Exposition*, pp. 1230–1235, Nov 2014.

[9] R. M. Cuzner and V. Singh, "Future shipboard mvdc system protection requirements and solid-state protective device topological tradeoffs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, pp. 244–259, March 2017.

[10] J.-Y. Kim, S.-S. Choi, S.-M. Song, and I.-D. Kim, "New dc solid state circuit breaker with reclosing and rebreaking capabilities," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, pp. 3554–3558, May 2016.

[11] K. Lawson, S. B. Bayne, S. Lacouture, L. Cheng, H. O'brien, A. Ogunniyi, and C. Scozzie, "Safe operating area and long-term reliability of 9-kV silicon carbide PNPN super gate turn-off thyristors," *IEEE Electron Device Letters*, vol. 35, no. 8, pp. 862–864, 2014.

[12] F. Agostini, U. Vemulapati, D. Torresin, M. Arnold, M. Rahimo, A. Antoniazzi, L. Raciti, D. Pessina, and H. Suryanarayana, "1MW bi-directional DC solid state circuit breaker based on air cooled reverse blocking-IGCT," in *2015 IEEE Electric Ship Technologies Symposium (ESTS)*, pp. 287–292, IEEE, 6 2015.

[13] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices: Physics, Characteristics, Reliability*. Springer, 2010.

[14] N. Mohan, T. Undeland, and P. W. Robbins, *Power Electronics: Converter, Applications, and Design*. John Wiley, 2003.

[15] ABB, "Data sheet, doc. no. 5sya 1450-03, 5sna 3000k452300 stakpak igbt module," november 2017.