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ABSTRACT

This paper presents an analytical investigation of the drain current model for symmetric short channel InGaAs gate-all-around (GAA) MOSFETs valid from depletion to strong inversion using a continuous expression. The development of the core model is facilitated by the solution of the quasi-2D Poisson equation in the doped channel, accounting for interface trap defects and fixed oxide charges. Correction to short channel effects such as threshold voltage roll-off, drain induced barrier lowering, and subthreshold slope degradation is later introduced, complemented with channel length modulation, velocity saturation, and mobility degradation from surface roughness, leading to accurate mobile charge density for electrostatic capacitance–voltage and transport characterization. The effect of physical process parameters such as fin width, oxide thickness, and channel length scaling is thoroughly investigated in both on and off states of the transistor. The robustness of the model is reflected by the precise match with published experimental reports in the literature. An R_{on} of 1160 $\Omega\,\mu$m is obtained from output characteristics and a switching efficiency improvement of 2.5 times is estimated by incorporating a high-κ dielectric into the GAA transistor. Numerical 3D simulations from TCAD corroborate the validity of the proposed model in all regions of operation.

I. INTRODUCTION

Electrostatic control in three dimensions has become imperative to reduce the short channel effects (SCEs) in deeply scaled transistors beyond the 22 nm technology node. The gate-all-around (GAA) MOSFET has proven to provide the greatest immunity to SCEs with the shortest natural length (λ) and impose stronger gate control over surface carriers.[1–3] Tremendous effort expended behind silicon nanowires and the incorporation of strain engineering reveal the potential of silicon as a favorable channel material for CMOS technology.[4–6] However, phonon scattering and surface roughness from the wrap-around gate configuration limit the mobility to subpar levels, impeding the performance of silicon nanowires from reaching near ballistic limits. This opens room for further improvement in carrier transport by utilizing high mobility III–V semiconductor channel materials.

To this end, InGaAs has attracted the attention of researchers as a viable candidate for providing superior drain current in both on and off states.[7–9] On one hand, intense research in the past four decades has ushered significant progress on the use of atomic layer deposition (ALD) to integrate a thermodynamically stable high-κ dielectric on a III–V semiconductor, which drastically reduces gate leakage current of InGaAs based transistors, offering better effective oxide thickness (EOT) for minimization of static power dissipation.[10] On the other hand, the inherent high mobility of a III–V semiconductor as the active channel material truncates dynamic power dissipation in the transistor, offering the same drive current at a reduced supply voltage.[11] This favored InGaAs gate-all-around MOSFETs to gain popularity in switching and logic applications.[9]

Although both cylindrical nanowires and rectangular GAA MOSFETs have exhibited excellent transport and subthreshold performance recently,[12,13] the rectangular geometry offers an additional

advantage in terms of the fabrication viewpoint. First, the seamless integration of rectangular MOSFETs with FinFET technology is possible because lateral nanowires bear strong resemblance with the FinFET architecture. This minimal deviation in the fabrication process encourages the semiconductor industry to reap the benefits provided by rectangular GAA MOSFETs over its cylindrical counterparts. Moreover, rectangular GAA MOSFETs can be grown epitaxially into thin nanosheets unlike cylindrical nanowire MOSFETs, which are grown by the vapor–liquid–solid (VLS) method.[14] This enables precise control of nanowire height in the rectangular geometry. One of the challenges in fabricating cylindrical nanowire is controlling the shape of the nanowire since the transport properties rely heavily on the nanowire diameter.[15] This difficulty is circumvented in rectangular GAA MOSFETs with etching techniques, allowing exact control of nanosheet width. Monolithic 3D stacking has persuaded researchers to explore the prospect of stacked nanosheets with a goal to achieve higher current drive while ensuring more W_{eff} under the same footprint as FinFETs.[16,17]

There have been numerous experimental reports on InGaAs MOSFETs exhibiting high drain current and excellent subthreshold characteristics.[3,7,8,18] Recently, short channel InGaAs GAA nanowire has been studied via top down approach, and numerical simulation of such a device illustrated volume inversion inside the active region for a fin width as low as 30 nm, which otherwise would require deca-nanometer dimensions for silicon counterparts.[19,20] Quantum mechanical simulations were carried out by Khan *et al.* to determine electrostatic charge and carrier transport under the uncoupled mode space approach, which is computationally expensive and often depends on the numerical convergence of the solution.[21,22] Existing analytical models developed for double-gate MOSFETs cannot be extrapolated to GAA geometry without involving proper physics into the Poisson equation. Compact models developed for silicon nanowires use a constant difference in potential between the center and the surface, which results in deviations near the threshold region and cannot be applied to the strong inversion operation.[23] Moreover, in InGaAs MOSFETs, a saturation of the decrease in subthreshold current is observed due to high drain junction leakage, which is not reflected by silicon based analytic reports.[11] Besides, fixed oxide charge and interface trap defects are neglected in these models, which are significant in high-κ oxide/semiconductor interfaces and crucial for device performance evaluation. An efficient analytical model is, therefore, due for characterizing the electrostatic and transport behavior of depletion mode GAA MOSFETs that would predict the performance metrics with scaling of process parameters.

In this paper, an analytical drain current model is proposed for symmetric operation of short channel InGaAs GAA MOSFETs that accurately predicts the carrier density under electrostatic conditions as well as computes drain current from depletion to strong inversion under applied drain bias, incorporating interface traps and volume oxide charges. In Sec. II, a quasi-2D Poisson equation is solved in the active region with appropriate boundary conditions to determine the mobile carrier density, facilitating the determination of the quasi-static capacitance–voltage (CV) profile. The drain current is evaluated in Sec. III under the classical drift-diffusion formalism with the inclusion of certain short channel effects such as drain induced barrier lowering (DIBL), threshold voltage roll-off, subthreshold slope degradation, series resistance, channel length modulation, velocity saturation, and mobility degradation due to vertical and lateral electric fields to implicate the underlying physics of short channel operation. The impact of physical process parameters is rigorously investigated with channel length scaling in Sec. IV. The feasibility of high-κ dielectrics to enhance device subthreshold characteristics will also be explored in this section. The excellent match between model results and published experimental reports highlights the accuracy of the proposed model in conjunction with numerical TCAD simulation to validate scaling properties. Section V systematically draws the conclusion of this work.

II. ELECTROSTATIC MODEL DESCRIPTION

A. Charge modeling

The symmetric gate-all-around MOSFET under consideration has acceptor doping concentration N_A in the $In_{1-x}Ga_xAs$ channel with equal width (W) and height (H), gate length L, and ALD Al_2O_3 having thickness t_{ox}, as shown in Fig. 1. The Ga-composition is 0.47 where not stated, and the central nanowire axis is taken as the origin so that the oxide/semiconductor interface is at $x = y = \mp W/2$.

Under the normal operating regime, the majority of carriers can be neglected, and the gradual channel approximation applies to the quasi-2D Poisson equation of a long channel GAA MOSFET,[24]

$$\frac{d^2\phi}{dx^2} + \frac{d^2\phi}{dy^2} = \frac{qN_A}{\varepsilon_s}\left(e^{\frac{\phi-2\phi_f-V}{\phi_t}} + 1\right). \tag{1}$$

Here, ε_s is the semiconductor permittivity, V is the electron quasi-fermi level with reference to the source, $\phi_t = kT/q$ is the thermal voltage, $\phi_f = \phi_t \ln(N_A/n_i)$, n_i is the intrinsic carrier density of $In_{0.53}Ga_{0.47}As$, and x and y represent the width and height directions, respectively. Due to the symmetric cross section, the electric field is identical in magnitude in both x and y directions, verified by 3D numerical simulations. Thus, the simplifying assumption $\frac{d\phi}{dx} = \frac{d\phi}{dy}$ applies to (1) leading to

$$\frac{d}{d\phi}\left(\frac{d\phi}{dx}\right)^2 = \frac{qN_A}{\varepsilon_s}\left(e^{\frac{\phi-2\phi_f-V}{\phi_t}} + 1\right). \tag{2}$$

Since (2) does not possess a closed form solution, by integrating once from the central nanowire axis to the oxide/semiconductor interface with appropriate boundary conditions,[24,25] which are

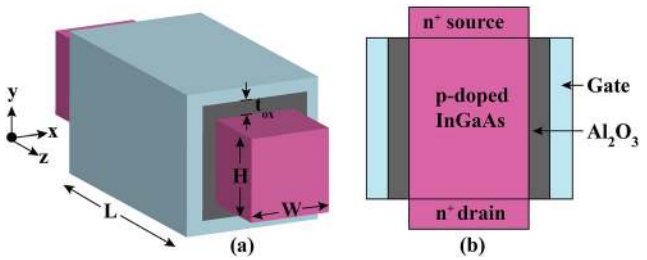

FIG. 1. Schematic view of a GAA MOSFET. The source/drain is heavily doped for Ohmic contacts, and the $In_{0.53}Ga_{0.47}As$ channel is p-doped. (a) Perspective view. (b) Lateral view.

$\phi = \phi_0$, $\frac{d\phi}{dx} = 0$ at the central nanowire axis, $\phi = \phi_s$, and $\frac{d\phi}{dx} = E_s$ at the interface, we get

$$E_s = \sqrt{\frac{qN_A}{\varepsilon_s}}\phi_t \sqrt{e^{\frac{\phi_s - 2\phi_f - V}{\phi_t}}\left(1 - e^{-\frac{\phi_s - \phi_0}{\phi_t}}\right) + \frac{\phi_s - \phi_0}{\phi_t}}, \quad (3)$$

where ϕ_s and ϕ_0 are the surface and center potential of the nanowire MOSFET, respectively. For the sake of simplicity, we consider $\alpha = (\phi_s - \phi_0)/\phi_t$ as the normalized difference of potential, which, in deep depletion, takes a constant value (α_{st}) under the full depletion approximation (FDA) in the Poisson equation,

$$\alpha_{st} = \frac{qN_A W^2}{16\varepsilon_s \phi_t} = \frac{Q_b}{16\varepsilon_s \phi_t}, \quad (4)$$

where Q_b is the total fixed charge per unit length.

Although the use of constant α_{st} well above the threshold is a crude approximation,[23] by relying on a coarse finite difference method, an exact expression of the normalized difference of potential above the threshold can be written in terms of the principle branch of the Lambert function,[26]

$$\alpha(\phi_s) = \alpha_{st} + \mathrm{LW}\left(\alpha_{st} e^{-\alpha_{st}} e^{\frac{\phi_s - 2\phi_f - V}{\phi_t}}\right). \quad (5)$$

Using Eq. (5) in (3) helps reduce the surface electric field in terms of ϕ_s only,

$$E_s(\phi_s) = \sqrt{\frac{qN_A}{\varepsilon_s}}\phi_t \sqrt{e^{\frac{\phi_s - 2\phi_f - V}{\phi_t}} + \left(1 - \frac{1}{\alpha_{st}}\right)\alpha + 1}. \quad (6)$$

Since the space charge density per unit length in the semiconductor is given by $Q_s = 4W\varepsilon_s E_s$, the mobile charge density per unit length follows from the difference in space charge density and fixed charge density.

Despite advancement in ALD techniques, significant trap defects exist at the high-κ oxide/semiconductor interface, which are accounted from the flat D_{it} profile through the relation[22]

$$Q_{it} = \int_{E_i}^{E_j} D_{it}\, dE, \quad (7)$$

where $E_i = E_0$ and $E_j = E_F$ if E_F lies above E_0 and vice versa. E_0 is the charge neutrality level of interface defects (~ 0.27 eV), which are mainly of donor type for Al_2O_3.[27] The presence of positive fixed oxide charges Q_f distributed throughout the gate dielectric affects the flat-band voltage V_{fb} by

$$V_{fb} = \phi_{ms} - \frac{Q_f}{C_{ox}}, \quad (8)$$

where ϕ_{ms} is the metal–semiconductor work function difference and C_{ox} is the oxide capacitance per unit length defined as

$$C_{ox} = \frac{4W\varepsilon_{ox}}{t_{ox}} + 8C_{fr}. \quad (9)$$

Here, $C_{fr} = 2(\varepsilon_{ox}/\pi)\ln(1 + d_1/d_2)$ is the fringing capacitance resulting from the perpendicular plate alignment in the corners of the GAA MOSFET.[28]

Applying Gauss's law to the oxide/semiconductor interface and using (6) relate the gate voltage to the surface potential by

$$C_{ox}(V_G - V_{fb} - \phi_s) = 4W\varepsilon_s E_s. \quad (10)$$

The solution of (10) facilitates the evaluation of surface potential necessary for determining mobile charge that is modulated under electrostatic conditions and takes part in carrier transport,

$$Q_n = Q_s - Q_b + Q_{it}. \quad (11)$$

The approximation of the Lambert function given by (12) remarkably improves the speed of the solution in (10) with only a minor error introduced in the threshold region, as will be discussed in Sec. IV,[29]

$$\mathrm{LW}(\gamma) \approx \ln(1 + \gamma)\left(1 - \frac{\ln(1 + \ln(1 + \gamma))}{2 + \ln(1 + \gamma)}\right). \quad (12)$$

B. Capacitance–voltage characteristics

The quasi-static capacitance–voltage profile is obtained from gated mobile charge density by differentiating Q_n with respect to gate voltage,

$$C_G = \frac{dQ_n(V_G)}{dV_G}, \quad (13)$$

where C_G depends implicitly on physical dimensions, material properties, and the gate dielectric.

III. TRANSPORT MODEL DESCRIPTION

The core drain current of the short channel GAA transistor is expressed in terms of the following integral:

$$I_D = \frac{\mu_{eff}}{L_{eff}} \int_{V_S}^{V_D} Q_n(V_G + \Delta\phi_{min})\, dV, \quad (14)$$

where μ_{eff} and L_{eff} are effective mobility and channel length, respectively, after accounting for mobility degradation and channel length modulation and $\Delta\phi_{min}$ is the minimum potential barrier change in the conduction channel as elaborated below.

A. SCE correction

The potential barrier along the conduction path is minimum in the leakiest path of the transistor, which lies in the central nanowire axis of the MOSFET. The degree of SCE affecting threshold voltage (V_{th}) roll-off, DIBL, and subthreshold slope degradation of the short channel transistor can be modeled by the change in this minimum potential obtained from the solution of the quasi-2D Poisson equation written in terms of ϕ_0 under FDA as follows:[30]

$$\frac{d^2\phi_0(z)}{dz^2} + \frac{V_G - V_{fb} - \phi_0}{\lambda^2} = \frac{qN_A}{\varepsilon_s}, \quad (15)$$

where the characteristic natural length of the symmetric GAA MOSFET is defined as[2]

$$\lambda = \sqrt{\frac{\varepsilon_s W t_{ox}}{4\varepsilon_{ox}}\left(1 + \frac{\varepsilon_{ox} W}{4\varepsilon_s t_{ox}}\right)}. \tag{16}$$

Here, the natural length of the GAA MOSFET has been derived from the parabolic potential model, which was proposed by Suzuki *et al.*[31] and Auth and Plummer[32] and further corroborated by the authors of Refs. 30, 33, and 34. By applying boundary conditions $\phi_0(0) = V_{bi}$ at the source end and $\phi_0(L) = V_{bi} + V_{DS}$ at the drain end, (15) is solved to obtain

$$\phi_0, \min = \frac{A \sinh\left(\frac{L - z_{min}}{\lambda}\right) + B \sinh\left(\frac{z_{min}}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} + V_{SL}, \tag{17}$$

where the point of minimum potential is given by

$$z_{min} = \frac{\lambda}{2} \ln\left(\frac{A e^{\frac{L}{\lambda}} - B}{B - A e^{-\frac{L}{\lambda}}}\right). \tag{18}$$

Here, the built-in potential $V_{bi} = \phi_t \ln\left(N_D N_A / n_i^2\right)$ depends on the concentration of the heavily doped source/drain region N_D,

$$A = V_{bi} - V_{SL}, \tag{19}$$

$$B = V_{bi} - V_{SL} + V_{DS}, \tag{20}$$

$$V_{SL} = V_G - V_{fb} - \frac{qN_A}{\varepsilon_s}\lambda^2. \tag{21}$$

It is to be noted that (18) is valid in the subthreshold region only. Hence, to determine z_{min}, the gate voltage is limited to threshold voltage.

At low V_{DS}, the approximation $A \approx B$ leads to $z_{min} = L/2$ and facilitates the determination of threshold voltage for short channel GAA transistors ($V_{th,SC}$) given by

$$V_{th,SC} = V_{th,LC} - \phi_{min,th}, \tag{22}$$

where $V_{th,LC}$ is the threshold voltage of the long channel GAA MOSFET obtained from the double derivative method in Ref. 25 and $\phi_{min,\,th}$ is the threshold voltage roll-off due to scaling of the gate length, evaluated by considering $\phi_{min,\,th}$ as the difference between the long channel minimum potential and the shift in minimum potential induced by the SCE,[33]

$$\phi_{min,th} = \frac{2V_{SL} \sinh\left(\frac{L}{2\lambda}\right)}{2 \sinh\left(\frac{L}{2\lambda}\right) + \sinh\left(\frac{L}{\lambda}\right)}. \tag{23}$$

The difference between (17) and (21) provides the change in minimum potential barrier $\Delta\phi_{min}$ necessary for SCE correction in the core transport model (14).

B. Velocity saturation

The drain saturation voltage of long channel devices $V_{GT} = V_{GS} - V_{th,LC}$ is no longer followed by short channel transistors due to velocity saturation. An empirical relation, derived from numerous simulations for channel lengths lower than 300 nm, models the drain saturation voltage as[35]

$$V_{DS,sat(SC)} = -0.36 + \eta(L v_{sat})^{\frac{1}{3}} V_{GT}^{\frac{1}{2}}, \tag{24}$$

where η is an adjusting parameter and v_{sat} is the saturation velocity. The drain saturation voltage $V_{DS,sat(SC)}$ is gradually limited from its long channel counterpart by the relation

$$V_{DS,sat} = \frac{1}{2} V_{DS,sat(SC)}(1 + \tanh(3V_{GT})) + \frac{1}{2} V_{GT}(1 - \tanh(3V_{GT})). \tag{25}$$

An effective drain voltage is used in the core model where the drain voltage from the terminal is restricted to drain saturation voltage by the continuous expression

$$V_{DS,eff} = V_{DS,sat} \frac{1 - \ln\left(e^{8\left(1 - \frac{V_{DS}}{V_{DS,sat}}\right)} + 1\right)}{\ln(e^8 + 1)}. \tag{26}$$

C. Mobility degradation

The degradation in mobility in the active region, resulting from the high lateral field due to proximity of the drain terminal to source end and surface scattering induced by the vertical electric field, is incorporated into the transport model by the effective mobility expression given by

$$\mu_{eff} = \frac{\mu_1}{\left[1 + \left(\frac{\mu_1 V_{DS,eff}}{v_{sat} L}\right)^{\sigma}\right]^{\frac{1}{\sigma}}}. \tag{27}$$

Here, σ is a constant parameter, which takes into account the carrier–carrier scattering in the channel region arising from the high lateral field, and μ_1 is the vertical field mobility degradation expressed in terms of low field mobility μ_0 and mobility degradation coefficient θ as

$$\mu_1 = \frac{\mu_0}{1 + \frac{1}{2}\theta(V_{GS} - V_{th,SC})[1 + \tanh(8(V_{GS} - V_{th,SC}))]}. \tag{28}$$

The mobility degradation coefficient is calibrated with experimental reports[19] such that contributions from surface scattering are incorporated into the model. Consequently, the corner effect in the GAA structure becomes strong at high overdrive voltage. The hyperbolic tangent factor in the denominator of (28) brings about this degradation at high gate field, thus mitigating the complexity of the numerical simulation.

D. Channel length modulation

As drain voltage exceeds saturation voltage, the short channel device suffers from reduced L due to extension of the drain-channel

depletion region. For $V_{DS} > V_{DS,sat}$, the effective channel length then follows[33]

$$L_{eff} = L - \sqrt{\frac{\kappa\varepsilon_s\beta}{qN_A}(1 + \tanh(10\beta))}, \quad (29)$$

where κ is a fitting parameter and $\beta = V_{DS} - V_{DS,sat}$.

E. Series resistance

The reduction in drain current in the saturation regime is attributed to the presence of parasitic resistance causing a voltage drop between the gate–source and the drain–source region. The total resistance can then be expressed in terms of channel resistance R_{ch} and parasitic resistance $R_S(R_D)$ at the source (drain) end as[36]

$$R_T = R_{ch} + R_S + R_D = \frac{V_{DS,eff}}{I'_D}. \quad (30)$$

Taking (14) to be the drain current without parasitic resistance and using $R_{ch} = V_{DS,eff}/I_D$, we get the final drain current model (I'_D) in the form

$$I'_D = \left[\frac{1}{I_D} + \frac{R_S + R_D}{V_{DS,eff}}\right]^{-1}. \quad (31)$$

IV. RESULTS AND DISCUSSION

The results derived from the analytical model in Secs. II and III were compared with the experimental demonstration in Ref. 19 and further corroborated with 3D numerical simulations using the Synopsis tool.[38] In order to capture the physical effects inherent in the inversion mode operation of the short channel GAA MOSFET, various models were used in the TCAD simulation. This includes mobility degradation at the interface due to surface roughness and surface phonon and carrier–carrier scattering, which stem from the doping within the channel region. Apart from mobility degradation, the velocity saturation model and trap charge specification at the semiconductor–oxide interface and fixed oxide charges distributed throughout the gate dielectric were utilized. Generation–recombination processes account for exchange of carriers between the conduction and valence band. They are very important for device physics, hence these were implemented during device simulation. As oxide thickness, channel width, and gate length are scaled toward the deca-nanometer regime, certain non-ideal effects come into play and degrade subthreshold characteristics. These effects are included by invoking the density gradient quantization model for important quantum effects. Table I lists the relevant physical process parameters used throughout this work for validation. As can be seen in Fig. 2(a), the mobile charge density predicted by the model, after inclusion of interface trap defects and a positive fixed oxide charge of ~ 9×10^{18} cm^{-3} distributed throughout the volume of oxide, matches well with that extracted at mid-channel from simulation. The use of (12) in the solution of mobile charge dramatically enhances the computation speed of the model with only an error of about 0.51% error introduced in the transition from threshold to weak inversion.

The effect of physical dimension and material properties on CV characteristics is illustrated in Fig. 3. The model accounts for minority carrier concentration only with the CV profile decreasing to zero in the depletion mode and saturating to oxide capacitance in the strong inversion regime. As dictated by (9), the oxide capacitance is highest for a larger fin width and the thinnest gate oxide. Figure 3(b) reveals that the electrostatic behavior of a GAA MOSFET depends strongly on fin width in comparison to oxide thickness. The analysis of devices with a fin width smaller than 10 nm is restricted from the proposed model due to negligence of the quantum effect. With inclusion of the density gradient quantization model in TCAD, the simulation results reflect a rightward shift in the CV curve for a fin width of 10 nm, indicating the impact of quantum effect in threshold voltage shift near the subthreshold region and a degradation of gate capacitance in the strong inversion regime. On the contrary, channel doping and the Ga-mole fraction affects the CV profile in the depletion region only. For channel doping above 1×10^{17} cm^{-3}, the shift in the CV curve is more prominent. At higher doping levels, the GAA MOSFET may enter partial depletion, requiring greater gate bias to create channel inversion. A decrease in the Ga mole fraction causes a leftward shift in CV transition, which is expected from the decreased bandgap of $In_{1-x}Ga_xAs$, facilitating the electron transition from the valence band to the conduction band at a reduced gate bias, as shown in Fig. 3(d).

The transfer characteristics obtained from the proposed model are displayed in Fig. 4. The drain current and extrinsic

TABLE I. Process/device parameters used in this work.

Parameter description (unit)	Value
Fin width (nm)	20–40
Oxide thickness (nm)	2.5–10
Acceptor concentration (cm^{-3})	$1 \times 10^{16} - 1 \times 10^{18}$
Mole fraction	0.25–0.47
Gate metal work function (eV)	4.6
Midgap D_{it} (cm^{-2} eV^{-1})	5.6×10^{12}
Relative permittivity of $In_{1-x}Ga_xAs$	13.9–14.2
Relative permittivity of Al_2O_3	9.3[a]
Relative permittivity of $LaAlO_3$	17[b]
Relative permittivity of HfO_2	25[c]

[a]Reference 18.
[b]Reference 37.
[c]Reference 38.

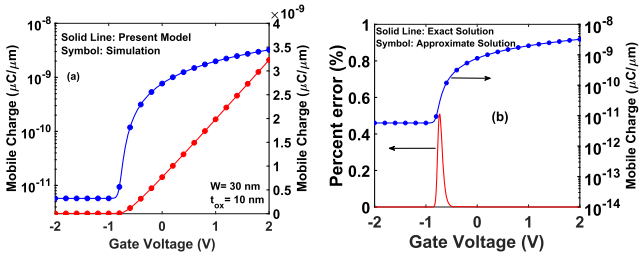

FIG. 2. Mobile charge density as a function of gate bias for a GAA MOSFET at $N_A = 2 \times 10^{16}$ cm^{-3}. (a) Comparison between the model and simulated charge density in both linear and log scales at low V_{DS}. (b) Error in charge density from using (12) instead of the Lambert function. The largest error occurs near the threshold region.

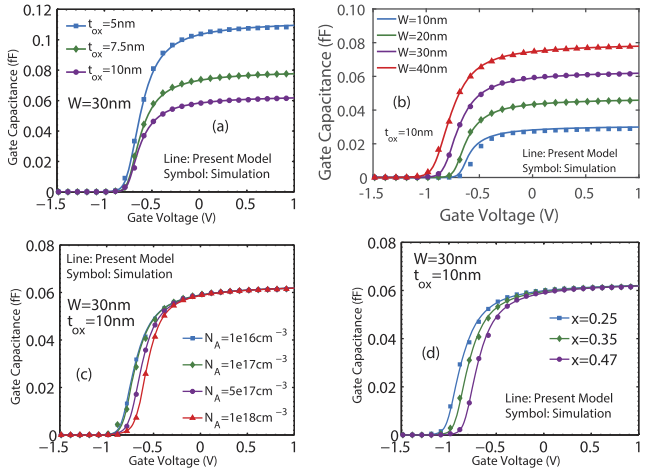

FIG. 3. Effect of device dimensions and material properties on capacitance–voltage characteristics of a nanowire MOSFET (a) for various oxide thicknesses and (b) for various fin widths. The fin width has a greater impact on CV characteristics than oxide thickness, which is reflected by a shift in threshold voltage. The impact of quantum effect on the CV profile is seen for a fin width of 10 nm where simulation results reflect a rightward shift in CV arising from the threshold voltage shift in the subthreshold region and gate capacitance degradation in the strong inversion region. (c)–(d) The impact of channel doping (x = 0.47) and the Ga-mole fraction ($N_A = 2 \times 10^{16}$ cm^{-3}) on electrostatic behavior of the same device. The saturated oxide capacitance is independent of channel doping and the mole fraction of Ga. High channel doping (above 1×10^{17} cm^{-3}) affects the CV profile to a greater extent.

transconductance g_m are normalized by the active region perimeter (2W + 2H). Some of the transport model parameters used to calibrate the model with published experimental reports are shown in Table II, which accounts for velocity saturation, mobility degradation, channel length modulation, and series resistance.

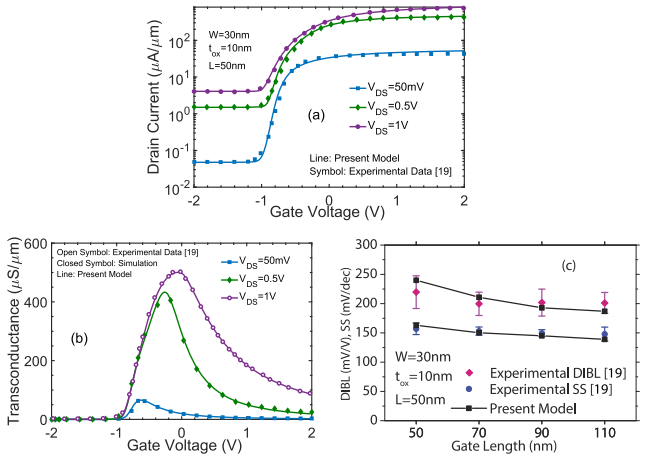

FIG. 4. Transfer characteristics of a 50 nm GAA MOSFET. (a) Drain current as a function of gate voltage. (b) Extrinsic transconductance. (c) DIBL and the subthreshold slope extracted from the I_D–V_G plot. Experimental data have been extracted from Ref. 19.

TABLE II. Relevant parameters used in the transport model.

Parameter description (unit)	Value
Parasitic source (drain) resistance (kΩ)	0.5–5
Saturation velocity (10^5 m/s)	3[a]
Low field electron mobility (cm^2/Vs)	903
Mobility degradation parameter, σ	1.5
Mobility degradation coefficient, θ	15
Velocity saturation parameter, η	4.14
Channel length modulation parameter, κ	1×10^{-5}

[a]Reference 39.

The numerical solution of (10) provides a smooth transition in the threshold regime, which is further confirmed by continuous g_m, producing distinct peaks near the threshold point [Fig. 4(b)]. The incorporation of interface trap charge is essential in evaluating subthreshold performance metrics, as portrayed in Fig. 4(c). The threshold voltage in DIBL evaluation is extracted from the I_D–V_G plot at a constant current level of 2 μA/μm due to high drain junction leakage current. The subthreshold slope (SS) obtained from the inverse of the steepest slope of transfer characteristics and DIBL at different gate lengths falls in the range of reported data, providing a precedent for comparing off-state performance of next generation GAA transistors.

The output characteristics of the GAA transistor match well with the published report[19] in both linear and saturation regimes. From Fig. 5(a), it can be seen that an on-resistance of 1160 Ω μm is obtained from the initial slope of the I_D–V_D curve at V_{GS} = 2 V. The continuity of the output characteristics is reflected from the gradual transition in output conductance, as illustrated in Fig. 5(b).

Before delving into the scaling properties of GAA transistors, the degree of SCE affecting such devices are explored semi-analytically in both on and off states. Double-gate MOSFETs suffer from severe SCEs as the W/L ratio approaches unity.[40] Gate-all-around MOSFETs, on the other hand, provide better off-state performance in this regard, with DIBL and SS demonstrating roughly a proportional variation with the W/L ratio. As shown in Fig. 6, for the range of fin width shown in Table I, the maximum W/L ratio studied was 0.8 after which the DIBL and SS stray away from the linear relation. The impact of SCE on the subthreshold slope is even more at higher drain bias, which is evident from the sparsity of SS from the best fit linear graph in Fig. 6(b). The scaling behavior of drain

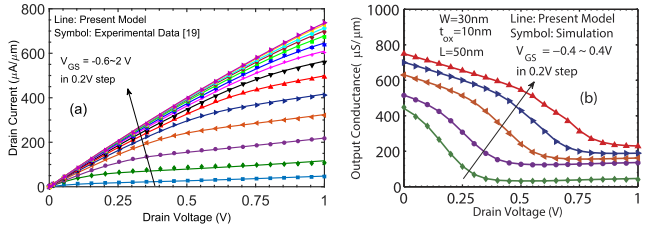

FIG. 5. (a) Output characteristics of a 50 nm GAA MOSFET. An R_{on} of 1160 Ω μm is obtained from the slope at V_{GS} = 2 V. (b) Output conductance of the same device, showing that drain current remains continuous from the linear to the saturation region. Experimental data have been extracted from Ref. 19.

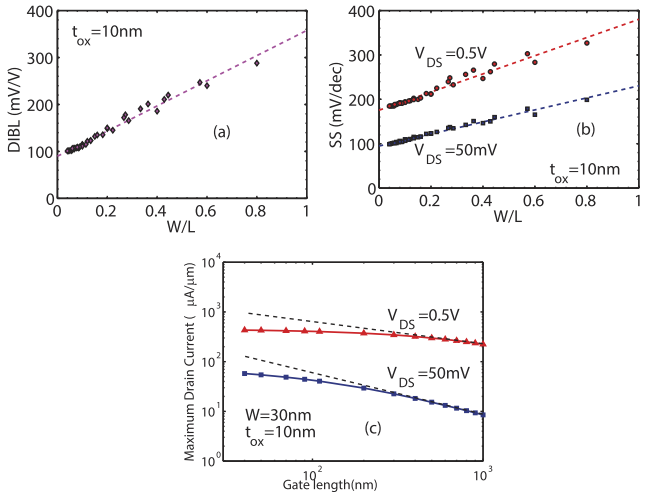

FIG. 6. On-state and off-state characteristics of an InGaAs GAA transistor. Variation in (a) DIBL and (b) SS with the W/L ratio. Best fit straight lines are also plotted based on least square regression to highlight the proportional relation with W/L. (c) Maximum on-current as a function of gate length obtained at V_{GS} = 2 V and different drain biases. For comparison, the dotted line shows when the drain current starts to saturate due to non-ideal effects in the short channel MOSFET.

current in the on-state of the transistor is displayed by tracing the maximum drain current from submicron to long channel lengths, as shown in Fig. 6(c). In the absence of non-ideal effects, the GAA transistor could reach drain current as high as 1 mA/μm at a gate length of around 40 nm. However, saturation induced by the SCE limits the channel current from reaching near ideal values.

The proposed model accurately describes the transport phenomenon of III–V channel devices with scaling of physical process parameters. The transfer characteristics of III–V GAA MOSFETs for various fin widths are presented in Fig. 7. The saturation levels of the normalized drain current in the strong inversion region is less dependent on fin width, although fin width scaling affects threshold characteristics strongly and indicates an improvement in threshold behavior by shifting the transition from threshold to weak inversion to the right. This is attributed to volume inversion of the III–V channel caused by confinement of charge carriers at sub-nanometer

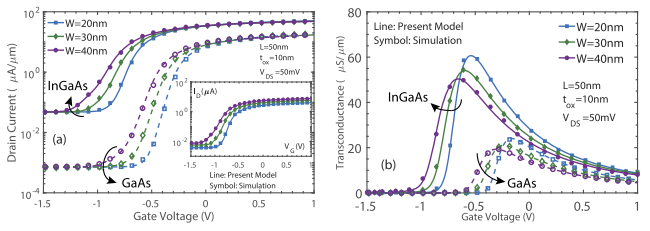

FIG. 7. Transfer characteristics of III–V channel GAA MOSFETs for various fin widths having $N_A = 2 \times 10^{16}$ cm^{-3}. (a) Normalized drain current as a function of gate voltage. The inset figure is for InGaAs GAA MOSFETs, showing that the total current of the wider nanowire is more, as expected. (b) Transconductance as a function of gate voltage. The solid lines and closed symbols are for InGaAs channel material, whereas the dashed lines and open symbols are for GaAs.

dimensions, which otherwise would require further reduction in fin width for silicon technology. The GaAs gate-all-around MOSFET has a lower off-current and better I_{on}/I_{off} ratio, arising from larger effective mass along the transport direction than InGaAs, which suppresses the drain-junction leakage current.[41] On the contrary, the lower saturation current of similar GaAs devices in the strong inversion region can be elaborated by the proportional dependence of drive current (I_D) on the product of channel mobility and inversion capacitance (μC_{inv}).[42] Although the larger density of states favors GaAs devices with a greater inversion capacitance, it is offset by the lower channel mobility of the GaAs channel, resulting in a low on-state current, as depicted in Fig. 7(a). These results are in coherence with previous reports, thus corroborating the efficacy of the proposed model in determining the scaling trend of physical dimensions for a range of III–V compounds as channel materials in GAA transistors. The inset figure reveals the finding that that the total current of a wider nanowire MOSFET is more, as expected, due to increased surface carriers near the oxide/semiconductor interface. There is only a slight increase in the g_m peak for both InGaAs and GaAs channels, as evidenced from Fig. 7(b), which can be further enhanced by scaling to deca-nanometer dimension, the analysis of which is restricted from the proposed model due to negligence of quantum effects.[20] Nevertheless, the excellent match between numerical simulations having a quantization model and analytical results justify the relaxation of quantum effect incorporation into the proposed model for the range of dimension under study.

Figure 8 explores the trend in transfer characteristics with oxide thickness variation. For the sake of benchmarking, an initial oxide thickness of 10 nm was used for a gate length of 50 nm, resulting in an EOT of 4.5 nm, which is much larger than the ITRS guideline for device dimension.[43] However, we explored the trend of oxide scaling with EOT around 1 nm in compliance with the proposition of

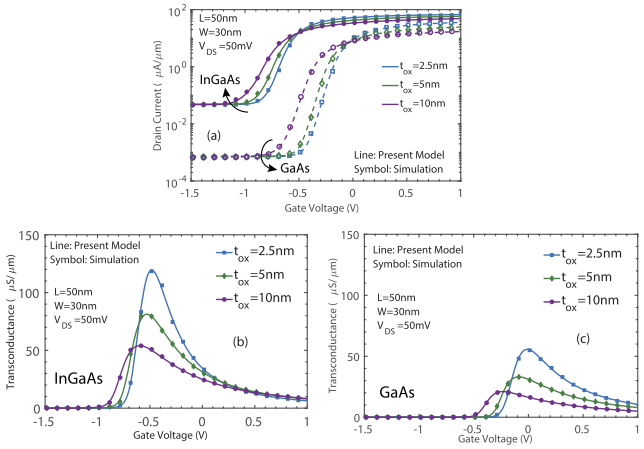

FIG. 8. Transfer characteristics of the III–V channel GAA MOSFET for various oxide thicknesses having $N_A = 2 \times 10^{16}$ cm^{-3}. (a) Drain current as a function of gate bias. The cross-over of the curves indicates an invariant point where the effect of oxide thickness variation due to process limitation is minimized. The solid lines and closed symbols are for the InGaAs channel material, whereas the dashed lines and open symbols are for GaAs. (b) Transconductance as a function of gate bias for the InGaAs GAA MOSFET. (c) Transconductance as a function of gate bias for the GaAs GAA MOSFET.

ITRS. It was found that increasing the gate oxide thickness induces a reduction in channel current, besides lowering the threshold voltage. The existence of a cross-over in the transfer characteristics was previously observed for long channel devices with a wrap-around gate.[44] This phenomenon is extant in short channel transistors as well, regardless of the III–V channel material, occurring near the threshold region of doped nanowire MOSFETs, and serves as an invariant point, particularly important where oxide thickness variation could not be strictly controlled due to process limitations. The g_m peak increases by 2.4 times by reducing the gate dielectric thickness from 10 nm to 2.5 nm, as portrayed in Figs. 8(b) and 8(c). This highlights a potential scope for EOT scaling, which, alternately, can be achieved by introducing high-κ dielectrics into the MOS transistor.

Figure 9 gives us an elaborate comparative analysis of the impact of dimension scaling on the subthreshold performance of GAA nanowire MOSFETs. Due to the presence of SCE, the minimum gate bias required for turning on the MOSFET is lowered as the channel length is scaled down. From Figs. 9(a) and 9(d), it is observed that fin width causes a greater threshold voltage roll-off at sub-nanometer gate lengths. The loss of gate control over electrostatic charges in thicker nanowire means that threshold voltage decreases drastically with gate length reduction. The effect of scaling on DIBL for various fin width and oxide thicknesses is displayed in Figs. 9(b) and 9(e). The effect of DIBL is severe for nanowires with a larger fin width, which is particularly inherited from the aggravated threshold voltage roll-off described earlier, and only slight improvement is obtained by reduction of fin width to practical limits. On the other hand, a dramatic enhancement of DIBL is identified for GAA MOSFETs with thinner oxide thicknesses. A similar variation in SS is observed from dimension scaling, where the minimum slope of the InGaAs MOSFET is far from the ideal SS of 60 mV/dec. The poor DIBL and SS are attributed to the high interface trap density between the Al_2O_3/InGaAs interface. This could be overcome by stacking the gate oxide with $LaAlO_3$, as was successfully demonstrated in Ref. 3.

It is evident that the ultimate scalability of GAA MOSFETs can be achieved by incorporating high-κ dielectrics having suitable integrability with the channel material. Although ALD Al_2O_3 is reported to have the best interface quality with InGaAs, the performance of such GAA transistors is limited by a poor I_{on}/I_{off} ratio resulting from high drain junction leakage current. The switching efficiency (Q = gm/SS) is an important figure of merit to quantify the potential of inserting III–V channel material in CMOS technology that evaluates the I_{on}-vs-I_{off} metric to capture the trade-off between dynamic switching speed and standby power.[45] The incorporation of $LaAlO_3$ or HfO_2 results in better switching efficiency, as clarified by Fig. 10. A high D_{it} of 12 $\times 10^{12}/cm^2eV$ at ~ 0.15 eV below the conduction band was adopted for HfO_2 from published reports into the analytical framework.[46,47] Figure 11 illustrates a radar plot comparing the key features and benefits of using HfO_2 over Al_2O_3 as the gate dielectric. At low drain bias, the subthreshold behavior is remarkably improved by replacing the gate oxide with HfO_2, reducing DIBL, subthreshold slope, and threshold voltage roll-off to a greater extent. An increase in I_{max} indicates the superior current drivability in the on-state of the GAA transistor with a high-κ dielectric. A switching figure of merit Q(=g_m/SS) of 0.82 (μs/μm)/(mV/dec) is obtained from using HfO_2, resulting in an improvement of 2.5 times over Al_2O_3. The high switching efficiency indicates InGaAs MOSFETs as a potential candidate for switching application and logic devices.

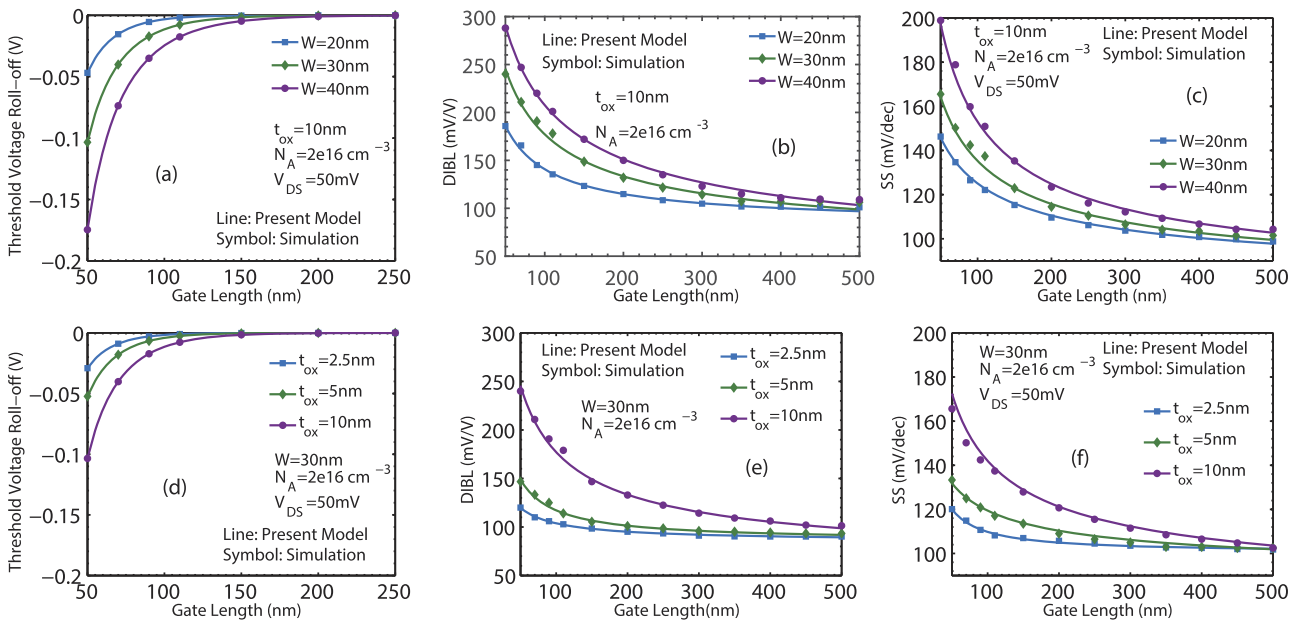

FIG. 9. (a) Threshold voltage roll-off, (b) drain induced barrier lowering, and (c) subthreshold slope degradation due to gate length scaling at various fin widths. (d) Threshold voltage roll-off, (e) drain induced barrier lowering, and (f) subthreshold slope degradation due to gate length scaling at various oxide thicknesses. The subthreshold properties are affected to a greater extent due to fin width variation.

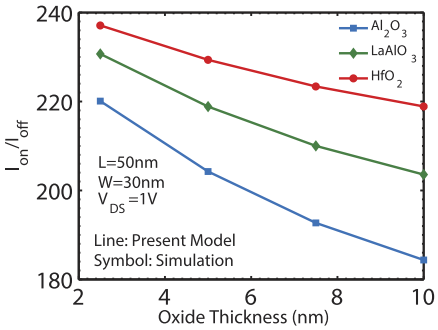

FIG. 10. I_{on}/I_{off} ratio as a function of oxide thickness for various gate dielectrics. $I_{on(off)}$ is defined as the drain current at maximum (minimum) V_{GS} and high drain bias. The high drain junction leakage current of InGaAs GAA MOSFETs results in a small on–off ratio.

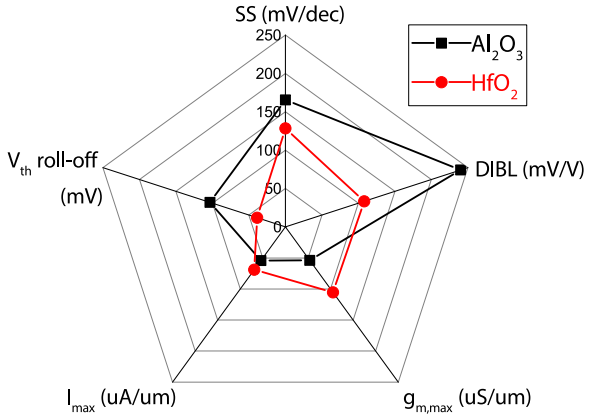

FIG. 11. I_{on}/I_{off} ratio as a function of oxide thickness for various gate dielectrics. $I_{on(off)}$ is defined as the drain current at maximum (minimum) V_{GS} and high drain bias. The high drain junction leakage current of InGaAs GAA MOSFETs results in a small on–off ratio.

V. CONCLUSION

A capacitance–voltage and analytical drain current model is proposed in this work, catered for InGaAs with inclusion of interface defects and trap charges existing near the oxide/semiconductor interface. Certain non-ideal effects are included to emulate the SCEs in ultrascaled transistors. The model parameters have been calibrated with published reports based on symmetric InGaAs MOSFETs. An extensive analysis of the GAA transistor is presented with variation in physical process parameters. Subthreshold performance metrics such as threshold voltage roll-off, DIBL, and subthreshold slope have been thoroughly investigated. Furthermore, the benefits of EOT scaling and integration of a high-κ dielectric are explored to realize the scalability of GAA MOSFETs in the sub-nanometer domain, making them a potential candidate for switching and logic applications. The analysis presented in this work will provide the necessary platform for examination of more complex nanosheet structures.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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