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Analytical Modeling of Threshold Voltage for a Biaxial Strained-Si-MOSFET

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Abstract

In this paper, an attempt has been made to model threshold voltage of biaxial strained silicon MOSFET in one dimension. The results show that a significant amount of threshold voltage decrease has been observed with the increase in the germanium content in the silicon. The results have also been compared with the reported results. The results compare well with the existing reported work.

Keywords: SiGe, strained -Si, technology CAD, energy quantization.

1 Introduction

CMOS technology has contributed significantly to the microelectronics industry thus playing an important role in the overall development of all the countries. The performance and density of a CMOS chip can be improved through device scaling which is inevitable as also propounded by Moore law which says

that the transistor density on a CMOS chip doubles approximately after every one and a half years [1, 2]. Continuing with the Moore law, the gate length of the MOSFET will eventually shrink to 10 nm in 2015 [1,2]. Seeing the trend of down scaling, continuous improvements in the VLSI MOSFET device models are required so that the exact behavior of deep sub-micron and nanometer scaled MOSFETs can be described with accuracy. MOSFET physics and modeling is facing difficulties to achieve accurate description of such scaled down devices. The reason is that many complicated new phenomena are arising, such as, reduction in carrier mobility and failure of classical physics in the nanoscale MOSFETs etc. The accurate modeling of these adverse effects and their remedial actions is very much required. But as we scale down the MOSFET, carrier mobility decreases due to the high vertical electrical fields in the substrate. This reduces the speed of the device. To control these effects, strained silicon technology has evolved in the past few years as a replacement to silicon in substrate and also in poly-gate.

The paper is organized as follows. Section 2 deals with the physics of strained silicon MOSFET. Section 3 deals with the threshold voltage modeling for strained silicon MOSFETs. Section 4 gives results and discussions. Conclusions are given in section 5.

2 Physics of strained MOSFETs

When a layer of a crystal is grown over another layer, a strain is developed in the upper layer due to the mismatch of the lattice constants of two layers. This process yields high speeds without scaling down the devices. The strain is a very useful parameter in devices as carrier mobility significantly increases by altering the band structure at the channel. The alteration of band structure in the channel layer provides lower effective mass and also suppresses intervalley scattering which is a prime cause of enhancement of carrier mobility and the drive current. The mobility becomes roughly twice as that of conventional Si substrate [3]. The conduction band splitting has been shown in Fig.1. Each energy level of silicon is composed of six equal energy states in three dimensions. These are named as two perpendicular Δ_2 (k_z) states and four Δ_4 (k_x and k_y) states parallel to the plane. These energy states have equal electron effective masses in all the directions. When biaxial stress is applied, the Δ_2 states and Δ_4 states are split up into lower and higher energy states respectively. This band alteration gives an alternate lower energy site for electrons to reside i.e. Δ_2. The difference in the energy levels causes repopulation of the electrons in the lower energy states Δ_2. The effective mass of electrons in the Δ_2 valley is lesser than the Δ_2. The effective mass of electrons in lower energy states is reduced from $0.33m_o$ in unstrained silicon to $0.19m_o$ in strained silicon structures [4]. Due to this, the electron mobility increases. Besides this, the inter-valley phonon scattering between the lower and upper states is suppressed due to the strain induced larger energy difference. The mathematical equation (1) proves this theory.

Mathematically, carrier mobility

$$\mu = q\,\tau/m^* \quad (1)$$

Where, $1/\tau$ = scattering rate, m^* = conductivity effective mass.

The mobility is directly related to the carrier velocity 'v' and applied external electric field 'E' as shown by (2):

$$v = \mu . E \quad (2)$$

It can be seen that increasing the carrier mobility increases the velocity, which is directly proportional to the switching speed of the device and the drain current.

This process is especially useful at nanometer scales where the carrier mobility is affected the most as explained earlier in section I also.

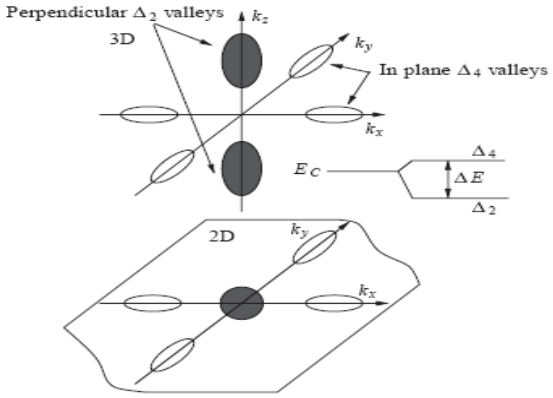

Fig 1: Energy band splitting due to biaxial strain in conduction bands

3 Strained silicon modeling

The effect of strain in terms of equivalent Ge mole fraction, strained-silicon thin film doping and thickness, energy quantization has been included to model the threshold voltage. The accuracy of the proposed analytical model is verified by comparing the model results with the reported numerical results. It has been demonstrated that the proposed model correctly predicts a decrease in threshold voltage with increasing strain in the silicon thin film, i.e., with increasing equivalent Ge concentration. The few models available in literature are related to the threshold voltage of bulk strained-Si/SiGe MOSFETs [5, 6] that are obtained by modifying the long channel threshold voltage model.

Threshold voltage modeling

In this paper, we have solved all these equations analytically and no approximations have been used. First parameter in solving these equations is the surface electrical field.

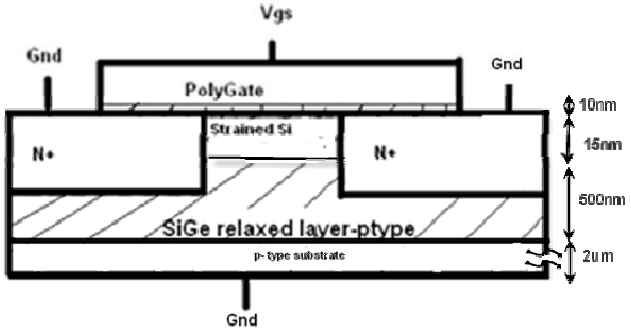

Fig 3: Cross-sectional view of biaxially strained-Si–SiGe bulk-Si MOSFET

a) Calculation of depletion ion density

The depletion charge density is given by

$$Q_{depl} = qN_a x_d \tag{3}$$

x_d= Depletion width in the substrate. x_d is calculated as: Dividing the MOS substrate region in three parts such as:

1. p-type silicon /silicon germanium interface
2. Silicon germanium interface/strained silicon layer interface
3. Strained silicon / oxide layer interface

Hetero-interface I: p-type substrate and the SiGe relaxed layer p-type

The depletion region extends in the p-type substrate and the SiGe relaxed layer. Let the thickness of SiGe relaxed layer is x_{SiGe} and the depletion region in the p-type substrate is x_s. Applying Poisson equation at this interface, for getting the potential distribution in the substrate and keeping substrate at zero bias, we get in the limits from $0 < x < x_d$ towards the oxide.

$$d^2\varphi / dx^2 = qN_a / \varepsilon_o\varepsilon_{si} \tag{4}$$

Integrating (4), by applying boundary conditions, we get, the electrical field at the interface I is given by

$$d\varphi / dx = -E_{Si} = qN_a x_d / \varepsilon_o\varepsilon_{si} \tag{5}$$

$$\varphi_1(x) = qN_a x^2 / 2\varepsilon_o\varepsilon_{si} \tag{6}$$

$$V_{fbs} = \varphi_m - \{\chi_s + E_g^{sige} - V_t \ln\left(N_v^{sige} / N_a\right)\}$$

At $x = x_d$,

$$\varphi_1(x_d) = qN_a x_d^2 / 2\varepsilon_o\varepsilon_{si} \tag{7}$$

is the potential at the substrate and SiGe relaxed layer hetero-interface. This can be called at the top of the substrate or at the bottom of the SiGe relaxed layer.

Hetero-interface II: SiGe relaxed layer p-type and p-type Strained Si

The SiGe relaxed layer is assumed to be of constant electrical field and hence no depletion region exists in this area. The electrical field in the hetero interface I is same as at hetero interface II. The electrical field is given in (5). Solving Poisson equation in the SiGe relaxed layer. Integrating (5) in the SiGe channel, from $x=x_d$ to $x = x_d + x_{SiGe}$, and putting boundary conditions for the potential φ_2, we get,

$$\varphi_2(x) - \varphi_1(x_d) = qN_a x_d x / \varepsilon_o \varepsilon_{si}$$
$$\varphi_2(x_{SiGe} + x_d) = qN_a x_d^2 / 2\varepsilon_o \varepsilon_{si} + qN_a x_d x_{SiGe} / \varepsilon_o \varepsilon_{si} \quad (8)$$

Hetero-interface III: p-type Strained Si and silicon oxide

The electrical field at the bottom of strained silicon cap layer is same as given by (5) due to continuity of electrical fields at the hetero interface III. The electrical field at the strained silicon/oxide interface is calculated. Integrating (5) in the SiGe channel, from $x=x_d$ to $x=x_d + x_{SiGe} + x_{ssi}$, and putting boundary conditions for the potential φ_3 we get,

$$\varphi_s(x) - \varphi_1(x_d) = qN_a x_d x / \varepsilon_o \varepsilon_{si}$$
$$\varphi_s(x_d + x_{SiGe} + x_{ssi}) = qN_a x_d x_{ssi} / \varepsilon_o \varepsilon_{si} + qN_a x_d^2 / 2\varepsilon_o \varepsilon_{si} + qN_a x_d x_{SiGe} / \varepsilon_o \varepsilon_{si} \quad (9)$$

Now, $\varphi_3(x_d + x_{SiGe} + x_{ssi})$ is the surface potential which is constant and is equal to

$$\varphi_{ss} = 2\varphi_f - \Delta E_C(x) \quad (10)$$

Where $\Delta E_C(x)$ is the conduction band offset due to strain in the lattice and φ_f is the Fermi potential, a parameter, which is a function of doping. $\varphi_f = kT/q \ln(N_a/n_i)$, n_i= intrinsic carrier concentration $= (N_c N_v)^{1/2} \exp(-E_g / 2kT)$

Equating (9) and (10) and solving the quadratic equation, we get the maximum depletion width in the substrate.

$$x_d = -(x_{SiGe} + x_{ssi}) + \{(x_{SiGe} + x_{ssi})^2 + 2(\varphi_{ss}\varepsilon_{si} / qN_a)\}^{1/2} \quad (11)$$

Using (11) in (3), we get the depletion charge density.

$$V_{Ts} = V_{fbs} + \varphi_{ss} + \varphi_{oxs} \quad (12)$$

Flat band voltage for a metal gate strained silicon MOSFET is hence given by [6].

$$V_{fbs} = \varphi_m - \{\chi_s + E_g^{sige} - V_t \ln(N_v^{sige} / N_a)\} \quad (13)$$

$$T_{ox} = 1.4\ nm$$

$$x_{sige} = 4\ nm$$

χ_s = 4.35+0.58*x*, N_v^{sige}=1.04+x (0.6– 1.04)*10^{19} cm^{-3} , φ_{ss} =2 φ_f - ΔE_g , E_g -ΔE_g = E_g^{sige} , E_g =1.12 eV , ΔE_g = 0.4*x*, φ_{oxs} = $qN_a x_d/C_{ox}$ obtained from (6). So, using (13) and (10) and (3) in (12), we get the threshold voltage for strained silicon MOSFET.

4 Results and discussion

We have modeled the one dimensional threshold voltage for the strained silicon/SiGe MOSFET for various device parameters. Figure 3 shows the variation of threshold voltage with Ge mole fraction in the relaxed SiGe buffer and for a strained-silicon thickness. It shows a clear fall in threshold voltage with the increase in germanium mole fraction. The parameters used are oxide thickness (T_{ox})= 1.4nm, Ge (x=0.2), strained silicon thickness (x_{ssi})=4.0nm. The figure 4 and 5 show an increase of threshold voltage with the thickness of strained silicon layer and the relaxed silicon germanium layer. Figure 6 shows the comparison of strained silicon and unstrained silicon threshold voltage. The threshold voltage for strained silicon MOSFET is lesser as compared to the unstrained one.

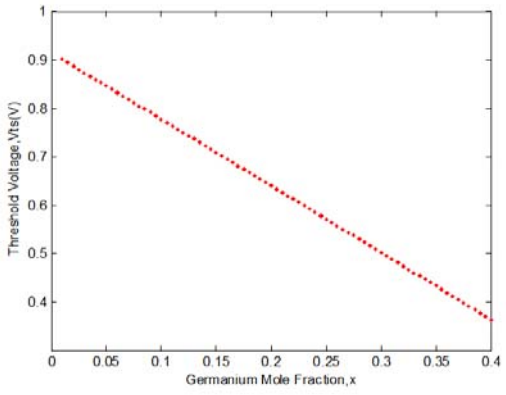

Fig 3: Variation of threshold voltage of strained-Si n-MOSFETs with germanium

mole fraction (x)

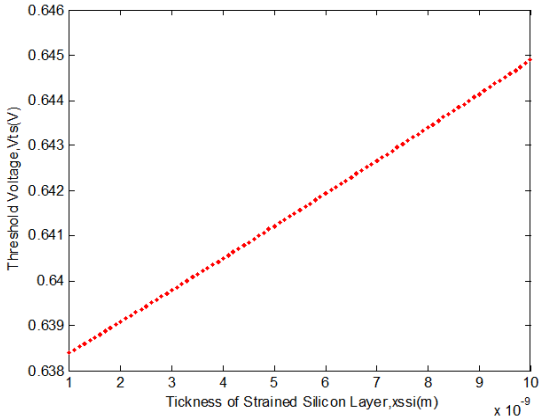

Fig 4: Variation of threshold voltage of strained-Si n-MOSFETs with thickness of strained silicon layer (xssi)

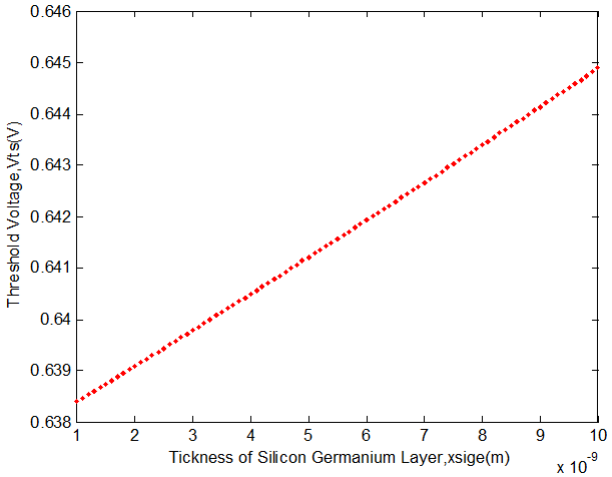

Fig 5: Variation of threshold voltage of strained-Si n-MOSFETs with thickness of silicon germanium layer (xsige)

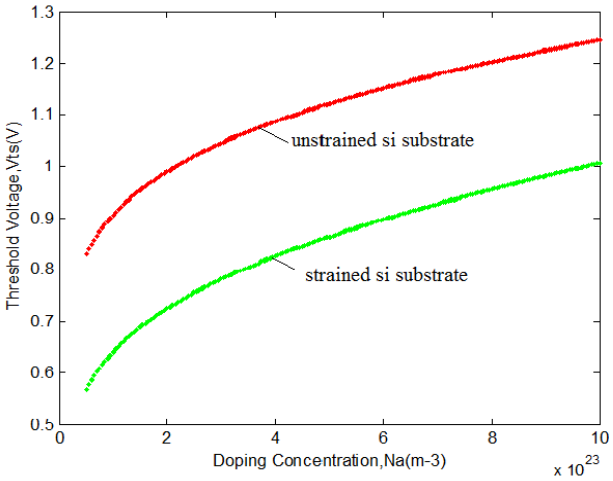

Fig 6: Variation of threshold voltage of strained and unstrained-Si n-MOSFETs

with doping concentration (Na). The parameters are oxide thickness (T_{ox})= 1.4nm, Ge (x=0.2), strained silicon thickness (x_{ssi}) and x_{sige} =4.0nm

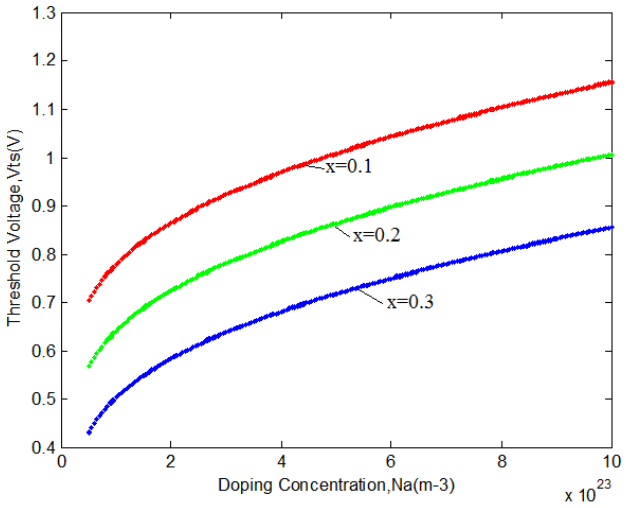

Fig 7: Variation of threshold voltage of strained-Si n-MOSFETs with doping concentration (Na) at different values of germanium mole fraction (x).

Figure 7 shows the variation of threshold voltage with doping concentration and Ge mole fraction as a third variable. It shows a clear fall in threshold voltage with the increase in germanium mole fraction. The parameters used are oxide thickness (T_{ox})= 1.4nm, strained silicon thickness (x_{ssi}) and x_{sige}=4.0nm. Figure 8 shows the validation of the results obtained with the reports results [5]. Similarly figure 9 and 10 validate our results with existing numerical and experimental results [6], thus proving the accuracy of the model developed.

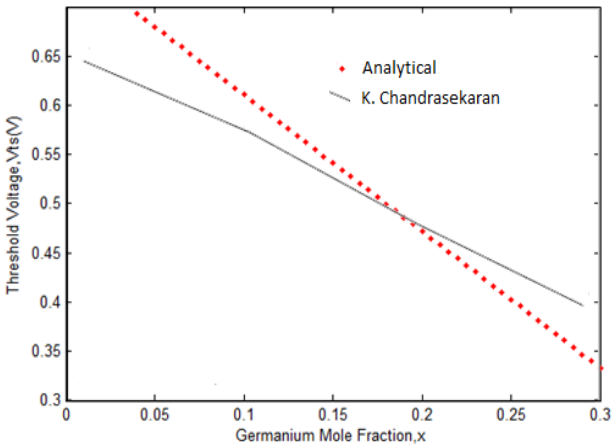

Fig 8: Variation of threshold voltage of strained-Si n-MOSFETs with germanium mole fraction (x). The parameters are oxide thickness (T_{ox})= 0.6nm, strained silicon thickness (x_{ssi}) and x_{sige} =4.0nm

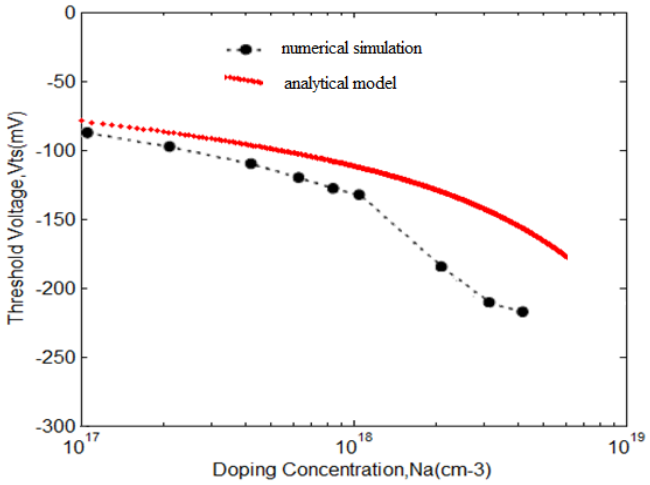

Fig 9: Analytical and simulated threshold voltage versus doping concentration. The difference increases with increased doping concentration. The parameters are oxide thickness (T_{ox})= 1.0nm, Ge (x=0.2), strained silicon thickness (x_{ssi}) and x_{sige} =5.0nm and 4.0nm respectively.

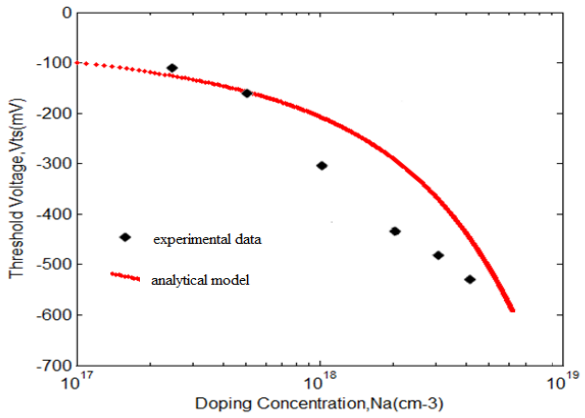

Fig 10: Threshold voltage difference versus doping concentration, comparing the analytical model of this work, with experimental data, demonstrating close agreement. The parameters are oxide thickness (T_{ox})= 5.0nm, Ge (x=0.2), strained silicon thickness (x_{ssi}) and x_{sige} =10.0nm and 4.0nm respectively.

5 Conclusion

The compact threshold voltage model for the strained silicon/SiGe MOSFET has been developed and studied the effect of various device parameters such as 1) strain (in equivalent Ge mole fraction in the relaxed SiGe buffer), 2) strained-silicon thin-film doping, and 3) strained-silicon thin-film thickness. The 1-D Poisson equation is solved in the strained-Si thin film using appropriate boundary conditions. The model results are compared with reported simulated and experimental results in the literature. There is a significant drop in threshold voltage with increasing strain.

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