ANALYTICAL MODELING OF THRESHOLD VOLTAGES IN p-CHANNEL Si/SiGe/Si MOS STRUCTURES

K. Iniewski, S. Voinigescu, J. Atcha and C. A. T. Salama

Department of Electrical Engineering, Toronto, Ontario, Canada M5A 1A4

Abstract—An analytical model for the threshold voltages in a Si/SiGe/Si MOS structure is presented. It offers very good accuracy as compared to results of one- and two-dimensional numerical simulations. It is shown that short-channel effects lower the threshold voltage of the SiGe channel and increase the threshold voltage for parasitic conduction in the Si-cap layer. The model can serve as a useful tool for p-channel Si/SiGe/Si MOSFET design.

NOTATION

C_{ox}	gate oxide capacitance per unit area
$H(\phi)$	contribution of holes to the electric field in the SiGe film
k	Boltzmann constant
L_{eff}	effective channel length
n_i	intrinsic carrier concentration
N_B	doping concentration in the bulk of the semiconductor
N_B^*	effective doping concentration in the bulk of the semiconductor
N_{vSi}	valence band density of states in silicon
N_{vSiGe}	valence band density of states in SiGe
p	hole concentration
p_H	hole concentration at the top heterointerface
p_S	hole concentration at the surface
q	electron charge
Q_f	fixed oxide charge at the Si-SiO$_2$ interface
Q_H	charge in the buried channel
Q_S	charge in the surface channel
R_ϵ	ratio of semiconductor permittivities in silicon and SiGe respectively
T	temperature
V_{bi}	build-in voltage of the drain-substrate p-n junction
V_D	drain voltage
V_D^*	effective drain voltage
V_G	gate voltage
V_{TH}	threshold voltage at the top SiGe/Si heterointerface
V_{TS}	threshold voltage at the silicon cap surface
x	Ge content in the SiGe film
x_{buff}	silicon buffer thickness
x_{cap}	silicon cap thickness
x_d	depletion layer width
x_{ox}	gate oxide thickness
x_{sige}	SiGe film thickness
ΔE_c	conduction band offset between SiGe and Si
ΔE_v	valence band offset between SiGe and Si
ΔV_T	gate voltage window
ϵ_{ox}	SiO$_2$ permittivity
ϵ_{Si}	silicon permittivity
ϵ_{SiGe}	SiGe permittivity
ϕ	potential
ϕ_F	Fermi potential
ϕ_H	potential at the top heterointerface
ϕ_{TH}	potential at threshold at the top heterointerface
ϕ_S	potential at the surface
ϕ_{TS}	potential at threshold at the surface
ϕ_{MS}	work function difference between the gate and the silicon substrate

1. INTRODUCTION

The application of SiGe alloys to bipolar and field-effect silicon devices can significantly improve their performance while maintaining compatibility with conventional silicon processing[1–5]. MOSFETs based on Si/SiGe/Si substrates offer higher hole mobility and higher resistance to hot electrons than their silicon counterparts[2–5]. Carrier transport in these devices takes place in an induced buried channel at the Si/SiGe heterointerface. In addition, at higher gate voltages parasitic conduction at the Si/SiO$_2$ interface occurs. For optimum device design the conduction in the parasitic channel has to be minimized.

Successful fabrication of p-channel Si/SiGe/Si MOSFETs has recently been reported[2–6]. However, no analytical expressions for the threshold voltages of the Si/SiGe/Si MOSFET are available in the literature. It is the purpose of this paper to present analytical expressions for the threshold voltages at which buried and parasitic surface channels start to conduct drain current and to show how optimum channel design can be achieved. The analytical model was derived from Poisson's equation and compares very well with the results of numerical simulations.

The paper is organized as follows. In Section 2 the analytical model is presented. First the conditions for the strong inversion at both interfaces are defined. Then Poisson's equation is solved for the one-dimensional case. Further, the solution is extended to the two-dimensional case to account for short-channel effects by using the voltage-doping transformation which was introduced in the analysis of short-channel silicon MOSFETs[7]. The analytical model is compared to the results of one- and two-dimensional numerical simulations in Section 3. Based on the model predictions an optimum vertical structure for p-channel Si/SiGe/Si MOSFETs is proposed. Finally, conclusions are given in Section 4.

2. ANALYTICAL MODEL

A cross section through the *p*-channel Si/SiGe/Si MOS structure is shown in Fig. 1. In the analysis it is assumed that the silicon cap layer, the SiGe film and the silicon buffer are undoped. The doping in the *n*-type substrate N_B is assumed uniform, germanium concentration in the SiGe film is constant and the film is considered fully strained.

For very small drain voltages V_D and long MOSFET channel, an analysis can be carried out in one dimension perpendicular to the surface. For negative voltages V_G applied to the gate, the silicon *n*-type substrate is depleted and the width of the depletion layer is denoted as x_d (Fig. 1). Depending on the gate voltage, strong inversion conditions can be induced at both the top Si/SiGe heterointerface and at the silicon surface or only at one of them. For a properly designed structure strong inversion at the top Si/SiGe heterointerface must occur first. In this case a buried channel is formed for hole conduction between source and drain. The hole mobility in this channel is expected to be larger than in silicon due to strong hole confinement and reduced surface roughness scattering. However, when strong inversion occurs at the surface, the parasitic surface channel is turned on and the advantages of the Si/SiGe/Si structure are lost to a large degree. In this region of operation both channels conduct current, but the gate voltage modulates mainly the parasitic surface channel. It is therefore desirable to design the device structure in such a way that parasitic surface

conduction is minimal. To provide design guidelines the conditions for channel formation are derived first.

2.1. Conditions for strong inversion

The gate voltage which causes strong inversion at the top Si/SiGe heterointerface is denoted as the heterointerface threshold voltage V_{TH}. The condition for the onset of strong inversion is defined, in a similar manner as for conventional MOS structures, as the gate voltage at which the concentration of minority carriers (holes in this case) is equal to the substrate doping concentration N_B. This leads to the following condition for the threshold potential ϕ_{TH} at the top heterointerface

$$\phi_{TH} = 2\phi_F + \frac{\Delta E_v}{q} - \frac{kT}{q} \ln\left(\frac{N_{vSi}}{N_{vSiGe}}\right) \qquad (1)$$

where $\phi_F = -kT/q \ln(N_B/n_i)$ is the Fermi potential in the bulk, ΔE_v is the valence band offset between SiGe and Si, N_{vSi} and N_{vSiGe} are the densities of states in the valence band for silicon and SiGe, respectively.

The gate voltage which causes strong inversion at the surface is denoted as the surface threshold voltage V_{TS}. The condition for the onset of strong inversion at the surface is defined, in a similar manner, as the gate voltage at which the minority carrier concentration at the surface is equal to the substrate doping concentration. The threshold surface potential ϕ_{TS} for strong inversion at the surface is given by

$$\phi_{TS} = 2\phi_F. \qquad (2)$$

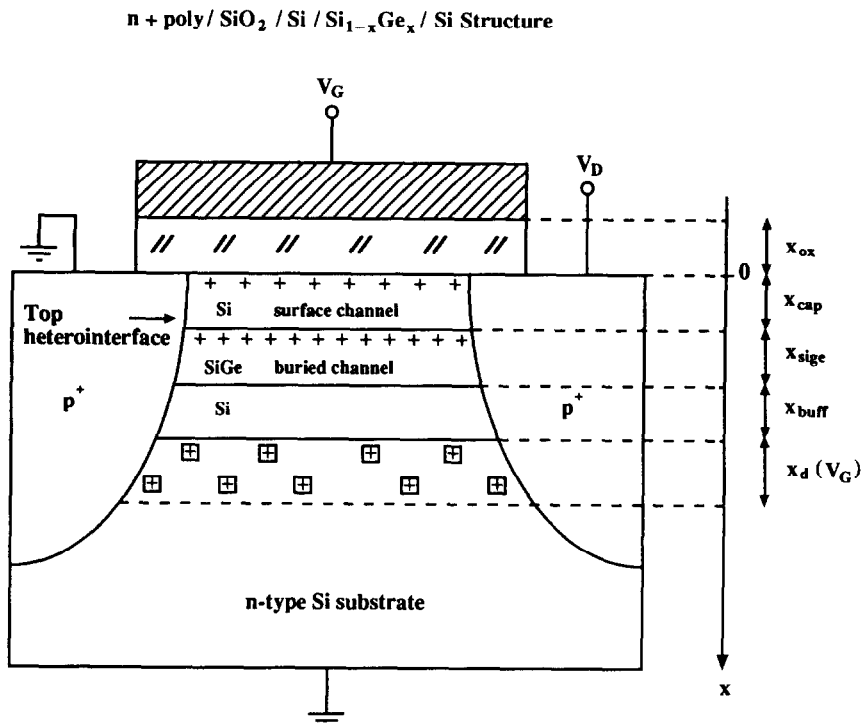**n + poly/ SiO$_2$ / Si / Si$_{1-x}$Ge$_x$ / Si Structure**

Fig. 1. Cross section through the Si/SiGe/Si MOSFET structure. For large negative gate voltage V_G both buried and parasitic surface channels are available for conduction between source and drain.
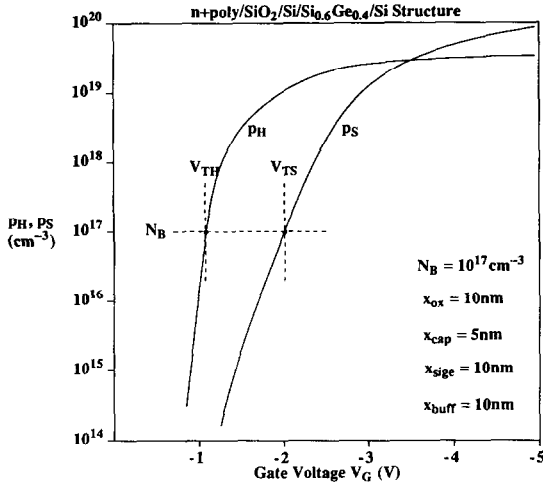
Fig. 2. One-dimensional numerical simulation of hole concentration at the top heterointerface p_H and at the surface p_S as a function of gate voltage V_G. The definition of the threshold voltages at the heterointerface V_{TH} and at the surface V_{TS} is illustrated.

The definition of both threshold voltages is illustrated in Fig. 2 where the hole concentration at the heterointerface $p_H = p(x = x_{cap})$ and at the surface $p_S = p(x = 0)$ are plotted as function of gate voltage. In addition, a dependence of the hole charge in the buried channel Q_H and in the surface channel Q_S on the gate voltage V_G is shown in Fig. 3 indicating that the chosen definition of the threshold voltages directly corresponds to the gate voltages at which both channels are available for conduction.

2.2. Threshold voltages for long-channel devices

To derive the expressions for the threshold voltages V_{TH} and V_{TS} Poisson's equation has to be solved.
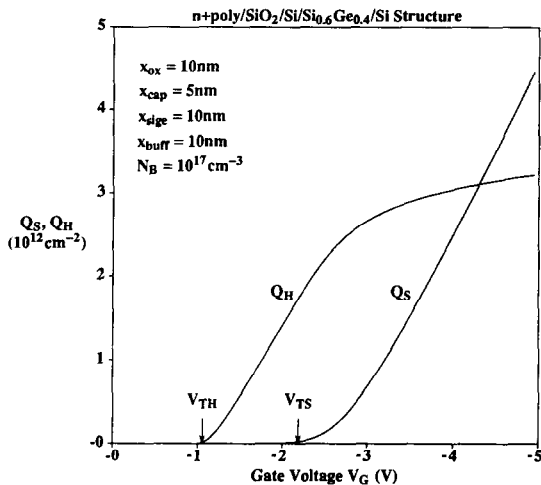

Fig. 3. One-dimensional numerical simulation of hole charge in the buried channel Q_H and in the surface channel Q_S as a function of gate voltage V_G. The threshold voltage at the heterointerface V_{TH} and the threshold voltage at the surface V_{TS} are indicated.

First the analytical solution is obtained for long-channel devices by solving Poisson's equation in the one-dimensional case. Later, the solution is extended to the two-dimensional case for short channel devices.

The analytical solution in the one-dimensional case can be obtained by taking into account the charge in the depletion layer and the hole charge in the SiGe layer. The hole charge in the silicon cap is neglected since, for a properly designed structure, $V_{TH} > V_{TS}$ which means that strong inversion occurs first at the top Si/SiGe heterointerface.

Under these assumptions, the one-dimensional Poisson's equation can be written for each region of the structure as follows

$$\epsilon_{Si} \frac{d^2\phi}{dx^2} = -qN_B,$$

$$x_{cap} + x_{sige} + x_{buff} < x < x_{cap} + x_{sige} + x_{buff} + x_d$$

$$\epsilon_{Si} \frac{d^2\phi}{dx^2} = 0, \quad x_{cap} + x_{sige} < x < x_{cap} + x_{sige} + x_{buff}$$

$$\epsilon_{Si} \frac{d^2\phi}{dx^2} = -qp(x)R_\epsilon, \quad x_{cap} < x < x_{cap} + x_{sige}$$

$$\epsilon_{Si} \frac{d^2\phi}{dx^2} = 0, \quad 0 < x < x_{cap} \tag{3}$$

where x_{buff} is the thickness of the silicon buffer, x_{sige} is the thickness of the SiGe film, x_{cap} is the thickness of the silicon cap layer and $R_\epsilon = \epsilon_{Si}/\epsilon_{SiGe}$ is the ratio of semiconductor permittivities in silicon and SiGe respectively.

The above set of the equations can be solved using the following boundary conditions for the potential

$$\phi \big|_{x = x_{cap} + x_{sige} + x_{buff} + x_d} = 0$$

$$\phi \big|_{x = x_{cap} + x_{sige} + x_{buff}^-} = \phi \big|_{x = x_{cap} + x_{sige} + x_{buff}^+}$$

$$\phi \big|_{x = x_{cap} + x_{sige}^-} = \phi \big|_{x = x_{cap} + x_{sige}^+}$$

$$\phi \big|_{x = x_{cap}^-} = \phi \big|_{x = x_{cap}^+} = \phi_H. \tag{4}$$

From Gauss's law the additional boundary conditions are

$$\frac{d\phi}{dx} \bigg|_{x = x_{cap} + x_{sige} + x_{buff} + x_d} = 0$$

$$\frac{d\phi}{dx} \bigg|_{x = x_{cap} + x_{sige} + x_{buff}^-} = \frac{d\phi}{dx} \bigg|_{x = x_{cap} + x_{sige} + x_{buff}^+}$$

$$\frac{d\phi}{dx} \bigg|_{x = x_{cap} + x_{sige}^-} = R_\epsilon \frac{d\phi}{dx} \bigg|_{x = x_{cap} + x_{sige}^+}$$

$$R_\epsilon \frac{d\phi}{dx} \bigg|_{x = x_{cap}^-} = \frac{d\phi}{dx} \bigg|_{x = x_{cap}^+}. \tag{5}$$

Using these boundary conditions and carrying out a first integration of Poisson's equation the following relations are obtained

$$\epsilon_{Si}\frac{d\phi}{dx} = qN_B(x_{cap} + x_{sige} + x_{buff} + x_d - x),$$

$$x_{cap} + x_{sige} + x_{buff} < x < x_{cap} + x_{sige} + x_{buff} + x_d$$

$$\epsilon_{Si}\frac{d\phi}{dx} = qN_B x_d, \quad x_{cap} + x_{sige} < x < x_{cap} + x_{sige} + x_{buff}$$

$$\epsilon_{Si}\frac{d\phi}{dx} = qN_B x_d R_r \sqrt{1 + H(\phi)}, \quad x_{cap} < x < x_{cap} + x_{sige}$$

$$\epsilon_{Si}\frac{d\phi}{dx} = qN_B x_d \sqrt{1 + H(\phi_H)}, \quad 0 < x < x_{cap} \quad (6)$$

where ϕ_H is the potential at the top SiGe/Si heterointerface as defined in eqn (4). In eqn (6), $H(\phi)$ represents the contribution of holes to the electric field in the SiGe film and is given by

$$H(\phi) = \frac{2\epsilon_{SiGe}N_B kT}{(qN_B x_d)^2}\left[\exp\left(\frac{\phi_{TH} - \phi}{kT/q}\right)\right.$$
$$\left. - \exp\left(\frac{\phi_{TH} - \phi(x = x_{cap} + x_{sige})}{kT/q}\right)\right]. \quad (7)$$

To obtain the potential distribution, a second integration of Poisson's equation is required. To generate an analytical solution the contribution of holes [the $H(\phi)$ term] to the potential drop in the SiGe film is neglected. This approximation introduces a small error as verified by comparison to numerical results presented in the next section.

Using this approximation, the potential at the top heterointerface ϕ_H and the potential at the surface ϕ_S are obtained respectively as

$$\phi_H = \phi(x = x_{cap})$$
$$= -\frac{qN_B}{2\epsilon_{Si}}[x_d^2 + 2x_d(x_{buff} + R_r x_{sige})] \quad (8)$$

and

$$\phi_S = \phi(x = 0) = \phi_H - \frac{qN_B x_d}{\epsilon_{Si}/x_{cap}}\sqrt{1 + H(\phi_H)}. \quad (9)$$

The $H(\phi_H)$ term in eqn (9) represents the contribution of free holes in the SiGe layer to the potential drop across the silicon cap. It is obtained from (7) by dropping the last exponential term, which is negligible, and can be expressed as

$$H(\phi_H) = \frac{2\epsilon_{SiGe}N_B kT}{(qN_B x_d)^2}\exp\left(\frac{\phi_{TH} - \phi_H}{kT/q}\right). \quad (10)$$

By taking into account all potential drops across the structure, an expression for the gate voltage V_G can be written as

$$V_G = \phi_{MS} - \frac{Q_f}{C_{ox}} + \phi_H - qN_B x_d$$
$$\times \left(\frac{x_{cap}}{\epsilon_{Si}} + \frac{x_{ox}}{\epsilon_{ox}}\right)\sqrt{1 + H(\phi_H)} \quad (11)$$

where $C_{ox} = \epsilon_{ox}/x_{ox}$ is the gate oxide capacitance per unit area, x_{ox} is the gate oxide thickness, ϕ_{MS} is the work-function difference between the gate and the silicon substrate and Q_f is the fixed oxide charge at the Si–SiO$_2$ interface.

The expression for V_{TH} can be derived directly from (11) as

$$V_{TH} = V_G(\phi_H = \phi_{TH}) = \phi_{MS} - \frac{Q_f}{C_{ox}} + \phi_{TH}$$
$$- qN_B x_{dmax}\left(\frac{x_{cap}}{\epsilon_{Si}} + \frac{x_{ox}}{\epsilon_{ox}}\right)\sqrt{1 + H(\phi_{TH})}. \quad (12)$$

In eqn (12) the depletion layer width x_d has been replaced by x_{dmax} since in strong inversion the depletion layer width reaches its maximum value. Further changes in gate voltage do not change x_{dmax} due to the screening effect of the strongly inverted layer at the top heterointerface. In this region of operation, the potential at the heterointerface is pinned to ϕ_{TH}. The maximum depletion layer width x_{dmax} can be derived from (8) as

$$x_{dmax} = x_d(\phi_H = \phi_{TH})$$
$$= \sqrt{\frac{2\epsilon_{Si}}{qN_B}(-\phi_{TH}) + (x_{buff} + R_r x_{sige})^2}$$
$$- x_{buff} - R_r x_{sige}. \quad (13)$$

Equation (12) can be simplified by noting that the hole contribution is very small at the onset of strong inversion at the top heterointerface and therefore the $H(\phi_{TH})$ term can be neglected. Under typical conditions this results in a negligible error.

The threshold voltage V_{TS} can be also obtained from (11) but in this case the hole contribution in the buried SiGe channel [the $H(\phi_H)$ term] is important. Using (9) and (11), the threshold voltage V_{TS} can be written as

$$V_{TS} = V_G(\phi_S = \phi_{TS}) = \phi_{MS} - \frac{Q_f}{C_{ox}} + \phi_{TS}$$
$$- \frac{qN_B x_{dmax}}{C_{ox}}\sqrt{1 + H(\phi_H)}. \quad (14)$$

The potential at the top heterointerface ϕ_H needed to calculate V_{TS} is obtained by solving eqn (9) and substituting $\phi_S = \phi_{TS}$, where the ϕ_{TS} potential is given by (2). The solution of this equation requires iteration, but the iteration process converges very quickly if a suitable first guess is provided (for example $\phi_H = \phi_{TH}$).

2.3. Threshold voltages for short-channel devices

As the MOSFET channel length is reduced, two-dimensional effects play an increasingly important role. The extension of the long-channel model derived above to the short channel case is indispensable for Si/SiGe/Si structures with potential applications in submicron MOS technology. Although the Si/SiGe/Si structure differs considerably from the

conventional silicon MOSFET, a similar approach can be used to model two-dimensional effects.

To account for the key effect in short-channel structures, namely the influence of the drain-source lateral field on the potential barrier, the voltage-doping transformation developed for silicon MOSFETs[7] is applied. This approach offers very good modeling accuracy, is physically based and does not involve iterative computations[10].

According to the voltage-doping transformation the relation for the long-channel threshold voltage can be still used for the short channel device if the real doping concentration N_B is replaced by the effective doping concentration N_B^* which is both bias and channel length dependent, as given by the following equation[7]

$$N_B^* = N_B + \frac{2\epsilon_{Si} V_D^*}{q L_{eff}^2}. \quad (15)$$

L_{eff} is the effective channel length, defined as the physical separation between source and drain, and V_D^* is the effective drain voltage (with respect to the source) which, in the absence of substrate bias, is given by[7]

$$V_D^* = V_D - 2(V_{bi} + \phi_{TH})$$
$$- 2\sqrt{(V_{bi} + \phi_{TH})(V_{bi} + \phi_{TH} - V_D)} \quad (16)$$

where V_{bi} is the built-in voltage of the drain-substrate $p-n$ junction. In the limiting case of very small V_D the above equation can be simplified into

$$V_D^* = -4(V_{bi} + \phi_{TH}). \quad (17)$$

The above voltage-doping transformation can be interpreted as follows. As the channel length is reduced, the effect of the drain-source lateral field increases reducing the effective doping concentration as indicated by (15). Note that for a p-channel device V_D as well as V_D^* are negative. As a result of the lower doping concentration, the depletion layer width in the center of the channel increases and the depletion layer charge decreases causing the changes in the threshold voltages.

The threshold voltages V_{TH} and V_{TS} for the Si/SiGe/Si MOSFET can be calculated in the following manner. For the given channel length L_{eff}, the effective doping concentration N_B^* is calculated from (15) using (17). Then in the formulas for the threshold voltages [eqns (9)–(14)] the real doping concentration N_B is replaced by the effective doping concentration N_B^*. With this substitution the threshold voltages are calculated the same way as for the long channel device.

The dependence of the threshold voltages on the channel length is more complex in the Si/SiGe/Si MOSFET than in the corresponding silicon structure. The absolute value of the first threshold voltage V_{TH} decreases as indicated by eqn (12) since the bulk charge term ($q N_B^* x_{dmax}$) decreases and the hole contri-

bution [$H(\phi_{TH})$] has only a small effect on V_{TH}. This dependence is analogous to that in silicon MOSFETs. However, the second threshold voltage V_{TS} behaves differently. As indicated by eqn (14), the dependence on the channel length is given by the last term in that equation. Although, the bulk charge term ($q N_B^* x_{dmax}$) decreases as L_{eff} decreases, the hole contribution [$H(\phi_H)$] increases as L_{eff} decreases. It turns out that the second effect (hole contribution to V_{TS}) is the dominant one and the absolute value of the second threshold voltage V_{TS} increases with channel length reduction. This result is confirmed by the two-dimensional numerical simulation presented in the next section.

The above model for the threshold voltages remains valid as long as N_B^* has a positive value. For extremely short-channel devices N_B^* becomes negative which implies that the gate completely loses control over the channel. In this range of L_{eff}, the model is no longer applicable since such devices work in the punchthrough mode and the term threshold voltage becomes meaningless.

3. RESULTS AND DISCUSSION

3.1. Long-channel device

The anlaytical model presented above was first compared to results obtained by one-dimensional numerical solution of Poisson's equation using Fermi–Dirac statistics[8]. The threshold voltages V_{TH} and V_{TS} were extracted from simulation results using the same definitions as in the analytical model. An n^+ polysilicon gate is assumed in the calculations and the fixed oxide charge Q_f is neglected. Strained SiGe bandgap and permittivity data have been taken from [9] and the conduction band offset ΔE_c, between Si and SiGe, was considered negligible ($\Delta E_v = \Delta E_g$), irrespective of the Ge concentration. Due to lack of reliable experimental data, the valence band densities of states, controversial even for Si[11], were assumed identical in Si and SiGe.

The dependence of the threshold voltages V_{TH} and V_{TS} on the Germanium content x in the $Si_{1-x}Ge_x$ film is shown in Fig. 4. The agreement between the analytical model and the numerical simulations is excellent. The absolute value of the threshold voltage V_{TH} decreases with Ge content x. This is due to the linear increase of the valence band offset ΔE_v with x which makes it easier to invert the top Si/SiGe heterointerface. Increasing x yields larger ϕ_{TH} (less negative) which increases $|V_{TS}|$. For an optimum device, x must be as large as possible subject to the requirement of maintaining strain in the SiGe film.

The dependence of the threshold voltages V_{TH} and V_{TS} on the thickness of the cap layer is shown in Fig. 5. The agreement between the model and numerical simulation is again excellent. It can be observed from Fig. 5 that the thickness of the cap layer plays a crucial role in the design of the Si/SiGe/Si MOS structure. If the cap thickness is
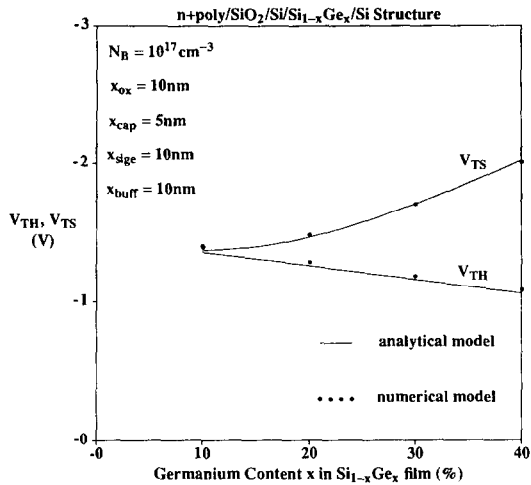
Fig. 4. Calculated dependence of the threshold voltages on the germanium content x in the $Si_{1-x}Ge_x$ film using the analytical model and one-dimensional numerical simulations.

Fig. 6. Calculated dependence of the threshold voltages on the gate oxide thickness x_{ox} using the analytical model and one-dimensional numerical simulations.

larger than 15 nm the gate voltage window $\Delta V_T = V_{TH} - V_{TS}$ becomes very small. Although the model predicts that the voltage window can be increased significantly by reducing the cap thickness below 5 nm, it must be mentioned that in a practical situation the advantage of using the SiGe structure may be lost to some degree due to the possible interaction of free carriers (holes) in the SiGe channel with the Si–SiO$_2$ interface. In addition, for very thin cap layers the quality of Si–SiO$_2$ interface may be degraded[4].

The dependence of the threshold voltages on the Ge content and the cap thickness discussed above are in accordance with earlier theoretical and experimental results[3–5] confirming the validity of the analytical model.
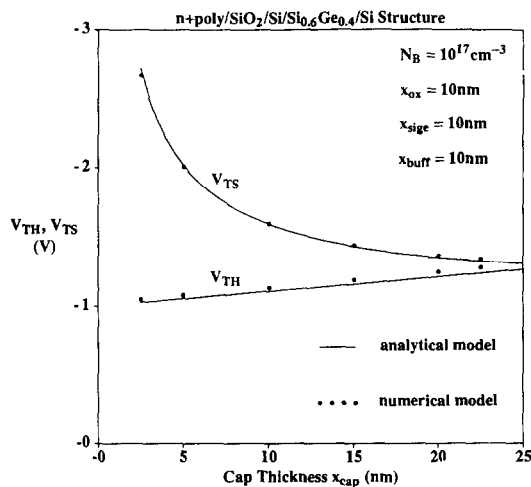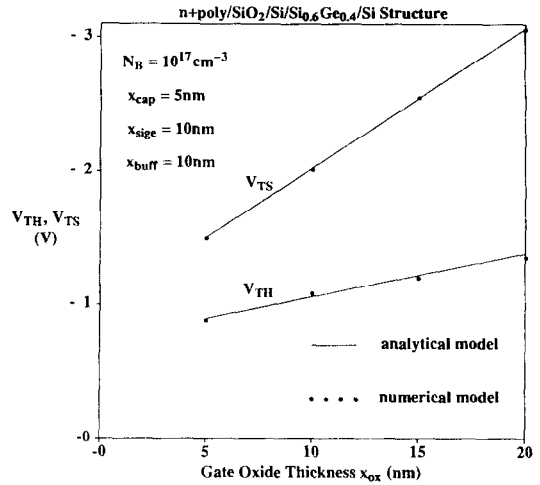
The absolute values of the threshold voltages V_{TH} and V_{TS} increase as the gate oxide thickness increases, as shown in Fig. 6. This dependence is linear as indicated by the analytical expressions (12) and (14). The change in V_{TH} and V_{TS} also increases the voltage window ΔV_T. However, this offers no real advantage since the number of carriers in the heterostructure channel remains constant for a given gate voltage as the gate oxide thickness increases. In addition, a penalty for using thicker gate oxide is the degradation of device transconductance.

The dependence of the threshold voltages V_{TH} and V_{TS} on the substrate doping concentration N_B is shown in Fig. 7. It can be observed that the absolute values of both threshold voltages increase with N_B in a similar manner. In the low doping range $(10^{16}-10^{17}$ cm$^{-3})$ the gate voltage window is nearly

Fig. 5. Calculatd dependence of the threshold voltages on the silicon cap thickness x_{cap} using the analytical model and one-dimensional numerical simulations.
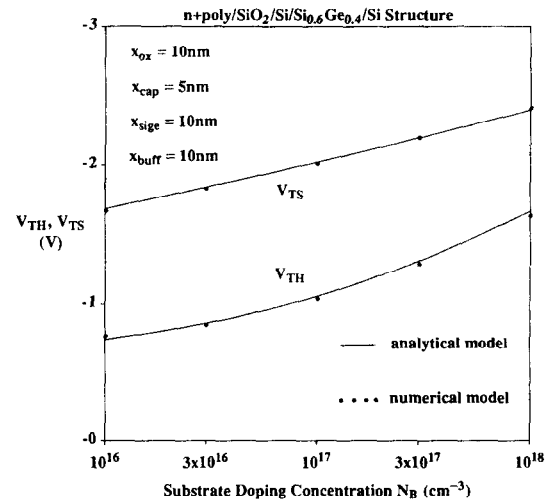

Fig. 7. Calculated dependence of the threshold voltages on the substrate doping concentration N_B using the analytical model and one-dimensional numerical simulations.

constant. However, ΔV_T starts to decrease at concentrations above 10^{17} cm^{-3}. Therefore, very high doping in the substrate should be avoided.

The dependence of the threshold voltages on the SiGe film thickness x_{sige} and the buffer thickness x_{buff} have also been studied. It has been found that these parameters have a minor influence on the threshold voltages. From a process point of view, the maximum value of the SiGe film thickness x_{sige} is limited by the requirement for maintaining strain in SiGe. In addition, the minimum value of the buffer layer x_{buff} may be limited by possible outdiffusion of impurities from the substrate during high-temperature processing.

The analytical model was derived assuming uniform Ge content in the SiGe film. However, the model remains valid even if the Ge concentration is graded, as long as the maximum concentration is at the top heterointerface, which is the most appropriate grading scheme[6,8]. In this case V_{TH} and V_{TS} can be calculated using the equations given in the previous section by assuming that the device has uniform Ge content identical to that at the top of the graded channel. The above statement was verified by numerical simulation of graded device structures. It was found that V_{TH}, within a margin error of 10–15 mV, does not depend on the grading and that V_{TS} depends very weakly on grading, changing by 100 mV from a structure with 40% uniform Ge content to one featuring 40–0% grading in the channel.

From the investigation presented above, it can be concluded that an optimum structure requires the largest possible gate voltage window. This in turn requires that the Ge concentration in the buried channel should be made as large as possible. To date the largest Ge concentration reported in a MOSFET buried channel is 40%. In this case the thickness of the SiGe film is limited to at most 10 nm in order to maintain strain. This condition can be relaxed (i.e. the SiGe thickness and/or thermal budget can be increased) by fully grading the channel from 40% (at the top) to 0% Ge (at the bottom) over a distance of 10–15 nm. For two devices with the same integrated Ge concentration, the fully graded device exhibits more efficient carrier confinement and higher transconductance then a device with uniform Ge concentration.

From the results of calculations presented above one can thus conclude that an optimum vertical structure for a p-channel Si/SiGe/Si MOSFET should be as follows:

- n-type Si substrate with a doping level in the low 10^{17} cm^{-3} range;
- undoped, 10 nm thick Si buffer;
- undoped, 10 nm thick, linearly graded (40–0% Ge) SiGe channel;
- undoped, 5 nm thick Si cap layer;
- 5–10 nm thick gate oxide.

The exact values of the gate oxide thickness depend on the oxide integrity and manufacturability. The choice of the appropriate doping level in the substrate is determined by a need to minimize short-channel effects and is discussed in more detail below.

3.2. Short-channel devices

Two-dimensional effects on the threshold voltage and the device high frequency performance were anlayzed using the commercial heterostructure device simulator PRISM[12,13]. SiGe and its material properties were introduced in the simulation by restoring to the user-defined material properties. Electric field and energy dependence of carrier mobility were not considered because PRISM does not allow such a model for user-defined material. Instead, constant hole mobilities of 414 cm^3/Vs for SiGe (40% Ge) and 150 cm^3/Vs for Si were employed. While these simplifications lead to an overestimation of the cutoff frequency, they do not affect the accuracy of the threshold voltages simulations.

The dependence of the threshold voltages on the effective channel length have been calculated for two device structures A and B having optimum vertical structure specified above. Device A has the gate oxide thickness $x_{\text{ox}} = 10$ nm, the substrate doping concentration $N_B = 10^{17}$ cm^{-13} and the source/drain junction depth $x_j = 0.15 \mu$m. Device B is a scaled version of A and has $x_{\text{ox}} = 5$ nm, $N_B = 2 \times 10^{17}$ cm^{-3} and $x_j = 0.1 \mu$m. The results of the simulations are shown in Figs 8 and 9. As can be seen, the agreement between the analytical model and two-dimensional simulation is very good.

As expected from the analytical derivation, the absolute value of the first threshold voltage V_{TH} decreases as the channel length is reduced. At the same time the absolute value of the second threshold voltage V_{TS} increases. Both predictions of the analytical model are fully supported by the results of two-dimensional simulation.

The voltage-doping transformation provides not only the means for accurate modeling the dependence of the threshold voltages on the channel length, but it also ensures the physical nature of the model. For example, the depletion layer width x_{dmax} at the strong inversion shows the correct behavior. As the channel length is reduced, the depletion layer width increases since the gate starts loosing its control over the channel and depletion layer. To illustrate this effect the depletion layer width x_{dmax} was calculated analytically using eqn (13) with the real doping concentration N_B replaced by the effective doping concentration N_B^* given by eqn (15). The analytical model is in good agreement with the results of two-dimensional simulations as shown in Fig. 10. In the numerical simulation the depletion layer width was defined in the center of the channel, in a similar manner as in the analytical model, as the distance between the substrate–buffer interface and the point
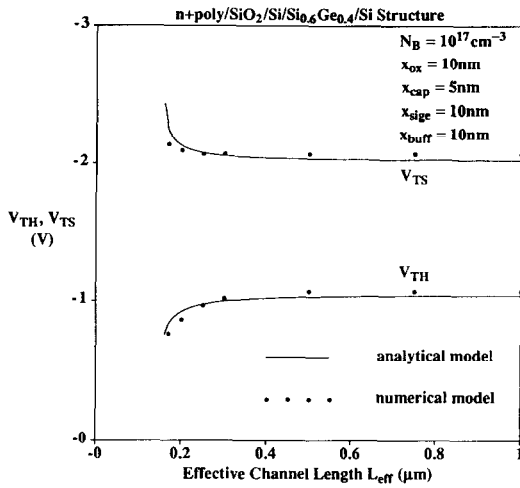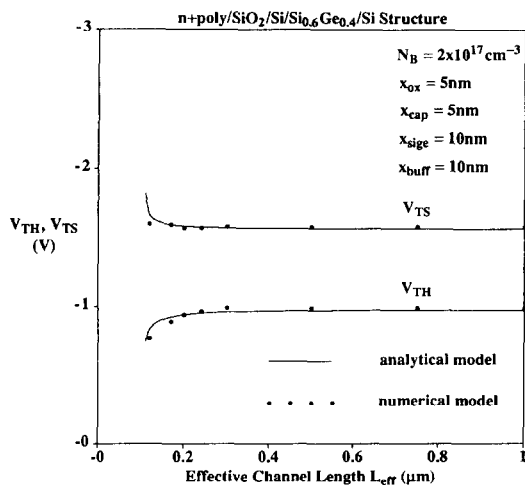
Fig. 8. Calculated dependence of the threshold voltages on the effective channel length L_{eff} for the structure A using the analytical model and two-dimensional simulations.
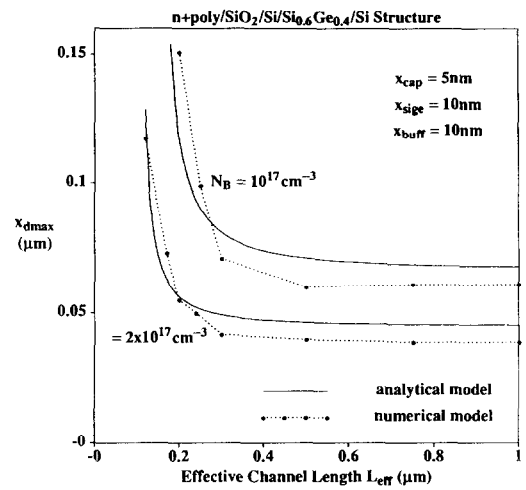

Fig. 10. Calculated dependence of the maximum depletion layer width x_{dmax} on the effective channel length L_{eff} using the analytical model and two-dimensional simulations.

in the substrate where majority carrier (electron) concentration is equal to $N_B/3$.

Based on the results shown in Figs 8 and 9 it is possible to define a critical effective channel length at which the threshold voltage V_{TH} differs by 100 mV from its corresponding long-channel value. For the device A the critical channel length is 0.22 μm and for the scaled device B it is reduced to 0.14 μm. As expected, scaling the gate oxide thickness and the substrate doping concentration helps in minimizing short-channel effects.

It can be therefore proposed that device A should be suitable for 0.5 μm and device B for 0.35 μm CMOS/BiCMOS technology. To provide exmples of the potential offered by these structures some device characteristics were simulated using PRISM for 3.3 V supply voltage applications. For the device A, 0.5 μm

gate length was selected, which resulted in 0.36 μm effective channel length due to the source/drain lateral diffusion. For the scaled device B the gate length was chosen to be 0.35 μm and the effective channel length was 0.24 μm.

As obtained from the results of two-dimensional simulations the subthreshold slope S is 98 mV/dec for device A and 95 mV/dec for device B. These values do not change as the drain-source voltage V_D is changed from -0.1 V to -3.3 V. When V_D is changed from -0.1 V to -3.3 V the threshold voltage V_{TH} changes by 97 mV for device A and 83 mV for device B. These results confirm that short-channel effects are effectively suppressed in both devices. The maximum cut-off frequency was calculated as in [8], resulting in 77 GHz for device A and 86 GHz for device B. These results suggest good device potential for high-speed applications.

4. CONCLUSIONS

Analytical expressions for the threshold voltages in a Si/SiGe/Si MOS structure were derived from Poisson's equation. The validity of the model was verified by numerical simulation.

The dependence of the threshold voltages on the device structural parameters was studied. The gate voltage window ΔV_T, defined as the difference between the V_{TH} and V_{TS} threshold voltages, was used as a performance indicator. It was shown that the voltage window increases as the germanium mole fraction increases, the cap thickness decreases and the gate oxide thickness increases. However, the increase in the Ge concentration is limited by the requirement of maintaining strain in the SiGe film. The decrease of the silicon cap thickness is limited by the interaction between the top heterointerface and the silicon surface. Finally, increasing the gate oxide thickness to expand the gate voltage window causes degradation of other device parameters.

Fig. 9. Calculated dependence of the threshold voltages on the effective channel length L_{eff} for the structure B using the analytical model and two-dimensional simulations.

The analytical model takes into account short-channel effects in Si/SiGe/Si MOSFETs. It correctly predicts the dependence of the threshold voltages on the device channel length as verified by two-dimensional numerical simulations. It was shown for the first time that short-channel effects reduce the threshold voltage at the heterointerface V_{TH} and increase the gate voltage window.

Based on this investigation an optimum vertical structure for the p-channel Si/SiGe/Si MOSFET was proposed. This structure should provide substantial improvement over conventional p-channel silicon MOSFETs for applications in submicron CMOS/BiCMOS technology.

REFERENCES

1. S. S. Iyer, G. L. Patton, J. M. C. Stork, B. S. Meyerson and D. L. Harame, *IEEE Trans. Electron. Devices* **36**, 2043 (1989).
2. D. K. Nayak, J. C. S. Woo, J. S. Park, K. L. Wang and K. P. MacWilliams, *IEEE Electron. Devices Lett.* **12**, 154 (1991).
3. P. M. Garone, V. Venkataraman and J. C. Sturm, *IEEE Electron. Devices Lett.* **12**, 230 (1991).
4. S. S. Iyer, P. M. Solomon, V. P. Kesan, A. A. Bright, T. N. Nguyen and A. C. Warren, *IEEE Electron Devices Lett.* **12**, 246 (1991).
5. S. Verdonckt-Vandebroek, E. F. Crabbe, B. S. Meyerson, D. L. Harame, P. J. Restle, J. M. C. Stork, A. C. Megdanis, C. L. Stanis, A. B. Bright, G. M. W. Kroesen and A. C. Warren, *IEEE Electron Devices Lett.* **12**, 447 (1991).
6. S. Verdonckt-Vandebroek, E. F. Crabbe, B. S. Meyerson, D. L. Harame, P. J. Restle, J. M. C. Stork, A. C. Megdanis, C. L. Stanis, A. Bright, G. M. W. Koresen and A. C. Warren, *Proc. Symp. VLSI Technology*, p. 105 (1991).
7. T. Skotnicki, G. Merckel and T. Pedron, *IEEE Electron Devices Lett.* **9**, 109 (1988).
8. S. Voinigescu and C. A. T. Salama, *Proc. 6th Canadian Semiconductor Technology Conf.*, Ottawa, p. 66, Aug. (1992). Also, *Can. J. Phys.* accepted for publication.
9. R. People, *IEEE J. Quantum Electron.* **QE-22**, 1696 (1986).
10. H. C. de Graaff and F. M. Klaassen, *Compact Transistor Modelling for Circuit Design*, Chap 6, Springer, Wien (1990).
11. M. A. Green, *J. appl. Phys.* **67**, 2944 (1990).
12. R. Vankemmel, W. Schoenmaker, R. Cartuyvels, K. Appeltans and K. De Meyer, *Solid-St. Electron.* **35**, 571 (1992).
13. PRISM, Program for Investigating Semiconductor Models, Users manual, Silvaco, Santa Clara, Calif. (1992).