Analytical Models and Algorithms for the Efficient Signal Integrity Verification of Inductance-Effect-Prominent Multicoupled VLSI Circuit Interconnects

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***Abstract*—Novel signal integrity verification models and algorithms for inductance-effect- prominent *RLC* interconnect lines are developed by using a traveling-wave-based waveform approximation (TWA) technique. The multicoupled line responses are decoupled into the eigenmodes of the system in order to exploit the TWA technique. Then, the response signals are mathematically represented by the linear combination of each eigenmode response based on TWA, followed by reporting the signal integrity models and algorithms for the multicoupled lines. The signal integrity of VLSI circuit interconnects is complicatedly correlated with input signal switching-patterns, layout geometry, and termination conditions. It is shown that the technique can be efficiently employed for complicated multicoupled interconnect lines with various termination conditions and the signal transients based on the technique have excellent agreement with SPICE simulations. Thus, with the proposed technique, the switching-dependent signal delay, crosstalk, ringing, and glitches of the inductance-effect-prominent *RLC* interconnect lines can be accurately as well as efficiently determined.**

***Index Terms*—Crosstalk, delay, glitch, ringing, signal integrity, transmission line, traveling-wave, traveling-wave-based waveform approximation (TWA), very large scale integration (VLSI) interconnects.**

I. Introduction

TOMORROW'S high-performance VLSI circuits may require a clock signal with several 10's picosecond edge rate and integrate more than a billion transistors in a single silicon die [1]–[3]. In such high-frequency-operating gigantic chips, the electrical lengths of interconnect lines become a significant fraction of the transient signal's fundamental and harmonic frequency wavelength [4]–[6]. Thus, neither simple capacitive loads nor lumped *RC* lines show the behavior of future VLSI circuit interconnects. In reality, even in today's integrated circuits, the signal integrity degradation due to interconnect lines is one of the crucial performance limitation factors [2]–[4], [7]–[9]. The signal integrity impairment of the future integrated circuits (less than 0.1-μm gatelength) owing to the signal loss, timing uncertainty, spurious glitches, and crosstalk noises is expected to be much more significant than today's integrated circuits [1]–[4], [6], [10], [11]. In the near future, copper interconnect metal as well as low intermetal dielectric material will be ubiquitously used in ultradeep submicron IC process in order to reduce the line resistances and capacitances [1], [4], [12]–[15]. Note, however, these process improvement efforts will negligibly reduce the inductances of the interconnect lines which are strongly correlated with current paths, i.e., layout geometry. Moreover, high-speed switching operation makes the interconnect lines more inductance-effect-prominent rather than capacitance-effect-prominent [6], [9], which means the underdamped circuit response of a series *RLC* circuit. In the lumped series *RLC* circuit, whether the circuit response is under-damped or not, can be very simply determined by the damping factor ($\xi \equiv R/2\sqrt{C/L}$) or quality factor ($Q \equiv 1/R\sqrt{L/C}$). In general, if ξ is less than one (or if Q is greater than 0.5), the circuit response is under-damped. The more stringent conditions may be determined with transmission line parameters, driver resistance, load capacitances, and input slew rate [16].

Unfortunately, the signal integrity verification problems are much more complicated in the inductance-effect-prominent *RLC* lines than in capacitance-effect-prominent *RLC* lines since the system response may be a nonmonotonic oscillating-wave shape contaminated with spurious noise spikes [13]. That is, unlike capacitance-effect-prominent lines (i.e., over-damped cases), not only can the response signals of the inductance-effect-prominent lines oscillate until they settle down to a final value but they may also contain many spurious glitches. In addition, unlike capacitive coupling, inductive coupling may have a substantial effect over a larger physical area of the system [6]. Consequently, future VLSI system designers may be victims of inexorably complicated signal integrity problems due to the inductance-effect-prominent interconnect lines. Thus, the electrical characteristics of these interconnect lines need to be carefully examined by treating them as *RLC*-transmission lines [4], [5]. Efficient as well as accurate signal integrity verification methodologies and simple computer-aided design (CAD) models for such inductance-effect-prominent *RLC* lines are essential for future intricate VLSI circuit designs.

Previously, fast-simulation techniques and closed form models for the signal integrity verification of *RC*-dominant

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integrated circuit interconnect networks have been reported [11], [17]–[22]. The techniques are considered to be very powerful for the lines that the inductance effects are negligibly small. However, since they do not take the inductance effects into account, the models will be used at great risk in future high-performance VLSI circuit designs. Recently, many interconnect line models have been developed incorporating inductive effects. A large collection of model order reduction techniques based on methods of moment matching is proposed in the literature [23]–[31]. However, if the lines are inductance-effect-prominent, these techniques may be limited by, i.e., inaccuracies, nonconvergence, or heavy computation time [13]. Further, these model order reduction techniques do not provide closed form expressions for signal integrity verification. Closed form solutions are highly desirable for the efficient layout verification of the extremely complicated future VLSI circuits.

In practice, inductance-effect-prominent lines cannot be simply modeled with dominant poles as is done for capacitance-effect-prominent lines since the high-frequency effects have to be taken into account [9], [13]. To date, there have been many modeling techniques that employ simplified expressions to represent *RLC* transmission line behavior. These techniques are very useful for the fast signal integrity verifications required in large interconnect systems [12], [32]–[38]. Kahng *et al.* proposed an approximate signal delay model of a single *RLC* line based on the two-dominant poles of the interconnect line [35]. Since the model requires several statistical fitting parameters, it may not be practical. Ismail *et al.* developed a very good timing model of *RLC* tree structure networks, assuming there were no coupling effects between the lines [12]. Thus, the model cannot be employed for the coupled *RLC*-line system which is very common in ICs. Cao *et al.* derived an analytical timing model by mathematically collapsing two-coupled *RLC* lines into an effective isolated line [34]. However, this technique cannot be suitably applied for multicoupled lines including more than two lines. Further, since the aforementioned techniques are focused only on the signal delay of the *RLC* interconnect lines, the other important signal variation characteristics such as switching-dependency of the signal delay, crosstalk, glitches, and ringing (overshoot/undershoot) are not examined. Unlike the other delay models, Davis and Meindl derived the time-domain responses in analytical manner for the limited cases of two- and triple-coupled lines based on the modified Bessel function, thereby providing closed form signal integrity models [37], [38]. Although the models are accurate for the intended applications, they are too complicated to be extended to general multicoupled lines with more than three-coupled lines. Note, unlike interline capacitive coupling, the inductive coupling may have a substantial effect on physically distant lines within the system. The authors find that the signal integrity of the high-speed/high-density VLSI circuits should be examined and verified in more than just adjacent lines for inductive coupling. Thus, the models need to be extended into a general n-coupled transmission line system.

Assuming a quasi-TEM mode, multicoupled transmission lines have been mathematically modeled as a matrix form of the Telegrapher Equation [6], [39]–[47]. Then a modal decoupling technique which represents the signal variations with the characteristic eigenmodes of the system has been widely used for modeling transmission line for the last several decades [6], [36], [39]–[41], [48]–[50]. However, these generic modal analysis techniques require computationally inefficient numerical integration for determining the time-domain responses and may not be suitable for the computationally fast signal integrity verification of intricate integrated circuits. Many model order reduction techniques such as AWE or related rational-function-based model order reduction techniques were developed by assuming linear device models and frequency-independent transmission line parameters [23]–[31], [36] in order to avoid the computationally inefficient numerical integration. However, these techniques may not be efficiently used for inductance-effect-prominent lines due to several limitations: heavy computation time, nonconvergence problems, or solution inaccuracies [13]. Recently, Eo *et al.* developed a novel signal transient characterization technique which was named the Traveling-wave-based Waveform Approximation (TWA) technique [6], [9]. The TWA-technique characterizes the physical phenomena of the transient signal of a transmission line by utilizing a frequency-domain-based approximation for slow-transient characteristics and time-domain approximation for fast-transient characteristics of the system response. Since the TWA-technique does not require any numerical integration, it is computationally very efficient. The TWA-technique focuses on a fast and efficient wave-shape modeling within a tolerable accuracy under the assumption that loads and sources are linear and transmission line parameters are frequency-independent. Thereby, the computation time for signal integrity simulations can be considerably reduced. Note, the constant transmission line approach that is assumed in the TWA-technique and almost all of the fast simulation algorithms can be considered to be conservative assumptions for signal integrity verification [6].

In this work, novel closed form models and efficient computation algorithms for the signal integrity parameter verification of the inductance-effect-prominent multicoupled *RLC* lines based on the TWA-technique are developed. Thereby, key signal integrity parameters of an arbitrary number of inductance-effect-prominent multicoupled interconnect lines can be determined several thousand times faster than slower methodologies. With these simple models and algorithms, it is shown that the switching-dependent signal delay, crosstalk, ringing, and glitches for inductance-effect-prominent multicoupled *RLC* lines can be accurately as well as efficiently determined.

II. Theoretical Background for TWA Technique

The physical description of the transient signal of a transmission line can be efficiently characterized by using a traveling-wave-based waveform approximation technique which combines a frequency-domain-based approximation for low-frequency characteristics with a time-domain-based approximation for high-frequency characteristics of the system response [6], [9], [51]. In the TWA-technique, assuming a step input, the low-frequency transient signal is represented

with only three-dominant poles. The three-pole-based frequency-domain response function can be transformed back into the time-domain without any numerical integration. Then, the high-frequency characteristics of the transient signal are incorporated into an approximation function by exploiting the traveling wave characteristics and a modified-*RC*-response approximation in the time domain.

When the load is open circuit, the resultant wave shape becomes at double the incident wave. However, a pulsed signal includes many frequency components from dc to very high frequency. Further, since the capacitive reactance of the load is frequency-dependent, the reflection coefficient is inherently frequency-dependent. That is, with the capacitive load, the reflection coefficient is in the range of 1 (for dc) to -1 (for very high-frequency components). This can be represented by combining a linear ramp shape (lower part) with a *RC*-response-like wave-shape (upper part) since the sharp edge part (i.e., the part that is concerned with the high-frequency components) of the time domain voltage response which is the summation of the incident and reflected waves is blunt a bit. Consequently, the upper part of the resultant response wave-shape is similar to the *RC*-response-like one, while the lower part of the resultant response wave-shape is similar to a ramp function. In order to separately model the linear ramp shape and *RC*-response-like shape of the resultant response signal, the boundary point has to be introduced. In practice, the exact boundary point between the linear part and the blunted part may not be accurately determined. Nonetheless, since the blunt amount of the wave-shape is strongly correlated with the magnitude of the load capacitance, the effect is modeled in terms of the load capacitance. That is, the smaller the load capacitance, the smaller the load capacitance effect. Thus, in this work, the capacitive loading effect is modeled as follows. The first incident wave arrives at the load with the time of the flight of a wave that is given by $t_f^- \approx \sqrt{L_{\text{line}} C_{\text{line}}}$. Including the load capacitance C_L, an effective time of flight (t_{f0}) is approximately $t_{f0} \approx \sqrt{L_{\text{line}} (C_{\text{line}} + C_L)}$. Defining the quantity δ which denotes the time difference between the flight time of the pure (unloaded) line and that of the line including loading effects as

$$\delta \equiv \sqrt{L_{\text{line}} (C_{\text{line}} + C_L)} - \sqrt{L_{\text{line}} C_{\text{line}}}. \tag{1}$$

the instant right before an incident wave is reflected can be represented by $t_f^- = t_{fo} - \delta$. Note that δ is considered to be an effective response time delay of the incident wave due to the capacitive load. Since the blunt effect of the pulsed signal happens at the upper part of the pulse, it may be assumed that the blunt effect approximately occurs after $t_f^+ = t_{fo} + \eta\delta$, where η is a constant factor which has approximately the value of one. In fact, since the *RC*-like response is approximately linear function until the 63% of the final value, η is not a critical factor to determine the wave-shape. Thus, in this work, it is conveniently selected as $\eta \approx 1$.

Thus, in the time interval between $(2n-1)\,t_{f0} - \delta$ and $(2n-1)\,t_{f0} + \delta$, where $n = 1, 2, 3, \ldots$(note, n is the reflection count), the waveform can be approximated with a linear function. In contrast, in the time interval between $(2n-1)\,t_{f0} + \delta$ and $(2n+1)\,t_{f0} - \delta$, the waveform can be modeled with an *RC*-response-like function. The time constant for this "fictitious" charging or discharging can be estimated by using an effective *RC* time constant (including C_L) of the system. The fictitious charging or discharging time constant τ can be reasonably modeled as $\tau \approx R_{\text{line}} (C_{\text{line}} + C_L)$ [9]. TWA-based resultant waveform is given by [9]. For $(2n-1)\,t_{f0} - \delta \le t \le (2n-1)\,t_{f0} + \delta$, the response can be modeled as linear ramp shape, as show in (2) at the bottom of the page, while for $(2n-1)\,t_{f0} + \delta \le t \le (2n+1)\,t_{f0} - \delta$, the response can be modeled as *RC*-response-like shape

$$\begin{aligned} v_0(t) \approx \sum_{n=1}^{\infty} \Bigg[& 2v_{03}((2n-1)\,t_{f0}) - v_{03}\left(2(n-1)\,t_{f0} + t_f^-\right) \\ & + w_n \left(1 - \exp\frac{2nt_{f0} - t_f^- - t}{\tau}\right)\Bigg] \\ & \cdot \left\{u\left(t - 2nt_{f0} + t_f^-\right) - u\left(t - 2nt_{f0} - t_f^-\right)\right\} \end{aligned} \tag{3}$$

where

$$\begin{aligned} w_n = & \frac{v_{03}\left(2nt_{f0} + t_f^-\right) - 2v_{03}((2n-1)\,t_{f0})}{1 - \exp\left(-\frac{2t_f^-}{\tau}\right)} \\ & + \frac{v_{03}\left(2(n-1)\,t_{f0} + t_f^-\right)}{1 - \exp\left(-\frac{2t_f^-}{\tau}\right)}. \end{aligned} \tag{4}$$

In the expressions, v_{03} is the three-pole-based time-domain response function and n indicates nth reflection. Thereby, an accurate time domain response signal can be calculated. Note, the magnitude of the overshoot/undershoot can be readily determined by using (3) since the overshoot and undershoot alternately occur in the time interval of $(2n-1)\,t_{f0} + \delta \le t \le (2n+1)\,t_{f0} - \delta$. The TWA technique is summarized in Fig. 1. This technique can provide the analytical signal integrity parameters of the *RLC* interconnect lines, i.e., signal delay, crosstalk, ringing, and glitches. These transmission parameters can have strong correlation with input signal switching-patterns in multiple lines.

$$\begin{aligned} v_0(t) \approx \sum_{n=1}^{\infty} & \left[\frac{v_{03}((2n-1)\,t_{f0}) - v_{03}\left(2(n-1)\,t_{f0} + t_f^-\right)}{t_{f0} - t_f^-}\,(t - (2n-1)\,t_{f0}) + v_{03}((2n-1)\,t_{fo})\right] \\ & \cdot \left[u\left(t - 2(n-1)\,t_{f0} - t_f^-\right) - u\left(t - 2nt_{f0} + t_f^-\right)\right] \end{aligned} \tag{2}$$

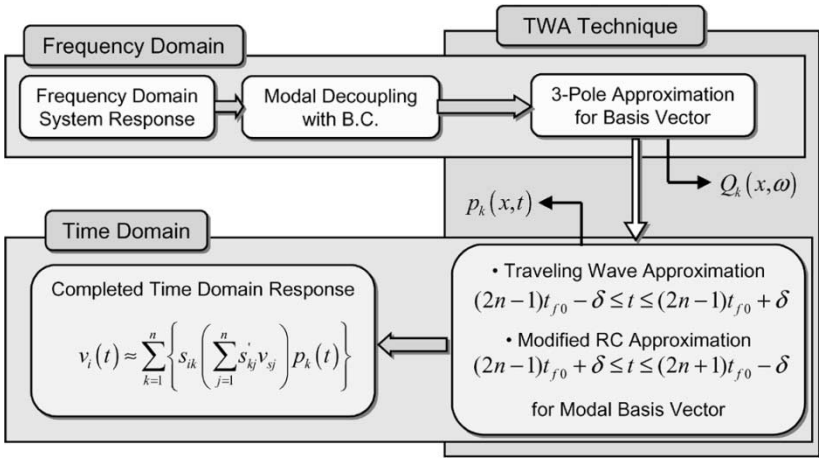


Fig. 1. Transient signal characterization based on TWA.

III. TWA-Based Signal Transient Formulation of Multicoupled Transmission Lines

Multicoupled (n-coupled) lines are modeled with a matrix form of the differential equation (Telegrapher equation). In the lossless system, the system matrix is composed of $n \times n$ inductance matrix and capacitance matrix. Thus, the equation can be solved by the eigenvalue problem corresponding to the system matrix which is [L][C]. Since the system matrix is $n \times n$ matrix, it has n eigenvalues. The solution vectors corresponding to each eigenvalue is called eigenvectors. The matrix composed of these n column vectors is called the eigenmatrix. The propagation resulting from one of these eigenvalues and eigenvectors is referred to as an eigenmode. Then finally, given boundary conditions, the signal responses of n-coupled lines can be represented with the linear combination of the eigenmodes.

The traveling waves of n-coupled lines (i.e., a transmission line system including n-signal lines) can be decoupled into the linear combination of the n-eigenmodes by using a modal analysis technique in the frequency-domain if the lines are identical or lossless (although nonidentical) [48]–[50]. Then, the incident waves in each line can be determined as

$$[W(x,\omega)] = [S][E][B], \tag{5}$$

where $[S]$ is the normalized $n \times n$ voltage eigenmatrix of the system and $[B]$ is a column vector describing the boundary conditions. The $[E]$ matrix is a diagonal matrix correlated with the propagation mode (i.e., eigenmodes) of the waves

$$[E] = \begin{bmatrix} e^{-\gamma_1 x} & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & e^{-\gamma_n x} \end{bmatrix}, \tag{6}$$

where the subscript n indicates the number of the lines. Note, $\gamma_i(\omega)$ is a function of ω. At $x = 0$, the incident wave vector is $[W(x=0,\omega)] = [v_{s1} \cdots v_{sn}]^T$, where v_{si} is the input voltage at the ith input port. Thus, the boundary condition vector is given by

$$[B] = [S]^{-1}[W(x=0,\omega)]. \tag{7}$$

Now, representing the inverse matrix of $[S]$ as follows

$$[S]^{-1} \triangleq \begin{bmatrix} s'_{11} & s'_{12} & \cdots & s'_{1n} \\ s'_{21} & s'_{22} & \cdots & s'_{2n} \\ \vdots & \vdots & & \vdots \\ s'_{n1} & s'_{n2} & \cdots & s'_{nn} \end{bmatrix}, \tag{8}$$

the kth element of $[B]$ vector can be represented by

$$b_k = \sum_{j=1}^{n} s'_{kj} v_{sj}. \tag{9}$$

Therefore, the ith incident wave can be represented by

$$W_i(x,\omega) = \sum_{k=1}^{n} \left(\frac{Z_{0k}}{R_{Si} + Z_{0k}}\right) s_{ik} e^{-\gamma_k x} b_k, \tag{10}$$

where Z_{0k} is the characteristic impedance of the kth mode and R_{Si} is the driver resistance of the ith line. In addition, $s_{ik}b_k$ is the magnitude corresponding to the kth mode. The $e^{-\gamma_k x}$ is the kth modal incident wave. Therefore, assuming the line length is "ℓ", the voltage signal of the ith line can be derived as follows,

$$V_i(x,\omega) = \sum_{k=1}^{n} \left(\frac{Z_{0k}}{R_{Si} + Z_{0k}}\right) s_{ik} b_k \left(e^{-\gamma_k x} + \Gamma_k e^{\gamma_k (x-2\ell)}\right), \tag{11}$$

where Γ_k is the reflection coefficient of the kth mode at the load. The frequency domain waveform of the kth modal wave, "$Z_{0k}/(R_{Si} + Z_{0k})\left(e^{-\gamma_k x} + \Gamma_k e^{\gamma_k (x-2\ell)}\right)$", can be approximated by using a three-pole approximation function, $Q_k(x,\omega)$. Thus, the ith line wave can be approximately modeled as

$$V_i(x,\omega) \approx \sum_{k=1}^{n} s_{ik} b_k Q_k(x,\omega). \tag{12}$$

Since $Q_k(x,\omega)$ is determined with three-dominant poles, it can be represented with partial-fractional forms. Thus, the $Q_k(x,\omega)$'s time domain counter part, $q_k(x,t)$, can be readily determined without any integral calculation. However, since the high-frequency effects are not considered in $Q_k(x,\omega)$, its time domain counter part, $q_k(x,t)$, does not model the

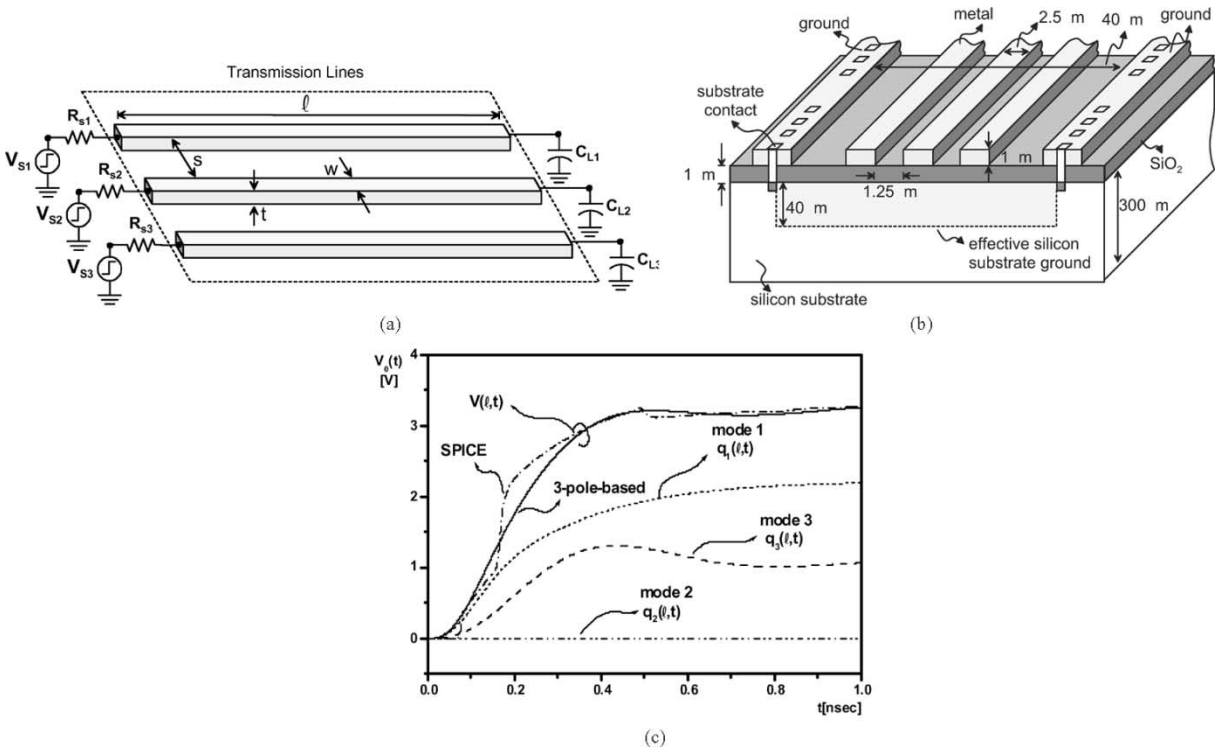


Fig. 2. The three-pole-based response signal and eigenmodes of the three-coupled line system. The response signal is investigated in the center line. The line lengths are 10 mm and the input switching pattern for respective lines is assumed as "0 ↑ 0" with a step input in the center line. (a) Test circuit configuration. (b) Cross-section. (c) Low-frequency waveforms at distance.

high-frequency effects. As an example, the three-pole-based response signal and eigenmodes for three-coupled lines are illustrated in Fig. 2. The three-pole-based response signal is not accurate enough to be useful for the timing verification. Thus, high-frequency effects have to be incorporated into the $q_k(x,t)$. This is done by exploiting the traveling-wave characteristics and the modified *RC*-approximation technique [9]. Now, denoting the TWA-based kth eigenmode function as $p_k(x,t)$ that incorporates the high-frequency characteristics into $q_k(x,t)$, the time-domain response of the ith line response $v_i(x,t)$ can be determined. That is, in the time interval between $(2n-1)t_{f0(k)} - \delta_{(k)}$ and $(2n-1)t_{f0(k)} + \delta_{(k)}$, $p_k(x,t)$ is modeled with a linear function by using $q_k(x,t)$. In contrast, in the time interval between $(2n-1)t_{f0(k)} + \delta_{(k)}$ and $(2n+1)t_{f0(k)} - \delta_{(k)}$, $p_k(x,t)$ is modeled with *RC*-response-like waveform by using $q_k(x,t)$. Then, at the load (i.e., at $x = \ell$), the time domain response $v_i(\ell,t)$ becomes

$$v_i(\ell,t) \approx \sum_{k=1}^{n} s_{ik} b_k p_k(\ell,t). \tag{13}$$

The TWA-based response signal and $p_k(x,t)$ for the same test circuit as in Fig. 2(a) are illustrated in Fig. 3. Unlike the previous three-pole-based response, TWA-based $v_i(\ell,t)$ can be accurately represented by the time-domain system response. Note, since ℓ is a constant, (13) is only a function of time. Thus, ℓ can be omitted in the expression. Then, plugging (9) into (13), at the load, the voltage signal of the ith line becomes

$$v_i(t) \approx \sum_{k=1}^{n} \left\{ s_{ik} \left(\sum_{j=1}^{n} s'_{kj} v_{sj} \right) p_k(t) \right\}. \tag{14}$$

Equation (14) is a fundamental expression for analytic signal integrity modeling of multicoupled *RLC* transmission lines.

IV. Signal Integrity Modeling and Algorithms

The 50% delay of the ith line can be determined by letting the response signal be $0.5v_{si}$ in (14). That is

$$v_i(t) = \sum_{k=1}^{n} \left\{ s_{ik} \left(\sum_{j=1}^{n} s'_{kj} v_{sj} \right) p_k(t) \right\} = 0.5 v_{si}. \tag{15}$$

Note, the signal voltage is composed of a linear combination of n eigenmodes of the system and each eigenmode has its own time of flight, $t_{f(k)}$, where the subscript k indicates the kth mode. For our convenience, assuming the modes are arranged in an ascending order based on the magnitude of the time of flight, $t_{f(k)}$, nth mode is the slowest (the largest time of flight) mode. In many practical cases, the 50% delay occurs after the slowest mode. However, since the 50% delay may occur before the slowest mode, whether the signal voltage value at the time of flight of the slowest mode exceeds the 50% value or not has to be tested. If the transmission value does not exceed the 50% value, the 50% value can be determined with the slowest mode. Otherwise, a similar test has to be done with the next slowest mode until the transmission value at the time of flight does not exceed the 50% value. Once the correct incremental mode is found, the 50% delay can be readily determined. Assuming 50% signal delay occurs after the time of flight $t_{f(n)}$ of the nth mode and the end point of the linear approximation interval is greater than the 50% of the final value, the 50% delay of the signal can

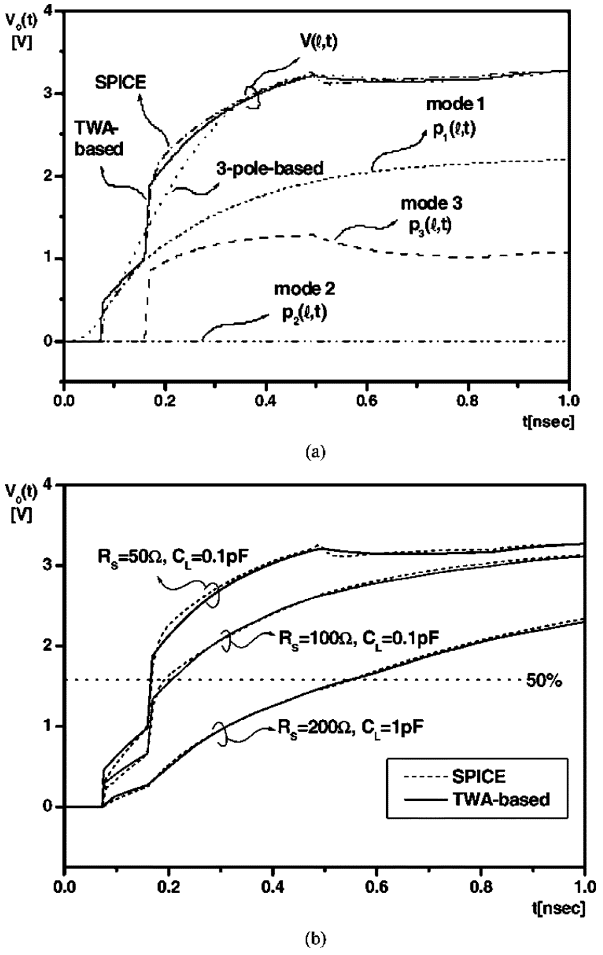


Fig. 3. TWA-based time domain response signal for the three-coupled lines. The test circuit is the same as in Fig. 2(a). (a) Stair-case response and eigenmodes. (b) Response signals dependent on the driver size and load capacitance. A circuit response with large driver and large load capacitance has an *RC*-response-like smoother waveform.

be estimated under a linear approximation. A linear approximation can be readily performed since the two key points, i.e., the starting point of the linear approximation interval of the n th mode, $\alpha\left(t^{-}_{f(n)},\, v_i\left(t^{-}_{f(n)}\right)\right)$ and the end point of the linear approximation interval of the nth mode, $\beta\left(t_{f0(n)}+\delta_{(n)},\ v_i\left(t_{f0(n)}+\delta_{(n)}\right)\right)$ of the approximation function are known values. Thus, the expression for the ith line signal delay can be represented as

$$v_i(t) \approx \frac{v_i\left(t_{f0(n)}+\delta_{(n)}\right)-v_i\left(t^{-}_{f(n)}\right)}{2\delta_{(n)}}\left(t-t^{-}_{f(n)}\right)+v_i\left(t^{-}_{f(n)}\right). \tag{16}$$

Therefore, the 50% delay time of the ith line can be approximated by

$$t_{50\%\text{delay}} = \frac{2\delta_{(n)}}{v_i\left(t_{f0(n)}+\delta_{(n)}\right)-v_i\left(t^{-}_{f(n)}\right)} \cdot\left(0.5v_{si}-v_i\left(t^{-}_{f(n)}\right)\right)+t^{-}_{f(n)}. \tag{17}$$

However, since the signal transients are strongly dependent on driver size and load capacitance, the response waveforms may not be a staircase as shown in Fig. 3(b). In this case, the β may be less than the 50% of the final value. Thus, if the β is less than the 50% of the final value, the delay expression has to be modified to be able to include an *RC*-response-like smoother waveform. The modified delay waveforms can be determined by linear approximation up to a time, t_{test}. The t_{test} is the 50% value which is determined by the linear approximation of the *RC*-like response region [52]. Note, it is guaranteed that the transmitted value of *RC*-like response at t_{test} is always greater than the 50% of the final value since the *RC*-like response function is a convex curve. Thus, the modified delay expression can be derived as

$$t'_{50\%\text{delay}} = \frac{t_{\text{test}}-\left(t_{f0(n)}+\delta_{(n)}\right)}{v_{\text{test}}-v_i\left(t_{f0(n)}+\delta_{(n)}\right)} \cdot\left(0.5v_{si}-v_i\left(t_{f0(n)}+\delta_{(n)}\right)\right)+\left(t_{f0(n)}+\delta_{(n)}\right), \tag{18}$$

where

$$t_{\text{test}} = \frac{2t^{-}_{f(n)}}{v_i\left(3t_{f0(n)}-\delta_{(n)}\right)-v_i\left(t_{f0(n)}+\delta_{(n)}\right)} \cdot\left(0.5v_{si}-v_i\left(t_{f0(n)}+\delta_{(n)}\right)\right)+\left(t_{f0(n)}+\delta_{(n)}\right) \tag{19}$$

$$v_{\text{test}} = v_i\left(t_{\text{test}}\right). \tag{20}$$

The graphical interpretation and algorithms for the 50% signal delay determination are described in Fig. 4. The 50% signal delay for various line lengths and input switching patterns of Fig. 2(a) circuits are investigated by using (17) and (18). The transmission line parameters are determined by using a commercial field solver. The parameters are as follows

$$[L] = \begin{bmatrix} 7.15 & 4.94 & 3.84 \\ 4.94 & 7.01 & 4.94 \\ 3.84 & 4.94 & 7.15 \end{bmatrix}\left[\frac{\text{nH}}{\text{cm}}\right]$$

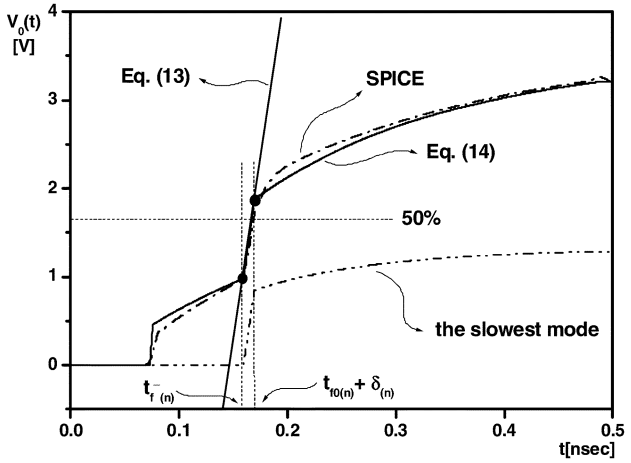
$$[C] = \begin{bmatrix} 2.22 & -0.52 & -0.04 \\ -0.52 & 2.42 & -0.52 \\ -0.04 & -0.52 & 2.22 \end{bmatrix}\left[\frac{\text{pF}}{\text{cm}}\right]$$

$$[R] = \text{diag}\,[68.97]\left[\frac{\Omega}{\text{cm}}\right].$$

As summarized in Tables I–III, the signal delays have excellent agreement with SPICE simulation with approximately 5% error. Further, the *RLC* line may oscillate due to impedance mismatches between the line characteristic impedance and load impedance. Since the peak overshoot occurs at the right before the second reflection of the incident wave at the load[1], the peak voltage can be readily determined with the following expression

$$v_{i-\text{peak}} = \text{MAX}\left(v_{si}, \sum_{k=1}^{n}\left\{s_{ik}\left(\sum_{j=1}^{n} s'_{kj}v_{sj}\right)p_k\left(3t_{f0(n)}\right)\right\}\right). \tag{21}$$

[1]The reflection due to the impedance mismatching causes the overshoot and undershoot alternatively at the load. The first overshoot (undershoot) is the largest one since the waveform is a kind of damped oscillation waveform. That is, the peak overshoot occurs right before the second reflection. Similarly, the peak undershoot occurs right before the third reflection.



(a)

```
Algorithm : DELAY( )
    input1 : objective line number
    input2 : total line number
    delay : 50% delay for the input1 line

PROCEDURE DELAY(input1, input2, delay)
  begin
    include "MODAL_PARAMETERS"
      t2= max. effective time of flight of all modes + delta;
      t1= max. time of flight of all modes;
    PROCEDURE TOTALVOLTAGE(input1, input2, t2, vi)
      v2= vi;
    PROCEDURE TOTALVOLTAGE(input1, input2, t1, vi)
      v1= vi;
      delay= 2 * delta / (v-v1) * (0.5*vs(input1) - v1) + t1;
  end_begin

PROCEDURE TOTALVOLTAGE (input1, input2, time, sum)
  begin
    while (i≤ input2)
      PROCEDURE TWA(input1, i, time, out) // a single-line-based TWA//
        sum=sum + out;
    end_while
  end_begin
```

(b)

```
Algorithm : RC_DELAY( )
    input1 : objective line number
    input2 : total line number
    delay : 50% delay for the input1 line

PROCEDURE RC_DELAY(input1, input2, delay)
  begin
    include "MODAL_PARAMETERS"
      t2= 3*max. effective time of flight of all modes - delta;
      t1= max. time of flight of all modes + delta;
    PROCEDURE TOTALVOLTAGE(input1, input2, t2, vi)
      v2= vi;
    PROCEDURE TOTALVOLTAGE(input1, input2, t1, vi)
      v1= vi;
      ttest= first false_ position point;
    PROCEDURE TOTALVOLTAGE(input1, input2, ttest, vi)
      vtest= vi;
      delay= (ttest – t1) / (vtest – vi) * 0.5 * vs(input1) – v1) + t1;
  end_begin
```

(c)

```
Algorithm : TOTALVOLTAGE( )
    input1 : objective line number
    input2 : total line number
    time : objective time
    sum : summation voltage of all modes

PROCEDURE TOTALVOLTAGE (input1, input2, time, sum)
  begin
    while (i≤ input2)
      PROCEDURE TWA(input1, i, time, out) // a single-line-based TWA//
        sum=sum + out;
    end_while
  end_begin
```

(d)

Fig. 4. Graphical description and algorithms for the 50% signal delay determination. The 50% signal delay is determined by using the slowest eigenmode and (14). The linear region of (14) is modeled with (16). (a) Graphical description. (b) Algorithm for the 50% delay determination in the linear region. (c) Algorithm for the 50% delay determination in the *RC*-like response region. (d) The algorithm of procedure "TOTALVOLTAGE."

TABLE I
LINE-LENGTH-DEPENDENT SIGNAL TRANSIENT CHARACTERISTICS. THE TEST CIRCUIT CONFIGURATION IS THE SAME AS IN FIG. 2 (A). THE INPUT SWITCHING PATTERN IS ASSUMED AS "0 ↑ 0"

Line Length	Active Line Delay [psec]		Active Line Overshoot [V]		Quiet Line Crosstalk [V]	
	SPICE	TWA	SPICE	TWA	SPICE	TWA
1mm	19.2	17.4	3.5913	3.3854	0.5807	0.6821
2mm	35.5	33.7	3.5868	3.4848	0.5762	0.6592
5mm	85.2	83.6	3.4601	3.4139	0.53	0.5652
10mm	168.8	166.8	3.2548	3.2060	0.5192	0.4446

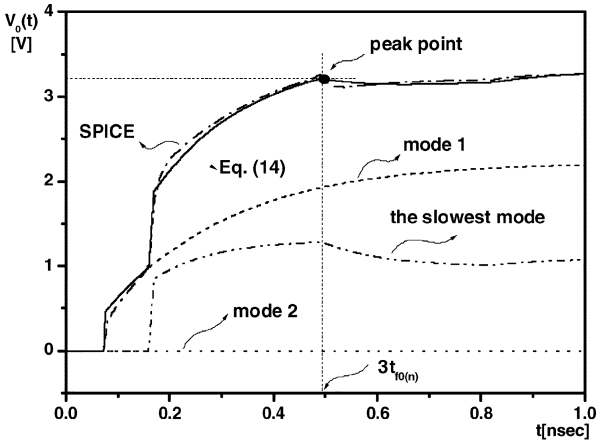
TABLE II
SWITCHING-PATTERN-DEPENDENT SIGNAL TRANSIENT CHARACTERISTICS. THE TEST CIRCUIT CONFIGURATION IS THE SAME AS IN FIG. 2(A)

Switching Patterns	Center Line Delay [psec]		Center Line Overshoot [V]		Quiet Line Crosstalk [V]	
	SPICE	TWA	SPICE	TWA	SPICE	TWA
0 ↑ 0	168.8	166.8	3.2548	3.2082	0.5192	0.4446
↑ ↑ ↑	167.6	165.7	4.0301	3.9860	—	—
↑ 0 ↑	—	—	—	—	1.0153	1.0275

The graphical interpretation and algorithm for peak overshoot determination are described in Fig. 5. The peak overshoots of the signals for three-coupled lines of Fig. 2(a) are investigated by varying the line length. As summarized in Tables I and II,

TABLE III
DRIVER-SIZE- AND LOAD-DEPENDENT SIGNAL DELAY CHARACTERISTICS

Items (driver/load)	SPICE [psec]	TWA-based [psec]	Error[%]
(50Ω / 0.1pF)	168.8	166.8	1.2
(100Ω / 0.1pF)	203.2	219.5	8
(200Ω / 1pF)	582.2	589.3	1.2



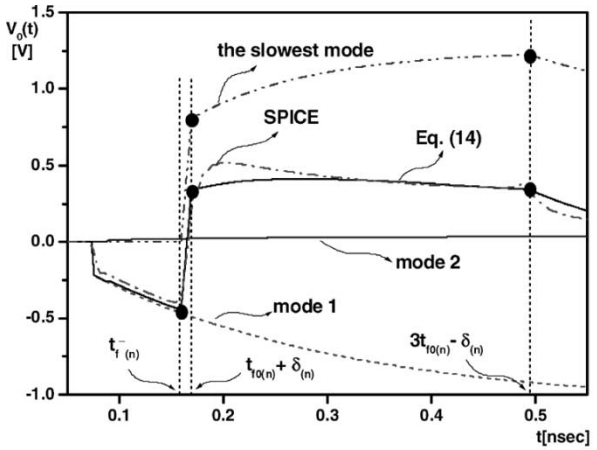
(a)

```
Algorithm : OVERSHOOT( )
      input1 : objective line number
      input2 : total line number
      overshoot : overshoot peak vlotage

PROCEDURE OVERSHOOT(input1, input2, overshoot)
   begin
      include "MODAL_PARAMETERS"
         t1= 3*max. effective time of flight of all modes;
      PROCEDURE TOTALVOLTAGE(input1, input2, t1, vi)
         overshoot= vi;
   end_begin
```

(b)

Fig. 5. Graphical description and algorithm for the peak overshoot voltage determination. The peak overshoot voltage is determined by using the slowest eigenmode and (14). (a) Graphical description. (b) Algorithm for the overshoot determination.



(a)

```
Algorithm : CROSSTALK( )
      input1 : objective line number
      input2 : total line number
      xtalk : peak crosstalk

PROCEDURE CROSSTALK(input1, input2, xtalk)
   begin
      include "MODAL_PARAMETERS"
         t2= max. effective time of flight of all modes + delta;
         t1= max. time of flight of all modes;
      PROCEDURE TOTALVOLTAGE(input1, input2, t2, vi)
         v2= absolute(vi);
      PROCEDURE TOTALVOLTAGE(input1, input2, t1, vi)
         v1= absolute(vi);
         xtalk = maximum(vi, v2);
   end_begin
```

(b)

Fig. 6. Graphical description and algorithm for the crosstalk noise determination. (a) Graphical description. (b) Algorithm for the peak crosstalk determination.

they have excellent agreement with SPICE simulations within roughly 5% error. The crosstalk noise expression can also be derived by using (14). Note, there are the negative peaks and positive peaks since the crosstalk signals are also oscillating [6], [53]. The signs may be changed with the opposite switching condition. Thus, the maximum of the absolute values of the first two peak points has to be determined for the maximum crosstalk. The negative peak occurs at the starting point of the slowest eigenmode while the positive peak approximately occurs at the end of the linear region of the slowest eigenmode. Note, the crosstalk is the most significant at the center line (victim line) when all the outer lines (aggressor lines) are switching from logic 0 to logic 1. Therefore, the maximum crosstalk can be readily determined by choosing the larger value between the negative peak and the positive peak, as shown in (22) at the bottom of the page. As long as the modeling is concerned with crosstalk noise, both the peak value and signal width is important. The crosstalk noise width can be very accurately determined with (14). Note, as shown in Fig. 6, the evaluated crosstalk (positive peak crosstalk) waveform deviates from the SPICE simulation a bit. This is

$$\mathrm{MAX}\left(\left|\sum_{k=1}^{n}\left\{s_{ik}\left(\sum_{j=1}^{n}s'_{kj}\cdot v_{sj}\right)\cdot p_k\left(t_{f(n)}^{-}\right)\right\}\right|,\left|\sum_{k=1}^{n}\left\{s_{ik}\left(\sum_{j=1}^{n}s'_{kj}\cdot v_{sj}\right)\cdot p_k\left(t_{f0(n)}+\delta_{(n)}\right)\right\}\right|\right). \tag{22}$$

TABLE IV
THE CROSSTALK FOR THREE-COUPLED LINES AND FIVE-COUPLED LINES

Line	↑0↑ crosstalk [V]		↑↑0↑↑ crosstalk [V]	
Length	SPICE	TWA	SPICE	TWA
1mm	1.176	1.5712	1.6705	2.1156
2mm	1.2022	1.5201	1.7357	2.0934
5mm	1.0829	1.3040	1.6241	1.8696
10mm	1.0153	1.0275	1.3867	1.5456

an inherent characteristic of the TWA technique. Therefore, the TWA technique may be empirically modified to improve the peak crosstalk noise evaluation. A possible modification is to select the maximum value by testing the estimated voltage values at several time points within the time interval, $\Delta\tau = \left(t_{f0(n)} + \delta_{(n)}, 3t_{f0(n)} - \delta_{(n)}\right)$. This reduces the error a small amount. The graphical interpretation and algorithms for the crosstalk determination are described in Fig. 6. The crosstalk noises for the three-coupled lines are investigated and summarized for the various input switching patterns in Table II. Further, the crosstalk noises of the three-coupled lines and the five-coupled lines with input switching patterns, "↑ 0 ↑" and "↑↑ 0 ↑↑," are also investigated and summarized in Table IV. The following transmission line parameters for the calculations are as follows.

$$[L] = \begin{bmatrix} 7.46 & 5.22 & 4.07 & 3.35 & 2.84 \\ 5.22 & 7.26 & 5.10 & 4.03 & 3.35 \\ 4.07 & 5.10 & 7.21 & 5.10 & 4.07 \\ 3.35 & 4.03 & 5.10 & 7.26 & 5.22 \\ 2.84 & 3.35 & 4.07 & 5.22 & 7.46 \end{bmatrix} \left[\frac{\text{nH}}{\text{cm}}\right]$$

$$[C] = \begin{bmatrix} 2.23 & -0.52 & -0.04 & -0.02 & -0.01 \\ -0.52 & 2.43 & -0.51 & -0.03 & -0.02 \\ -0.04 & -0.51 & 2.43 & -0.51 & -0.04 \\ -0.02 & -0.03 & -0.51 & 2.43 & -0.52 \\ -0.01 & -0.02 & -0.04 & -0.52 & 2.23 \end{bmatrix} \left[\frac{\text{pF}}{\text{cm}}\right]$$

$$[R] = \text{diag}\,[68.97] \left[\frac{\Omega}{\text{cm}}\right].$$

As it was shown, the crosstalk noise of the center line is really significant. The TWA-based crosstalk noise estimation is a bit larger than SPICE noise simulation although their differences are small. Further, the TWA technique assumes a step input. Thus, the TWA-based crosstalk-noise can be considered a good conservative design guide line. It is noteworthy that the crosstalk noise of the five-coupled lines (i.e., "↑↑ 0 ↑↑" switching) is much larger than that of three-coupled lines (i.e., "↑ 0 ↑" switching). This demonstrates that the inductive coupling due to the far-apart lines cannot be neglected in high speed interconnects. The TWA-technique models inductively coupled crosstalk very well.

Up to now, we considered only the typical cases in which the input signals switch from logic 0 to logic 1. However, there are other cases in which some of the input signals may switch from logic 0 to logic 1 while rest of them switch from logic 1 to logic 0. An example case, for three-coupled lines is shown in Fig. 7. In this particular case, i.e., the switching pattern of "↓↑↓," the signal waveform contains a spurious glitch rather than being monotonic. In practice, since this glitch signal may exceed 50%

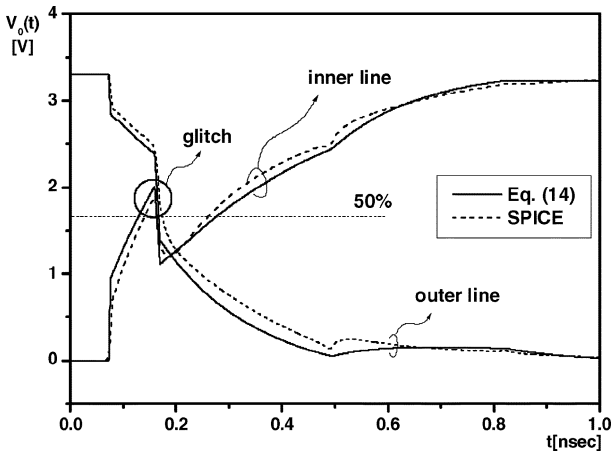


Fig. 7. The signal transient for the input switching pattern of "↓↑↓". The test circuit configuration is the same as in Fig. 2(a).

of the final value, this kind of waveform should be characterized with both the peak signal of the glitch and the main lobe of the signal. The analytical waveform determination for this special case is not simple since the signal variation is not dominated by a single eigenmode. Thus, the other eigenmodes, which may be different in magnitude as well as sign, have to be taken into account. Since the peak of the spurious glitch signal for the switching pattern of "↓↑↓" occurs at the instant the slowest eigenmode occurs, it can be readily determined as follows:

$$v_{i-\text{glitch}-\text{peak}} = v_i\left(t^-_{f(n)}\right) \approx \sum_{k=1}^{n}\left\{s_{ik}\left(\sum_{j=1}^{n} s'_{kj} v_{sj}\right) p_k\left(t^-_{f(n)}\right)\right\}. \quad (23)$$

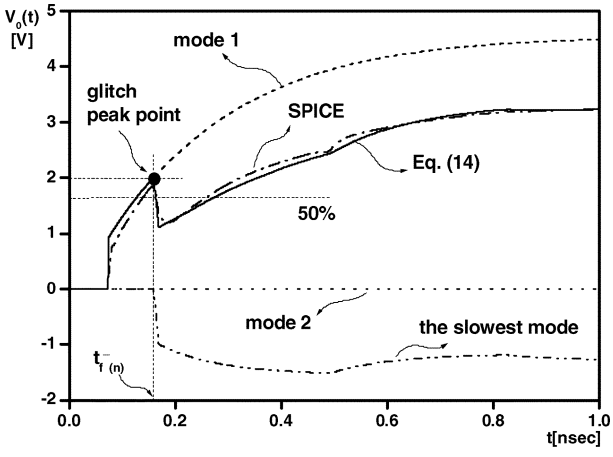
The graphical interpretation and algorithms for the glitch-peak determination are described in Fig. 8. If the $v_{i-\text{glitch}-\text{peak}}$ is less than the 50% of the final value, the 50% delay of the signal can be determined with an *RC*-response-like main lobe by using (18). However, if it is not the case, the signal delay due to the glitch has to be taken into account since the $v_{i-\text{glitch}-\text{peak}}$ may exceed the 50% of the final value. The glitch signal can be approximately linearized as

$$v_{\text{glitch}}(t) \approx \frac{v_i\left(t_{f0(1)}\right)}{\delta_{(1)}}\left(t - t^-_{f(1)}\right). \quad (24)$$

Thus, the 50% delay due to the glitch signal for the switching pattern of "↓↑↓" can be determined as

$$t_{50\%-\text{glitch}} = 0.5 v_{si} \cdot \frac{\delta_{(1)}}{v_i\left(t_{f0(1)}\right)} + t^-_{f(1)}. \quad (25)$$

In the case of the switching pattern of "↓↑↓", the signal delays and glitch peaks are investigated by varying the line length. They are summarized in Table V. It is noteworthy that the signal delay of this case is approximately two times larger than the previous nominal switching case (i.e., the case in which the input switching pattern is "0 ↑ 0"). Even for this case, the TWA-based modeling can provide an accurate prediction of signal delay and glitches.



(a)

```
Algorithm : GLITCH( )
    input1 : objective line number
    input2 : total line number
    glitch : peak voltage of a glitch

PROCEDURE GLITCH (input1, input2, glitch)
  begin
    include "MODAL_PARAMETER"
      t1= max. effective time of flight of all modes;
    PROCEDURE TOTALVOLTAGE(input1, input2, t1, vi)
      glitch= vi;
  end_begin
```

(b)

Fig. 8. Graphical description and algorithm for the glitch noise determination. (a) Graphical description. (b) Algorithm for the peak value of the glitch signal.

TABLE V
DELAY AND GLITCH FOR SWITCHING PATTERN OF "↓↑↓"

Line Length	Delay [psec]		Glitch Peak [V]	
	SPICE	TWA	SPICE	TWA
1mm	10.7	9.5	2.452	3.0690
2mm	18.9	16.9	2.4743	2.9691
5mm	51	46.4	2.2505	2.5470
10mm	258.4	275.6	1.8435	2.0068

Note, in general, modal decoupling of the multicoupled lines can be readily as well as accurately achieved for straight lossless line structures whatever their cross-sectional dimensions are (i.e., identical or nonidentical) [48]–[50]. However, if they are nonstraight lines which include vias and have different line lengths, decoupling may not be possible except for some limited cases [48], [49], [54]. In fact, since the modal resistance parameter matrix of lossy lines has nonzero off-diagonal parameters, they cannot be accurately decoupled for the TWA technique. Nonetheless, neglecting the off-diagonal components (which implicitly means neglecting the eddy current effect) of the modal resistance parameter matrix for most of the realistic structures, TWA technique can be usefully employed with marginal error.

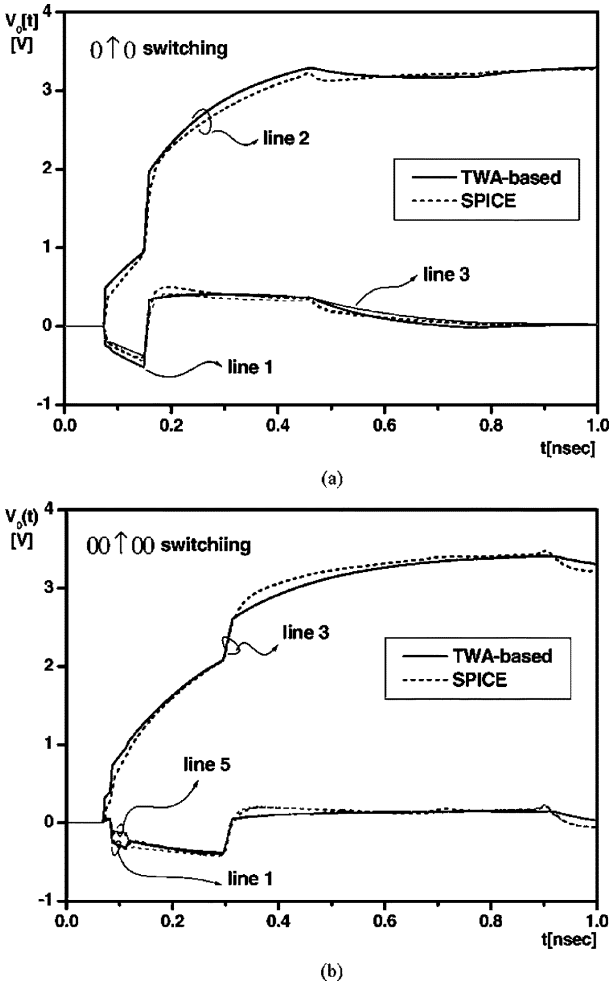


Fig. 9. The signal transient waveforms of the three-coupled and five-coupled nonidentical lines. (a) Three-coupled lines ($0 \uparrow 0$). (b) Five-coupled lines [$00 \uparrow 00$].

For three-coupled lines and five-coupled lines which have nonidentical cross-sectional dimensions, the TWA-based waveforms that neglect the off-diagonal elements of the modal resistance parameters are shown in Fig. 9. For the three-coupled lines, different line widths ($w_1 = 2.2$ μm, $w_2 = 2.5$ μm, and $w_3 = 1.5$ μm) are assumed. The line spacing between w_1 and w_2 is 1.3 μm and the line spacing between w_2 and w_3 is 1.8 μm. For the five-coupled lines, line widths of each line are $w_1 = 2$ μm, $w_2 = 3$ μm, $w_3 = 1.5$ μm, $w_4 = 2$ μm, and $w_5 = 5$ μm, respectively. The line spacings are 1.5 μm (between w_1 and w_2), 1 μm(between w_2 and w_3), 2 μm (between w_3 and w_4), and 1.5 μm (between w_4 and w_5), respectively. The transmission line parameters can be determined by using a commercial field solver as follows

$$[L] = \begin{bmatrix} 6.84 & 4.50 & 3.28 \\ 4.50 & 6.65 & 4.30 \\ 3.28 & 4.30 & 7.32 \end{bmatrix} \left[\frac{\text{nH}}{\text{cm}}\right]$$

$$[C] = \begin{bmatrix} 2.09 & -0.49 & -0.02 \\ -0.49 & 2.32 & -0.34 \\ -0.02 & -0.34 & 1.72 \end{bmatrix} \left[\frac{\text{pF}}{\text{cm}}\right]$$

$$[R] = \begin{bmatrix} 78.4 & 0 & 0 \\ 0 & 69.0 & 0 \\ 0 & 0 & 114.9 \end{bmatrix} \left[\frac{\Omega}{\text{cm}}\right] (3\text{lines})$$

TABLE VI
SIGNAL TRANSIENT CHARACTERISTICS OF NON-IDENTICAL LINES

model / items	3 lines			5 lines		
	SPICE	TWA-based	Error[%]	SPICE	TWA- based	Error[%]
50% delay	158.6 psec	155.7 psec	1.8	208.6 psec	212.4 psec	3.8
Overshoot	3.2265 V	3.2855 V	1.8	3.4780 V	3.4103 V	1.9
Crosstalk	0.5014 V	0.5215 V	4.0	0.4211 V	0.3819 V	9.3

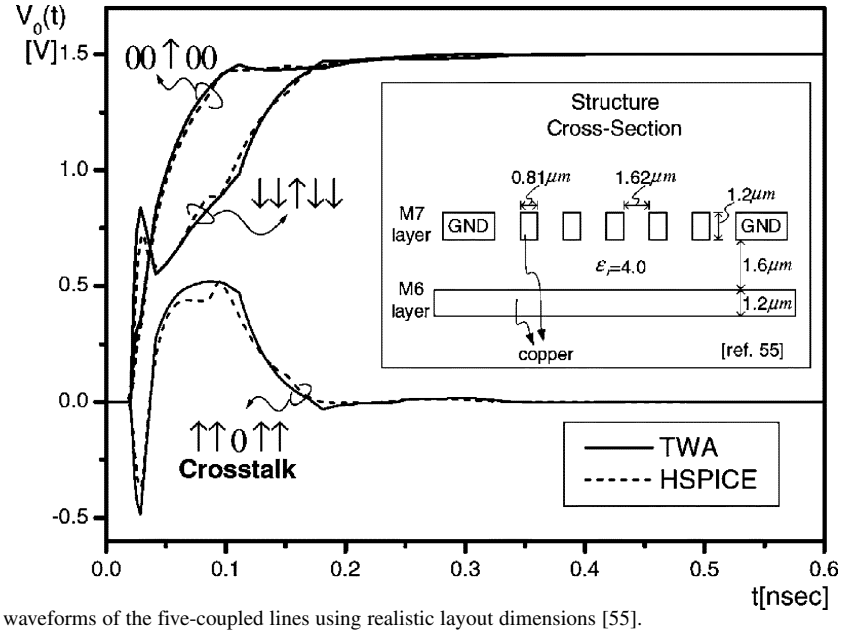


Fig. 10. The signal transient waveforms of the five-coupled lines using realistic layout dimensions [55].

$$[L] = \begin{bmatrix} 13.12 & 10.50 & 9.59 & 8.63 & 8.00 \\ 10.50 & 12.57 & 10.84 & 9.36 & 8.51 \\ 9.60 & 10.84 & 13.11 & 10.22 & 9.03 \\ 8.63 & 9.36 & 10.22 & 12.87 & 10.19 \\ 8.00 & 8.51 & 9.03 & 10.19 & 12.08 \end{bmatrix} \left[\frac{\text{nH}}{\text{cm}}\right]$$

$$[C] = \begin{bmatrix} 1.97 & -0.36 & 0 & 0 & 0 \\ -0.36 & 2.63 & -0.55 & 0 & 0 \\ 0 & -0.55 & 1.92 & -0.24 & 0 \\ 0 & 0 & -0.24 & 2.01 & -0.35 \\ 0 & 0 & 0 & -0.35 & 3.23 \end{bmatrix} \left[\frac{\text{pF}}{\text{cm}}\right]$$

$$[R] = \begin{bmatrix} 86.2 & 0 & 0 & 0 & 0 \\ 0 & 57.5 & 0 & 0 & 0 \\ 0 & 0 & 114.9 & 0 & 0 \\ 0 & 0 & 0 & 86.2 & 0 \\ 0 & 0 & 0 & 0 & 34.5 \end{bmatrix} \left[\frac{\Omega}{\text{cm}}\right] \quad (5\text{lines}).$$

As it was expected, the signal integrity simulation due to the nonidentical transmission line structure introduced more error than that of the simulation structure with identical lines. Nonetheless, the TWA-based signal transients for both three-coupled lines and five-coupled lines have a reasonably good agreement with SPICE simulations. The characteristics of the nonidentical lines are summarized in Table VI.

Note, in previous examples, the inductance effect was unrealistically exaggerated (note that $Q \approx 1$) just like the inductance-dominant global interconnect lines. That is, even if the examples are not realistic, they can explain all the realistic cases since the inductances are larger than realistic ones. Note, the smaller the inductance values, the more accurate the TWA technique. For a more realistic example, using the structures as shown in [55] (see the [55, Fig. 30]), TWA-based signal transients are investigated. They show excellent agreements with SPICE simulation results as shown in Fig. 10 and Table VII. In this realistic example, the signal integrity parameters such as delay, crosstalk, and overshoot can be accurately estimated within 5% error.

TABLE VII
SIGNAL INTEGRITY CHARACTERISTICS USING REALISTIC LAYOUT DIMENSIONS [55]

Items / model	SPICE	TWA	Error[%]
50% delay	40.5psec	39.3psec	-2.96
(worst)	(69psec)	(71.4psec)	(3.48)
Overshoot	1.4284V	1.4361V	0.54
Crosstalk	0.5174V	0.51772V	0.06
Glitch	0.723V	0.839V	16.04

In general, the proposed TWA-based signal integrity models and algorithms provide the signal delay with approximately 10% error for the strongly inductive-coupled *RLC* lines as shown in Tables I–VI. A glitch which is mainly due to the inductive crosstalk in the cross-coupled switching case always occurs. When considering the glitch signal, the model somewhat overestimates the peak value of the glitch signal with approximately 25% error.

Finally, in order to show the computation-time-efficiency of the models, we compared the execution time of the models with

TABLE VIII
COMPARISON OF THE EXECUTION TIME OF THE MODELS WITH SPICE SIMULATION

items / model	3-lines [sec]	5-lines [sec]	Output
SPICE	29	65	Waveform
Eq. (17)	0.03	0.04	50% delay
Eq. (21)	0.03	0.04	Overshoot
Eq. (22)	0.03	0.04	Crosstalk

SPICE. SPICE simulations have been performed with 500-segment model for interconnect lines while the model-based calculations have been done with MATLAB 5.3 program in a PC (which employs Pentium IV 2.4 GHz system). The CPU execution time is compared in Table VIII. As it was shown, the models are 1000 times faster than SPICE simulation for three-coupled lines. The difference is significantly increased with the increasing the numbers of lines. That is, it is 1600 times faster than the SPICE simulation for five-coupled lines.

V. CONCLUSION

In this work, new efficient signal integrity models and algorithms for inductance-effect-prominent multicoupled *RLC* interconnect lines are developed in an analytic manner by using TWA-techniques. Since they are the closed form models, the signal transient characteristics of multicoupled lines such as delay, crosstalk, ringing, and glitches can be very efficiently as well as accurately determined. In the multicoupled lines, the signal transient characteristics are correlated in a complicated fashion with the input switching patterns. Nonetheless, the TWA-based models can afford to efficiently provide signal transient characteristics due to the input switching patterns. It was shown that the models have excellent agreement with SPICE simulation while the proposed technique is several thousand times faster than SPICE simulation. Further, it can be usefully employed even for nonidentical lines with marginal error.

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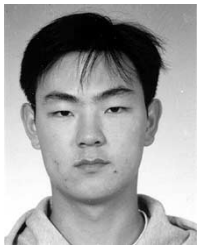

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