Analytical Surface Potential-Based Compact Model for Independent Dual Gate a-IGZO TFT

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***Abstract*— A surface potential-based compact model for independent dual gate (IDG) amorphous In-Ga-Zn-O thin-film transistors (IDG a-IGZO TFTs) is proposed here. The transport theories of percolation conduction, trap-limited conduction (TLC), and variable range hopping (VRH) in extended and localized states are first considered simultaneously via Schroder method, obtaining a physical description of the transport mechanism under different conditions of temperature and gate voltage. Moreover, a single formulation of front and back surface potentials which is valid and extremely accurate in all operation regimes is developed. Based on the transport theories and surface potentials, the complete compact model is developed and verified using both numerical simulation and experiment with an excellent agreement, and the threshold compensation effect is also included. Finally, the compact model is coded in Verilog-A, and implemented in a vendor CAD environment, which suggested that the proposed model can be successfully applied to circuit design.**

***Index Terms*— Analytical models, independent dual gate (IDG) amorphous In-Ga-Zn-O thin-film transistors (IDG a-IGZO TFTs), Schroder method, surface potential, threshold compensation effect.**

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I. Introduction

On account of the extremely low leakage current and the possibility of low-temperature fabrication, amorphous In-Ga-Zn-O thin-film transistors (a-IGZO TFTs) are under active research and development in the circuit application such as flexible display, memory, and 3-D integration [1]–[3]. Especially, the independent dual gate (IDG) a-IGZO TFTs have become the key choice in the industry due to its controllability of turn-on voltage and enhancement of ON/OFF-current ratio [4]–[6]. To further effectively evaluate circuit performance, it is significant to have an accurate compact model describing the physical device behavior. However, due to the amorphous disordered structure, charge transport in a-IGZO exhibits complex behavior, which also brings difficulty in calculating the surface potentials, and the latter is the key issue in the modeling of IDG transistors [7], [8]. To our understanding, the surface potential-based completely compact model of IDG a-IGZO TFT considering amorphous structure and charge transport is still lacking.

In this article, we develop a physics-based compact model for IDG a-IGZO TFT considering both traps and free electrons in an analytical way. With the combination of percolation conduction, trap-limited conduction (TLC), variable range hopping (VRH) for transport mechanism, and a new capacitance calculation method for dual-gate transistors, the model accurately replicates the experimental data. Also, the compact model is evaluated for circuit design in SPICE.

II. Modeling

A. Surface Potential Calculation

The geometric definition and schematic view of equivalent capacitance for IDG a-IGZO TFT investigated here are illustrated in Fig. 1. Definitions of constants and variables used in this paper are summarized in Table I. For amorphous oxide semiconductors, the total carrier concentration $n(z)$ is given by the sum of the carrier concentration in the extended states and concentration in the localized states as [9], [10]

$$n(z) = \int_{-\infty}^{\infty} \frac{g(E)}{1+\exp\left(\frac{E-E_F(z)}{k_BT}\right)} dE \tag{1}$$

$$g(E) = \begin{cases} g_c\sqrt{E+\left(\dfrac{N_t}{k_BT_0g_c}\right)^2} & E>0 \\ \dfrac{N_t}{k_BT_0}\exp\left(\dfrac{E}{k_BT_0}\right) & E<0 \end{cases} \tag{2}$$

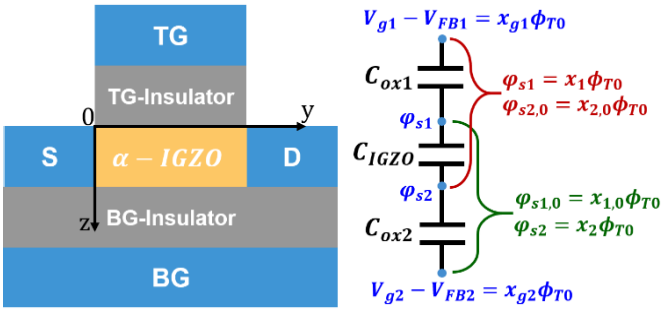

Fig. 1. Geometric definition for IDG a-IGZO TFT compact model, the *z*-axis is the vertical channel direction, and the *y*-axis is the parallel channel direction (left) and the electric potential distribution and equivalent capacitances between TG and BG (right).

where $g(E)$ is the density of states (DOS) energy distribution, $E = 0$ corresponds to the mobility edge, the first term on the right-hand side of (2) describes the density of extended states with the positive E [11], and the second term describes the density of localized states with the negative E, which is related to the disorder and the Urbach tail [12], N_t is the total concentration of localized states, the value $g_c = 1.4\times10^{21}$ $\text{cm}^{-3}\text{eV}^{-3/2}$ has been reported for a-IGZO thin films [13], k_B is Boltzmann's constant, T_0 is the characteristic temperature of the exponential DOS, and $E_F(z)$ is the quasi-Fermi level.

Accurate surface potentials for IDG MOSFET have been proposed in [14]–[17]. However, those methods are applicable to only free carriers or need iterative resolution of the Poisson equation. Here, we developed a very accurate direct calculation of surface potentials, which is an extension of the methodology presented in [14] to the case where the channel material becomes a-IGZO, accounting for both localized and extended states.

First, we use the method of equivalent capacitance illustrated in Fig. 1 to obtain an approximate initial solution in the case of traps only, because traps prevail for a broad range of working gate voltage.

$$\begin{cases} x_{1(2),\text{sat}} = x_n + \ln\left(\dfrac{k_{1(2)}+\dfrac{k_{2(1)}}{1+k_{2(1)}}}{0.25A_0}\right) + \ln\left(\dfrac{\frac{\Delta x}{2}}{\tanh\left(\frac{\Delta x}{2}\right)}\right) + 3 \\ x_{1(2),\text{sub0}} = x_{g1(2)} + \dfrac{k_{2(1)}}{k_1+k_2+k_1k_2}\left(x_{g2(1)} - x_{g1(2)}\right) \\ x_{1(2),0} = x_{1(2),\text{sub0}} - 3\ln\left(1+\exp\left(\dfrac{x_{1(2),\text{sub0}} - x_{1(2),\text{sat}}}{3}\right)\right) \\ x_{1(2),\text{sub}} = \dfrac{x_{2(1),0} + k_{1(2)}x_{g1(2)}}{1+k_{1(2)}} \\ x_{1(2)} = x_{1(2),\text{sub}} - 3\ln\left(1+\exp\left(\dfrac{x_{1(2),\text{sub}} - x_{1(2),\text{sat}}}{3}\right)\right) \end{cases} \tag{3}$$

which is identical to [14, (13)–(24)], where $\Delta x = x_{1,\text{sat}} - x_{2,\text{sat}} = \ln((1+k_1)/(1+k_2))$ is the difference in the saturation value of normalized potentials between the top and bottom surfaces, and $A_0 = ((2et_{\text{IGZO}}N_t\Gamma(1-(T/T_0))\Gamma(1+(T/T_0)))/(C_{\text{IGZO}}\phi_{T0})$, with e is the elementary charge. However, there are still some errors in the approximate surface potential calculation because the carrier in extended states is missing. To improve its accuracy, we use the Schroder series to introduce the contribution of free electrons into the correction.

TABLE I
NOTATIONS USED IN THIS ARTICLE

Symbol	Definition	Dimensionless counterpart
ϕ_T	thermal potential	
ϕ_{T0}	characteristic thermal potential	$t = \phi_{T0}/\phi_T$
φ_{s1}	top surface potential	$x_1 = \varphi_{s1}/\phi_{T0}$
φ_{s2}	bottom surface potential	$x_2 = \varphi_{s2}/\phi_{T0}$
V_{FB1}	flat-band voltage of top surface	
V_{FB2}	flat-band voltage of bottom surface	
V_{g1}	top gate voltage	$x_{g1} = (V_{g1} - V_{FB1})/\phi_{T0}$
V_{g2}	bottom gate voltage	$x_{g2} = (V_{g2} - V_{FB1})/\phi_{T0}$
V_{ch}	channel voltage	$x_n = V_{ch}/\phi_{T0}$
V_s	source bias	$x_s = V_s/\phi_{T0}$
V_d	drain bias	$x_d = V_d/\phi_{T0}$
ε	dielectric constant of a-IGZO	
t_{IGZO}	active layer thickness	
C_{IGZO}	depleted body capacitance	
C_{ox1}	top gate dielectric capacitance	$k_1 = C_{ox1}/C_{IGZO}$
C_{ox2}	bottom gate dielectric capacitance	$k_2 = C_{ox2}/C_{IGZO}$
Q_{g1}	top gate charge density	$q_1 = Q_{g1}/(C_{ox1}\phi_{T0})$
Q_{g2}	bottom gate charge density	$q_2 = Q_{g2}/(C_{ox2}\phi_{T0})$
α	normalized coupling charge	

Second, by separating variables and integrating Poisson equation from the top surface to an arbitrary point across the thickness, we obtain

$$\alpha^2 = k_{1(2)}^2 q_{1(2)}^2 - A_0 e^{x_{1(2)}-x_n} - B_0 e^{t\left(x_{1(2)}-x_n\right)} \tag{4}$$

$$\alpha^2 = t_{\text{IGZO}}^2\left(\frac{\partial x}{\partial z}\right)^2 - A_0 e^{x-x_n} - B_0 e^{t(x-x_n)} \tag{5}$$

where $B_0 = ((2et_{\text{IGZO}}N_t v_0\tau_0))/(tC_{\text{IGZO}}\phi_{T0}))$, with τ_0 is the lifetime of carriers and v_0 is the attempt-to-escape frequency; x is the electrostatic potential which depends on (y, z) normalized by ϕ_{T0}. Only one carrier can be considered in the calculation of [13], and we use Schroder series to extend the method to include carriers of both states.

Defining the complex function $a(y,z)$ by $\alpha coth[a(y,z)] = -t_{\text{IGZO}}(\partial x/\partial z)$, and substituting it into (5), we obtain (6) that is equal to zero. Think of $a(y,z)$ as a linear function of z and define $k_a = (\partial a/\partial z)$.

$$f(k_a) = k_a - \frac{\alpha}{2t_{\text{IGZO}}} - \frac{B_0 C_{\text{IGZO}} t}{2t_{\text{IGZO}}}\left[\frac{t_{\text{IGZO}}^2 k_a^2(\phi_{T0}-\phi_T)}{\alpha C_{\text{IGZO}}\phi_{T0}}\right]^{1-t} \times\left(\frac{\alpha t - 2t_{\text{IGZO}}k_a}{A_0 C_{\text{IGZO}} t}\right)^t \tag{6}$$

$$\delta = -\frac{f(k_a)}{f'(k_a)}\left[1 + \frac{f''(k_a)}{2f'(k_a)}\frac{f(k_a)}{f'(k_a)}\right], \quad k_a = \frac{\alpha}{2t_{\text{IGZO}}} + \delta \tag{7}$$

$$F(x_1) = \left[k_1q_1 + \alpha\cdot\coth\left(\frac{\alpha}{2} + t_{\text{IGZO}}\cdot\delta\right)\right](k_1q_1 + k_2q_2) - A_0 e^{x_1-x_n} - B_0 e^{t(x_1-x_n)} \tag{8}$$

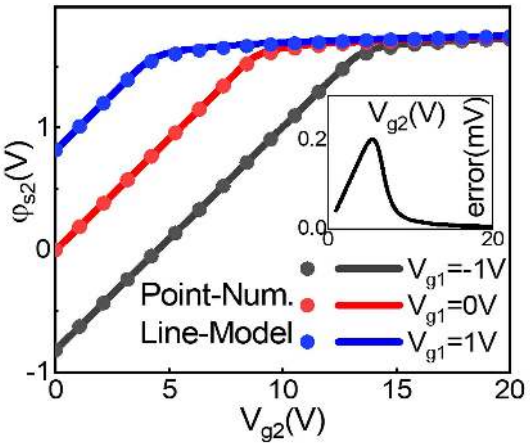

Fig. 2. Agreement between the analytical solutions calculated by the model and numerical results for φ_s with different TG voltage, with the error is inserted.

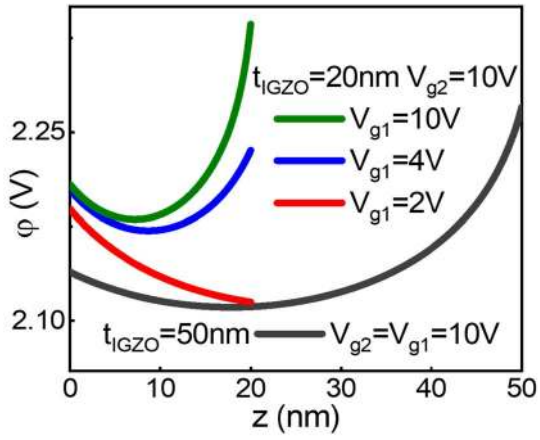

Fig. 3. Electrostatic potential (φ) as a function of distance in the vertical channel direction with different TG biases and active layer thicknesses.

$$q_2 = x_{g2} - x_1 + 2ln\left(k_1 q_1 + \alpha \cdot \coth\left(\frac{\alpha}{2} + t_{\mathrm{IGZO}} \cdot \delta\right)\right) - 2\ln\left(\alpha \cdot \mathrm{csch}\left(\frac{\alpha}{2} + t_{\mathrm{IGZO}} \cdot \delta\right)\right). \quad (9)$$

Through estimating the orders of magnitude, the last term is much smaller than the second term on the right side of (6). In the case, we use the second term as the basic solution and use Schroder series as the correction term, embodied in (7).

Combining the coupled equations, we can work with real unknowns only and build a unique (8) to be solved with x_1 as a variable. Then, thanks to a robust analytical procedure involving two successive corrections on x_1 based on the above approximation, the analytical solutions of the surface potentials can be written as

$$x_{11} = x_1 - \frac{F(x_1)}{F'(x_1) - \frac{F(x_1)}{F'(x_1)}\frac{F''(x_1)}{2}} \quad (10)$$

$$\varphi_{s1} = \phi_{T0}\left(x_{11} - \frac{F(x_{11})}{F'(x_{11}) - \frac{F(x_{11})}{F'(x_{11})}\frac{F''(x_{11})}{2}}\right) \quad (11)$$

$$\varphi_{s2} = \phi_{T0}(x_{g2} - q_2). \quad (12)$$

Fig. 2 compares the analytical solutions calculated by the model and numerical results of the bottom surface potentials. The percentage error is always below 0.01%.

In addition, Fig. 3 illustrates the distribution of electrostatic potential in the vertical channel direction with different top-gate (TG) biases and active layer thicknesses, which is obtained by numerical calculation, showing the thinner active layer and higher TG voltage, the larger potential, which leads to a better performance of device.

B. Mobility Model

Because IGZO has conduction band fluctuations in the amorphous phase, this leads to localized states in the subgap and potential barriers above the conduction band minima (E_m). At low gate voltages, E_F lies in the localized tail states, so electrons are trapped. They are released and move forward by thermal excitation. Therefore, TLC prevails for a broad range of temperatures, whereas VRH becomes dominant at lower temperature because carrier activation is reduced. At high gate voltages, E_F turns into the conduction band,

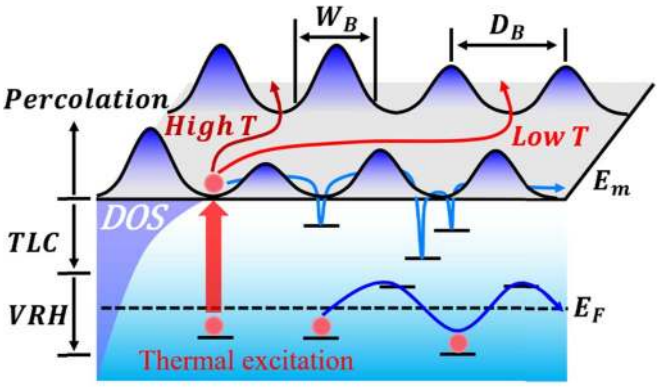

Fig. 4. Schematic view of the percolation conduction (when $E_F > E_m$), TLC (at high temperature when $E_F < E_m$) and VRH (at low temperature when $E_F < E_m$) transport mechanism [18].

and percolation conduction occurs. In high temperature case, an electron chooses a shorter but higher barrier path, due to the higher thermal energy and more localized states that are occupied. At low temperature, an electron chooses a longer but lower barrier path, as shown in Fig. 4. So carrier transport in IGZO is carried out by both traps in localized states and free electrons in extended states.

The temperature-dependent mobility model of the IDG a-IGZO TFTs contains three physical transport mechanisms, TLC, percolation conduction, and VRH [18], which can cover various temperature and gate voltage ranges

$$\mu_{\mathrm{tLC}} = \mu_b^* A^* \left(V_{g1} - V_{\mathrm{FB1}} + V_{g2} - V_{\mathrm{FB2}}\right)^{2(T_0/T-1)} \quad (13)$$

$$\mu_{\mathrm{PERC}} = \mu_b^* B^* \left(V_{g1} - V_{P1} + V_{g2} - V_{P2}\right)^{4[(D_B - W_B)/D_B]} \quad (14)$$

$$\mu_{\mathrm{VRH}} = \mu_0 C^* \exp\left(\left(\frac{T_1}{T}\right)^{\frac{1}{4}}\right)\left(V_{g1} - V_{T1} + V_{g2} - V_{T2}\right)^{\gamma} \quad (15)$$

where A^*, B^*, and C^* are related to N_t and T_0, and μ_b^* is the band mobility scaled by the percolation term in terms of potential barrier height and variance, μ_0 is a reference mobility for hopping conduction, $V_{P1(2)}$ is the gate voltage where the transition between TLC and percolation takes place when $E_F = E_m$, T_1 is the associated characteristic temperature, $(D_B - W_B)/D_B$ is a spatial coherence ratio of the potential

barriers, and γ is a power parameter associated with the density of tail states. In all cases, the mobility obeys a universal power law as a function of gate voltage.

C. Current and Capacitance Model

A drain current model based on Pao–Sah's double integral under the assumption of the gradual channel approximation for long-channel IDG devices is given by [19]–[21]

$$I_{ds} = -\mu_{\text{eff}}\frac{W}{L}\int_0^{V_{ds}} Q_i dV_{ch} = \mu_{\text{eff}}\frac{W}{L}\int_0^{V_{ds}}\int_{\varphi_{s2}}^{\varphi_{s1}} \frac{\text{en}}{E} d\varphi dV_{ch} \tag{16}$$

$$\frac{\text{en}}{E} = \frac{1}{2\varepsilon E}C_{\text{IGZO}}^2\phi_{T0}^2\frac{\partial\alpha^2}{\partial V_{ch}} - \varepsilon\frac{\partial E}{\partial V} \tag{17}$$

$$E = \pm\frac{1}{\varepsilon}\sqrt{\alpha + \frac{A_0\exp\left(\frac{\varphi - V_{ch}}{\phi_{T0}}\right)}{C_{\text{IGZO}}^2\phi_{T0}^2} + \frac{B_0\exp\left(\frac{\varphi - V_{ch}}{\phi_T}\right)}{C_{\text{IGZO}}^2\phi_{T0}^2}} \tag{18}$$

where W is the channel width, L is the channel length, Q_i is the total accumulated layer charge density which is expressed as an integral form, V_{ch} is the channel voltage that varies from 0 to V_{ds}, $and E$ is the electric field intensity, which plays a major role on the top surface $E_1 = (C_{\text{ox1}}/\varepsilon)(V_{g1} - \varphi_{s1})$ and the bottom surface $E_2 = -(C_{\text{ox2}}/\varepsilon)(V_{g2} - \varphi_{s2})$.

The effective mobility μ_{eff} is determined by different conduction regimes at different temperatures and gate biases. μ_{TLC} can prevalent at $\Delta\text{V} = V_{g1} - V_{P1} + V_{g2} - V_{P2} < 0$, whereas percolation can be dominant at $\Delta V > 0$ at room temperature and above

$$\mu_{\text{eff}} = S(-\Delta V)\mu_{\text{TLC}} + S(\Delta V)\mu_{\text{PERC}} \tag{19}$$

where the two mobility expressions are connected by the Sigmoid function $S(-\Delta V)$ and $S(\Delta V)$, and μ_{TLC} is replaced by μ_{VRH} at low temperature.

The drain current model is formulated by substituting the front and back surface potentials at the source and drain, and then turn (16) into a quadratic integral. After some algebraic manipulations, the final expression of drain current is set up with four parts: top surface (I_{s1}), bottom surface (I_{s2}), interfacial coupling (I_{coup}), and subthreshold (I_{sub}), written as

$$I_{ds} = \mu_{\text{eff}}\frac{W}{L}\left(I_{s1} + I_{s2} + I_{\text{coup}} + I_{\text{sub}}\right) \tag{20}$$

$$I_{s1} = C_{\text{ox1}}\left[\begin{array}{l}\left(V_{g1} - V_{\text{FB1}} + 2\phi_T\right)(\varphi_{s1d} - \varphi_{s1s}) \\ -0.5\left(\varphi_{s1d}^2 - \varphi_{s1s}^2\right)\end{array}\right] \tag{21}$$

$$I_{s2} = C_{\text{ox2}}\left[\begin{array}{l}\left(V_{g2} - V_{\text{FB2}} + 2\phi_T\right)(\varphi_{s2d} - \varphi_{\text{s2s}}) \\ -0.5\left(\varphi_{s2d}^2 - \varphi_{s2s}^2\right)\end{array}\right] \tag{22}$$

$$I_{\text{coup}} = \frac{C_{\text{IGZO}}}{2\phi_{t0}^2}\left(\alpha_s^2 - \alpha_d^2\right) \tag{23}$$

$$I_{\text{sub}} = 2eN_t\Gamma\left(1 - \frac{T}{T_0}\right)\Gamma\left(1 + \frac{T}{T_0}\right)(\phi_{t0} - \phi_t)t_{\text{IGZO}} * \exp\left(\frac{\varphi_{s1s} + \varphi_{s2s}}{2\phi_{t0}}\right)\left[1 - \exp\left(-\frac{V_{ds}}{\phi_{t0}}\right)\right]. \tag{24}$$

Simulating the transient mode requires not only the drain current behavior, but also a correct compact model of terminal charge and trans-capacitance. We propose a new method to get analytical solution of terminal charges for IDG devices. The core idea is to introduce the accumulated layer charge into the formula with two expressions. One is obtained by multiplying the capacitance of the gate dielectric layer by the potential drop on it (25). The other is an integral form used in calculating drain current model.

$$Q_i = -C_{\text{ox1}}\left(V_{g1} - V_{\text{FB1}} - \varphi_{s1}\right) - C_{\text{ox2}}\left(V_{g2} - V_{\text{FB2}} - \varphi_{s2}\right) \tag{25}$$

$$Q_g = -\frac{\mu W^2}{I_{ds}}\int_0^{V_{ds}} Q_i\int_{\varphi_{s2}}^{\varphi_{s1}}\frac{\text{en}}{E}d\varphi dV_{ch} = WL\left(\frac{G_1 + G_2}{3C_{ox1}\left(A^2 - B^2\right) + 3C_{\text{ox2}}\left(C^2 - D^2\right)}\right) \tag{26}$$

$$G_1 = 2C_{\text{ox1}}^2\left(A^3 - B^3\right) + 3C_{\text{ox1}}C_{\text{ox2}}\left(A^2C - B^2D\right) \tag{27}$$

$$G_2 = 2C_{\text{ox2}}^2\left(C^3 - D^3\right) + 3C_{\text{ox1}}C_{\text{ox2}}\left(AC^2 - BD^2\right) \tag{28}$$

where $a = V_{g1} - V_{\text{FB1}} - \varphi_{s1s}$, $B = V_{g1} - V_{\text{FB1}} - \varphi_{s1d}$, $C = V_{g2} - V_{\text{FB2}} - \varphi_{s2s}$, and $D = V_{g2} - V_{\text{FB2}} - \varphi_{s2d}$, G_1 represents the TG charges and G_2 corresponds to the bottom-gate (BG) charges, that is, the expression of Q_{g1} can be separated from (26) by ignoring the effect of G_2, and Q_{g2} can be obtained with $G_1 = 0$. In particular, the denominator of the above gate charge expression is equal to 0 when the same voltages are applied at source and drain ($A = B$ and $C = D$). Under such conditions, the terms $(A - B)$ and $(C - D)$ with values of 0 are regarded as the same infinitely small quantities and L'Hospital's rule is used to deal with the limit.

$$Q_{g(V_{ds}=0)} = WL\left(\frac{G_{11} + G_{22}}{3C_{\text{ox1}}(A + B) + 3C_{\text{ox2}}(C + D)}\right) \tag{29}$$

$$G_{11} = 2C_{\text{ox1}}^2\left(A^2 + AB + B^2\right) + 3C_{\text{ox1}}C_{\text{ox2}}(A*C + B*D) \tag{30}$$

$$G_{22} = 2C_{\text{ox2}}^2\left(C^2 + CD + D^2\right) + 3C_{\text{ox1}}C_{\text{ox2}}(A*C + B*D). \tag{31}$$

Correspondingly, the expressions of Q_{g1} and Q_{g2} in the case of $V_{ds} = 0$ can be separated from (29) as mentioned above. According to Ward's charge-partitioning scheme and total charge neutrality requirement, the drain charge Q_d and source charge Q_s can be expressed as

$$Q_d = WL\left(\frac{2(D_1 + D_2 + D_3)}{\left(C_{\text{ox1}}\left(A^2 - B^2\right) + C_{\text{ox2}}\left(C^2 - D^2\right)\right)^2}\right) \tag{32}$$

$$D_1 = \frac{1}{5}C_{\text{ox1}}^3\left(A^5 - B^5\right) + \frac{1}{5}C_{\text{ox2}}^3\left(C^5 - D^5\right) \tag{33}$$

$$D_2 = \frac{1}{12}C_{\text{ox1}}^2C_{\text{ox2}}\left(3A^4C - 3B^4D + 10A^3C^2 - 10B^3D^2\right) \tag{34}$$

$$D_3 = \frac{1}{12}C_{\text{ox1}}C_{\text{ox2}}^2\left(3AC^4 - 3BD^4 + 10A^2C^3 - 10B^2D^3\right) \tag{35}$$

$$Q_s = -Q_d - Q_g. \tag{36}$$

In the case where the denominator becomes 0, the same approach used for dealing with Q_g is also applicable for Q_d and Q_s. Finally, the capacitance model can be calculated by

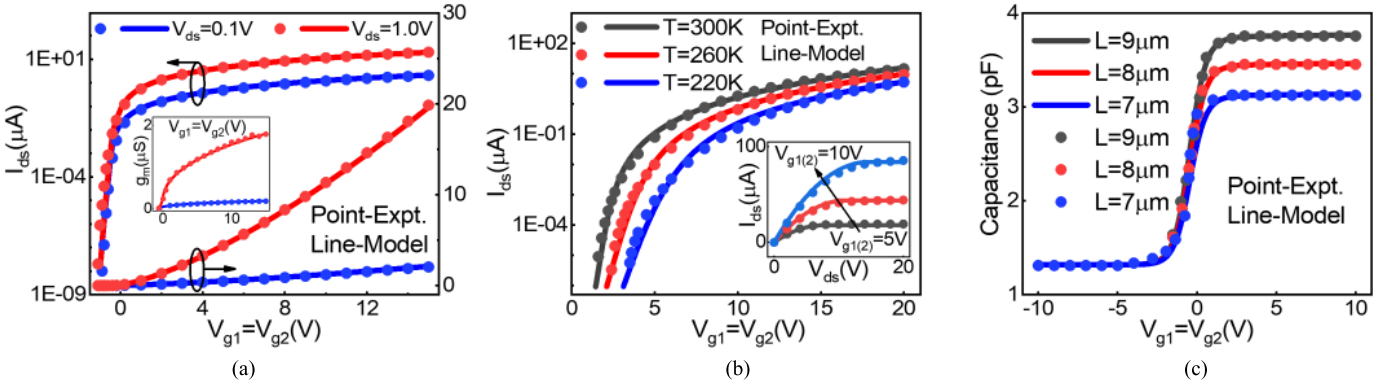

Fig. 5. Comparison between the calculated and experimental data for (a) transfer characteristics of the IDG a-IGZO TFT (both in conventional and logarithmic coordinates, and the corresponding transconductance curves (g_m) are inserted), (b) transfer characteristics at different temperatures (output characteristics is inserted), and (c) total gate capacitance of IDG a-IGZO TFT under various channel lengths. Good agreement has been achieved between the model and the measurement.

the derivation of terminal charges.

$$C_{i,j}=\pm\frac{\partial Q_i}{\partial V_j} \tag{37}$$

where i and j denote the transistor terminal: TG, BG, source, or drain. The negative sign is used when $i \neq j$. The overlap capacitance should also be considered in the model to account for the limitations in the TFTs structure and process. Consequently, the total TG-source capacitance can be expressed as

$$C_{\text{total\_}g1s} = C_{\text{g1s}} + C_{\text{g1so}} \tag{38}$$

where C_{g1so} is the TG-source overlap capacitance calculated as $C_{\text{g1so}} = C_{\text{ox1}} W L_{\text{overlap}}$ and L_{overlap} is the overlap length, which is set to 2μm to take into account of the fabrication process. Other total gate–source/drain capacitance can be obtained in a similar way.

III. Model Validation

To obtain experimental data, we fabricated IDG a-IGZO TFTs. The TG is indium-zinc oxide that is deposited by sputtering at room temperature, and all other metal electrodes are made of molybdenum, deposited by sputtering at 200 °C. The BG-insulator is a bilayer of SiN_x (100 nm) and SiO_2 (150 nm), both deposited by plasma-enhanced chemical vapor deposition (PECVD) at 200 °C. The 100-nm-thick etch stopper and the passivation layer [SiO_2 (100 nm) / SiN_X (100 nm)] make up the TG-insulator; and these three layers are also deposited at 200 °C by PECVD. The 20-nm-thick active layer (a-IGZO) is deposited by sputtering at 200 °C using a polycrystalline IGZO target (InO_3: Ga_2O_3: ZnO = 1 : 1 : 1 mol%). TFTs with channel width $W = 50\mu m$ and channel length $L = 20\mu m$ were measured for the verification of current model, and $W = 1000\mu m/L = 7 \sim 9\mu m$ for Capacitance Model.

Fig. 5(a) and the inset in (b) show a comparison between the calculated and the experimental data for the transfer and output characteristics. The excellent agreement validates our model. Furthermore, the transfer characteristics in the linear coordinate system support the accuracy of the model

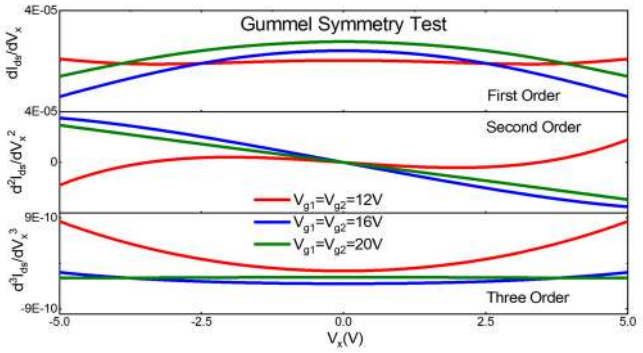

Fig. 6. Gummel symmetry test for the 1-, 2-, and 3-order derivatives of the drain current under various gate voltages ($V_{g1} = V_{g2} = 12$, 16, 20 V).

in the linear region, and the transfer characteristics in the semi-logarithmic coordinate system demonstrate the accuracy of the model in the subthreshold region. The key physical parameters are as follows: $C_{\text{IGZO}} = 4.427 \times 10^{-7}$ F/cm^2, with $t_{\text{IGZO}} = 20$ nm and $\varepsilon = 10 \times 8.854\times10^{-12}$ F/m. $C_{\text{ox1}} = 1.17 \times 10^{-8}$ F/cm^2, which is reasonable considering that the thickness of the top oxide layer in our device is 300 nm and $C_{\text{ox2}} = 1.4 \times 10^{-8}$ F/cm^2 with 250-nm-thick BG insulator. At room temperature, the TLC-dominated mobility-related parameter T_0 was extracted as 410 K, N_t in our model has been extracted from the subthreshold swing (SS) of the experimental transfer curves as 10^{18} cm^{-3}, andV_{FB1} and V_{FB2} were set to -0.2 V and -0.5 V, respectively. The parameters in percolation are $V_{P1} = V_{P2} = 10\ V$ and $(D_B - W_B)/D_B = 0.025$. The product of escape frequency υ_0 and lifetime of carriers τ_0 can be extracted as 1. Fig. 5(b) shows a comparison between the calculated and experimental data at different temperatures, and the accurate match means that the model can adapt to various physical states. At low temperature, the VRH-dominated mobility-related parameter T_1 was extracted as 948 K, and $\gamma = 2.5$. Fig. 5(c) shows that the model fits well with the experiments of capacitance in different channel lengths.

Moreover, the continuity and symmetry characteristics must be preserved to achieve convergence between simulation and analysis in IDG a-IGZO TFT-based circuits. To qualify as

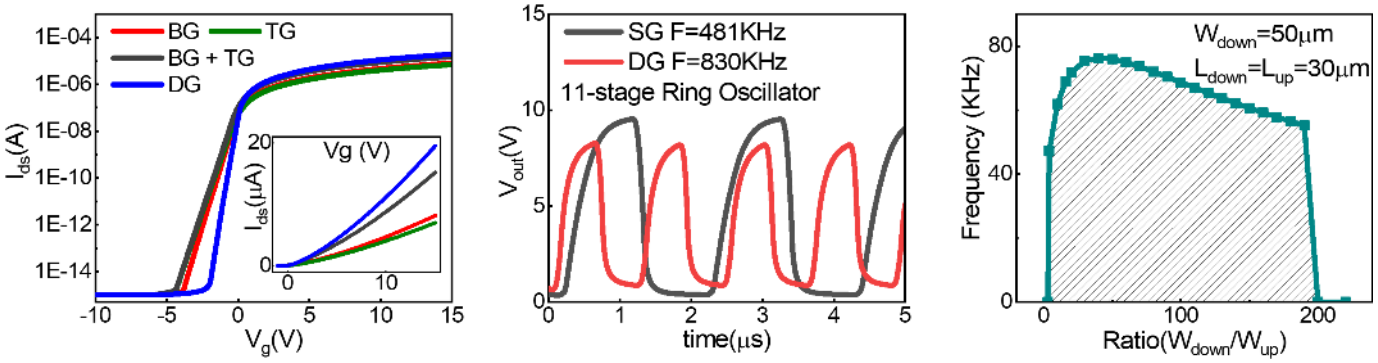

Fig. 7. (a) Transfer characteristics curves under BG, TG, and DG bias sweep conditions. The driving current and SS are both greatly improved in DG mode. (b) Typical output waveforms of SG- and DG-driven ROs. Supply voltage V_{DD} is 10V. (c) Variation of oscillation frequency with width ratio W_{down}/W_{up}. The shadow indicates that the workable region is from 4 to 190.

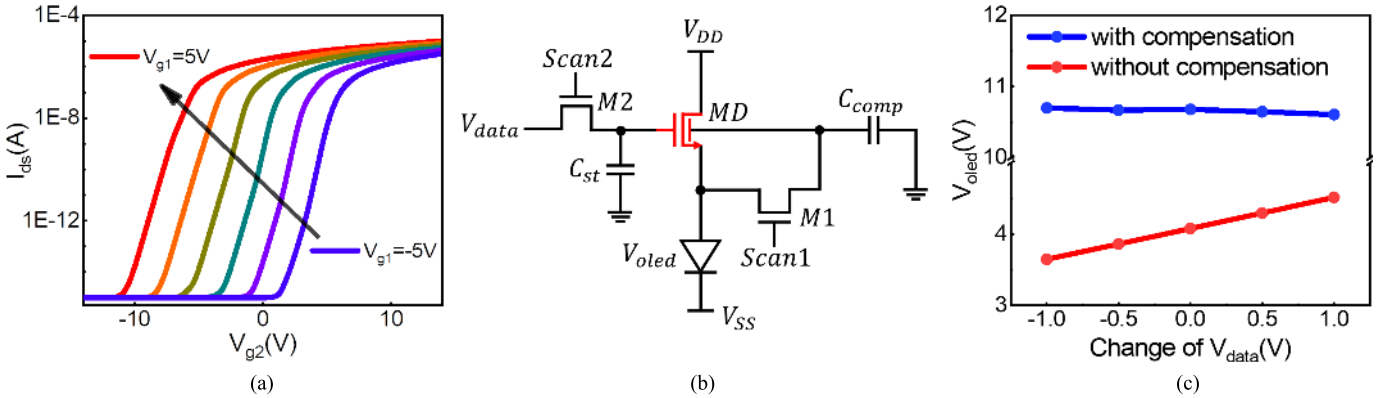

Fig. 8. (a) Curves of drain current versus BG voltage for the IDG a-IGZO TFT at different TG voltages. (b) Three-transistor AMOLED pixel circuit with threshold voltage compensation function using IDG a-IGZO TFT compact model. (c) V_{oled} variation at different V_{data} sets for the circuits with and without compensation [22].

a compact model, our model needs to satisfy the Gummel symmetry test. We have provided the results of this benchmark test in Fig. 6, showing that the first-, second-, and third-order derivatives of I_{ds} with various gate voltages display excellent continuity and symmetry characteristics of our model.

IV. Circuit Simulation Results and Discussion

To verify the model's usability in EDA design tools, the model is written in Verilog-A and compiled to include the IDG a-IGZO TFTs as new active components of the circuit simulator. The two most obvious advantages of IDG a-IGZO TFTs over single gate (SG) are the enhancement of on/off-current ratio and controllability of turn-on voltage. For the assistance of analyzing device physics and guiding fabrication, we have carried on the simulation analysis to these two characteristics.

DG-driving achieves bulk-accumulation, giving advantages such as high driving current and small SS. Fig. 7(a) shows the transfer characteristics under three different gate bias sweep conditions: DG (driving simultaneously the TG and BG), TG (sweeping the TG, while grounding the BG), and BG (sweeping the BG, while grounding the TG). The driving current is greatly improved in DG transistors, even better than the sum of TG and BG. This is because of the coupling effect between the two gates, the conductive channels are no longer limited to the top and bottom surfaces, but extend to the body of the active layer, carriers are less affected by the interface states, and the field effect mobility increases significantly. In addition, the SS of DG devices is smaller than TG and BG, which is mainly due to the enhanced control ability of the double gates to the carriers in the channels. Ring oscillator (RO) as a basic cell in circuit design is simulated to check the circuit-level accuracy of our proposed model. Typical output waveforms of SG- and DG-driven ROs are shown in Fig. 7(b) for $V_{DD} = 10\ V$. Consistent with experimental results, the simulation results demonstrate that DG-driving increases the switching speed by about two times, for the same device size and driving voltage. Moreover, DG-driving has higher crossing current compared with SG-driving, indicating an enhanced driving capability in charging and discharging the load capacitors. The model can also be used to predict the variation of frequency with the size of the device (e.g. channel width ratio) for the optimization analysis. Fig. 7(c) indicates that the circuit workable range is from 4 to 190.

The parallel shifting characteristic of drain current versus BG voltage at different TG voltages is shown in Fig. 8(a). The threshold voltage of IDG TFT using the BG in its normal operation can be controlled artificially by the TG voltage. The reason is the attraction and expelling of free carriers in the

active layer by the TG. Therefore, the problem of the threshold voltage shift can be get rid of by appropriately setting the voltage on the TG. Based on this phenomenon, a simple circuit of active-matrix OLED, as shown in Fig. 8(b), using the TG to compensate threshold voltage variation is implemented by our model [22]. Fig. 8(c) compares the pixel circuit results with and without threshold voltage compensation. The output voltage converges to almost the same value with the compensation, while has an obvious shift in the latter case, which verifies the capability of the model to compensate the threshold voltage in the circuit.

V. Conclusion

In this article, a new surface potential-based physical compact model for IDG a-IGZO TFTs is established with continuous analytical solution and extensively verified by device measurements. As several transport mechanisms are considered, the model can predict temperature and gate voltages-dependent characteristics. To prove the compact model in an optimization of the logic circuit design, the ROs and pixel circuit are successfully simulated. Most importantly, a circuit with threshold voltage compensation function using IDG a-IGZO TFTs can be obtained, which is instructive to IGZO-based circuit design and performance prediction.

References

[1] K. Hoshino, D. Hong, H. Q. Chiang, and J. F. Wager, "Constant-voltage-bias stress testing of a-IGZO thin-film transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 7, pp. 1365–1370, Jul. 2009.

[2] M. Kim *et al.*, "High mobility bottom gate InGaZnO thin film transistors with SiO_x etch stopper," *Appl. Phys. Lett.*, vol. 90, no. 21, May 2007, Art. no. 212114.

[3] Y. W. Jeon *et al.*, "Subgap density-of-states-based amorphous oxide thin film transistor simulator (DeAOTS)," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 2988–3000, Nov. 2010.

[4] S. Hong, S. Lee, M. Mativenga, and J. Jang, "Reduction of negative bias and light instability of a-IGZO TFTs by dual-gate driving," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 93–95, Jan. 2014.

[5] Y. Chen, D. Geng, M. Mativenga, H. Nam, and J. Jang, "High-speed pseudo-CMOS circuits using bulk accumulation a-IGZO TFTs," *IEEE Electron Device Lett.*, vol. 36, no. 2, pp. 153–155, Feb. 2015.

[6] X. Li, D. Geng, M. Mativenga, and J. Jang, "High-speed dual-gate a-IGZO TFT-based circuits with top-gate offset structure," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 461–463, Apr. 2014.

[7] Z. Zong, "A new surface potential-based compact model for a-IGZO TFTs in RFID applications," in *IEDM Tech. Dig.*, Dec. 2014, pp. 35-1–35-5.

[8] Z. Zong, L. Li, J. Jang, N. Lu, and M. Liu, "Analytical surface-potential compact model for amorphous-IGZO thin-film transistors," *J. Appl. Phys.*, vol. 117, no. 21, Jun. 2015, Art. no. 215705.

[9] L. Li, N. Lu, and M. Liu, "Field effect mobility model in oxide semiconductor thin film transistors with arbitrary energy distribution of traps," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 226–228, Feb. 2014.

[10] M. C. J. M. Vissenberg and M. Matters, "Theory of the field-effect mobility in amorphous organic transistors," *Phys. Rev. B, Condens. Matter*, vol. 57, no. 20, p. 12964, Jan. 1998.

[11] A. V. Nenashev, J. O. Oelerich, S. H. M. Greiner, A. V. Dvurechenskii, F. Gebhard, and S. D. Baranovskii, "Percolation description of charge transport in amorphous oxide semiconductors," *Phys. Rev. B, Condens. Matter*, vol. 100, no. 12, Sep. 2019, Art. no. 125202.

[12] D. Venkateshvaran *et al.*, "Approaching disorder-free transport in high-mobility conjugated polymers," *Nature*, vol. 515, no. 7527, pp. 384–388, Nov. 2014.

[13] T. Kamiya, K. Nomura, and H. Hosono, "Origin of definite Hall voltage and positive slope in mobility-donor density relation in disordered oxide semiconductors," *Appl. Phys. Lett.*, vol. 96, no. 12, Mar. 2010, Art. no. 122103.

[14] T. Poiroux *et al.*, "Leti-UTSOI2.1: A compact model for UTBB-FDSOI technologies—Part I: Interface potentials analytical model," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2751–2759, Sep. 2015.

[15] A. Ortiz-Conde, F. G. Sanchez, S. Malobabic, J. Muci, and R. Salazar, "Drain current and transconductance model for the undoped body asymmetric double-gate MOSFET," in *Proc. 8th Int. Conf. Solid-State Integr. Circuit Technol.*, Oct. 2006, pp. 1239–1242.

[16] A. Ortiz-Conde and F. J. García-Sánchez, "Generic complex-variable potential equation for the undoped asymmetric independent double-gate MOSFET," *Solid-State Electron.*, vol. 57, no. 1, pp. 43–51, Mar. 2011.

[17] M. Reyboz, P. Martin, T. Poiroux, and O. Rozeau, "Continuous model for independent double gate MOSFET," *Solid-State Electron.*, vol. 53, no. 5, pp. 504–513, May 2009.

[18] S. Lee *et al.*, "Temperature dependent electron transport in amorphous oxide semiconductor thin film transistors," in *IEDM Tech. Dig.*, Dec. 2011, pp. 14-1–14-6.

[19] P. Dutta, B. Syamal, N. Mohankumar, and C. K. Sarkar, "A surface potential based drain current model for asymmetric double gate MOSFETs," *Solid-State Electron.*, vol. 56, no. 1, pp. 148–154, Feb. 2011.

[20] X. Zhou and K. Y. Lim, "Unified MOSFET compact I-V model formulation through physics-based effective transformation," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 887–896, May 2001.

[21] S. Lee, S. Jeon, and A. Nathan, "Modeling sub-threshold current–voltage characteristics in thin film transistors," *J. Display Technol.*, vol. 9, no. 11, pp. 883–889, Nov. 2013.

[22] Y.-H. Tai, L.-S. Chou, H.-L. Chiu, and B.-C. Chen, "Three-transistor AMOLED pixel circuit with threshold voltage compensation function using dual-gate IGZO TFT," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 393–395, Mar. 2012.