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Analytical Switching Cycle Modeling of Bidirectional High Voltage Flyback Converter for Capacitive Load Considering Core Loss Effect

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Abstract — **With the advancement of material science, various smart materials with intrinsic capacitive property are emerging. The high voltage (HV) power electronics converters with bidirectional energy flow functionality for supplying the capacitive load are highly demanded. A switching cycle based analytical model of HV bidirectional converter driving capacitive load is beneficial in thoroughly understanding the operational behavior, investigating the energy efficiency and optimizing the design. In this paper, a HV bidirectional flyback converter for capacitive load is generally discussed in terms of configuration and working principle. Considering the parasitic elements as well as the core loss effect, the converter is modeled with analytical formulas for one switching cycle. The comparison between the model based calculation results and prototype experiments based measurement results are used to validate the analytical model.**

Index Terms – **Analytical modeling, switching cycle, high voltage, bidirectional, flyback, capacitive load.**

I. INTRODUCTION

Power electronics technology focuses on processing power in order to supply the load as required with minimum cost in terms of power loss (high efficiency), volume (high power density) and price (low cost) [1]-[3]. Since the equipment or devices with resistive or resistive-inductive characteristic have been intensively used, such as the electrical heater, motor and lighting appliance, most research in this field pays attention to the resistive or resistive-inductive load. In the past decades, with the rapid development of material science, a variety of smart material with intrinsic capacitive property is constantly emerging. Due to their advantages, such as light weight, compact size, nonmagnetic and the ability to directly generate mechanical motion under external voltage, they tend to become desired candidate in various actuation systems to replace the conventional hydraulic, pneumatic or electromagnetic actuator. Taking the modern heating system as an example, the smart material based actuator can be used to replace the conventional counterparts inside the thermostat in order to save energy or provide noise free operation. In addition, the conceptual ultra-flat loudspeaker is possible to be formed by the light and flexible smart material. Furthermore, the actuation system involved in the modern bionic robot can easily be achieved through the smart material technology. In order to supply the capacitive actuators as required, a considerable effort needs to be dedicated to develop the applicable power electronics converters with competitive efficiency, size as well as cost.

Piezoelectric and dielectric electro active polymer (DEAP) materials are two types of smart material with highly capacitive characteristic [4] [5]. They share a similar structure – an insulating layer sandwiched between two compliant conducting electrodes. The ceramic material forms dielectric layer in the piezoelectric case and the soft silicone polymer is employed for DEAP material. Once an electric field is applied to the capacitive materials, the deformation of the insulation layer will be induced due to the inverse piezoelectric effect or electrostatic force. This intrinsic property enables the actuators composed of capacitive materials. One common challenge in driving capacitive actuators is the relatively high stimulating voltage: thanks to the employment of multilayer structure in piezoelectric actuator, this voltage can be reduced to the range of hundred volts; however in DEAP case, the voltage still needs to be in the vicinity of several kilovolts in order to fully elongate the actuator. Normally, this high voltage (HV) cannot be directly available, especially in the autonomous circumstance, which actually will be the most case for the system consisting of capacitive actuator. Thus, a converter with the features of low input voltage and high output voltage needs to be investigated. Besides, to avoid the waste of electrical energy stored in the capacitive actuator, the energy (charge) recovery technique needs to be employed in order to recycle the energy to the power source when the actuator needs to be released [6]. Hence, a converter which can deal with the bidirectional energy flow tends to be a desired candidate in this case.

As a simple and easily implemented configuration with galvanic isolation functionality, flyback topology has been widely used in power electronics industry, such as the laptop and mobile phone charger, standby power supplies, etc. [7]

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[8]. Recently, due to the energy crisis, researchers in power electronics community concentrate more on investigating the flyback based inverters for renewable energy applications [9]-[15]. Besides, the investigation regarding the flyback has also been intensively carried out in the field of light-emitting diode (LED) driver [16]-[22]. As a mature technology, flyback is well suited for the high output voltage applications since no extra inductor is needed in the HV side and it had already been successfully applied in the color TVs to generate HV [23]-[25]. Flyback topology can easily achieve the bidirectional energy flow by replacing the rectifier diode with an active semiconductor device in the secondary side [26] [27]. The emerging of smart materials will encourage the research into the HV bidirectional energy conversion for capacitive load in the coming years. Preliminary research has been conducted to design and implement the bidirectional HV flyback converter for capacitive actuators [28]-[30]. As a critical part in flyback configuration, the transformer (coupled inductors) considerably affects the operational behavior due to the parasitic elements, especially in the HV condition [7] [31]-[34]. Compared to the converter feeding the resistive load, the capacitive property of the actuators will introduce different operating behavior for the energy conversion. The effect of core loss needs to be taken into account in this capacitive load case, if an accurate model is set to be the ultimate goal. Hence, the operational behavior is worthy to be investigated in the bidirectional energy flow for HV converter with capacitive load in order to thoroughly understand the working principle, which will be beneficial for analyzing the efficiency, providing the design guideline as well as optimizing the design.

This paper will focus on the analytical behavioral modeling of bidirectional HV flyback converter for capacitive load in each switching cycle with the consideration of core loss effect. In Section II, the bidirectional HV flyback converter for capacitive load is described in terms of configuration and fundamental operation principle. The general discussion, definition and consideration utilized to perform the analytical modeling as well as the detailed analytical switching cycle modeling are presented in Section III. In Section IV, the analyzed model is verified through the comparison between the calculated results and the experimental ones for both charging and discharging mode. The efficiency comparison is applied to verify the importance of considering the core loss. A conclusion is drawn in Section V.

II. Description of Bidirectional HV Flyback Converter for Capacitive Load

A. Topology and configuration

The proposed bidirectional HV flyback converter for capacitive load is depicted in Fig. 1. Due to the poor performance of body diode inside the HV MOSFET (S_2), two extra HV diodes (D_{21} and D_{22}) are employed to block the current through the body diode and to form the freewheeling path for the secondary side current, respectively. The current sensing resistors (RP_1, RP_2 and RP_3) are applied in order to realize the current loop control. As aforementioned, the

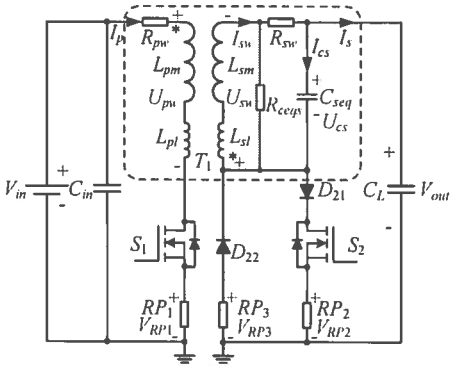


Fig. 1. The configuration of bidirectional HV flyback converter for capacitive load.

parasitic components in flyback transformer will introduce significant influence to the operation of the converter, especially in the HV condition, and must be considered in the analytical modeling. The most critical parasitic element in the HV transformer is the secondary winding stray capacitance caused by a large number of winding turns [31] [32]. Combined with other parasitic capacitances in the HV side, such as the junction capacitance of HV diodes and the output capacitance of the HV MOSFET, an equivalent stray capacitance C_{seq} paralleled to secondary winding of transformer is utilized to represent the effect of parasitic capacitances. In addition, the leakage inductance (L_{pl} and L_{sl}) has always been focused on by the researchers who want to improve the efficiency [7]. It should be noted that the primary side leakage inductance (L_{pl}) and secondary side leakage inductance (L_{sl}) cannot exist simultaneously. When the energy flow is from primary side to secondary side, L_{pl} is adopted to stand for the untransferrable energy stored in the flyback transformer. The same concept applies to L_{sl}. Furthermore, in order to establish the precise analytical model, the winding resistances (R_{pw} and R_{sw}) cannot be neglected [33] [34]. All the essential parasitic elements are shown in Fig. 1 as well. For precisely analyzing the behavior of the converter supplying the capacitive load, the impact of the core loss must be considered as in the conventional converter for resistive load. Resistive element is proved to be an effective means to represent the core loss. An equivalent resistance of core loss reflected to the secondary side (R_{ceqs}), therefore, is employed to stand for the influence of the core loss in each switching cycle.

B. General operation principle

Unlike the conventional DC-DC converter, the bidirectional HV converter designed for capacitive load normally does not operate in the steady state. The common operating states consist of the charging mode (the output voltage increases) - energy transfers from source to the capacitive load, and discharging mode (the output voltage decreases) - energy recycles from capacitive load to power source. The entire charging process from zero till the pre-set maximum output voltage is just like the startup process in the conventional converter and consists of a large number of successive switching charging cycles. Similarly, the overall

discharging process is comprised of a lot of successive switching cycles to discharge the capacitive load from maximum voltage to zero. The variation of output voltage in the normal operation is shown in Fig. 2 with the identification of entire charging and discharging process as well as switching cycles in charging and discharging mode. In order to achieve the complete energy transfer in each switching cycle, the current involved in the flyback transformer can be controlled to operate in the Boundary Conduction Mode (BCM) or Discontinuous Conduction Mode (DCM).

III. Analytical Modeling

A. General discussion and definitions

As the typical and long-term operation status in conventional DC-DC converter, the steady state has been traditionally researched in terms of modeling and detailed analysis. Correspondingly, the charging and discharging modes, as the normal operating states, in the converter with capacitive load are necessary to be thoroughly investigated. Referring to Fig. 2, the charging process contains a series of switching cycles and the behavior in one switching cycle differs from that in another one due to the variable initial output voltage. In spite of this, all the switching cycles share the same fundamental analytical model. Hence, the investigation of charging mode can be focused on just one single charging cycle. The same concept can also be applied to the discharging mode. In this paper, the charging mode will be analyzed in BCM which is beneficial in achieving a fast charging process, while the discharge mode will be modeled in DCM which can easily be implemented. Due to the employment of two control ICs, the BCM for charging process and DCM for the discharging cycles can easily be achieved.

In the circuit shown in Fig. 1, as aforementioned, L_{pm} and L_{sm} are primary and secondary magnetizing inductances, respectively. L_{pl} and L_{sl} are primary and secondary leakage inductances, respectively. And $L_p = L_{pm} + L_{pl}$ as well as $L_s = L_{sm} + L_{sl}$ is utilized to stand for the primary and secondary total inductance. RP_1, RP_2 and RP_3 are the resistances of three current sensing resistors. The secondary side equivalent parasitic capacitance paralleled to transformer winding is denoted as C_{seq}. V_{D21} and V_{D22} are the forward voltage drop of high voltage diodes D_{21} and D_{22}, respectively. In fact, the voltage drop changes with the forward current. To reduce the complexity, the constant forward voltage drop is assumed here. In the discharging mode, the body diode of primary switch (S_1) plays the role of freewheeling and its forward voltage drop is denoted as V_{bdS1}. In order to improve the accuracy of the model, the on resistances of MOSFETs (S_1 and S_2) need to be taken into account, especially that for the HV MOSFET due to its large value. On the other hand, to simplify the analytical model, the on resistances are considered to be a fixed value and denoted as R_{dsonS1} and R_{dsonS2}, respectively. Winding resistances (R_{pw} and R_{sw}) are frequency related parameters and do not have the fixed values, which will be defined in the analytical modeling later. C_L is utilized to stand for the capacitance of the capacitive load. V_{in} is the input voltage source with fixed value, V_o is the output voltage and the initial output voltage for the current switching cycle is denoted as V_{oini}. U_{cs} is used to stand for the voltage over the equivalent parasitic capacitance C_{seq}. Considering the measuring of the current in reality, it is reasonable to use the voltages over the current sensing resistors V_{RP1} V_{RP2} and V_{RP3} to represent the currents in the circuit. The voltages over transformer windings are denoted as U_{pw} and U_{sw}, respectively. And the positive directions for all the voltages are illustrated in Fig. 1. The primary current I_p and secondary current I_s are also depicted in Fig. 1 with their positive directions. The current through C_{seq} is denoted as I_{cs} with the corresponding positive direction to the voltage. Due to the impact of C_{seq} and the equivalent resistance of core loss, the secondary current I_s cannot stand for the secondary side winding current, which is then denoted as I_{sw} with the positive direction shown in Fig. 1.

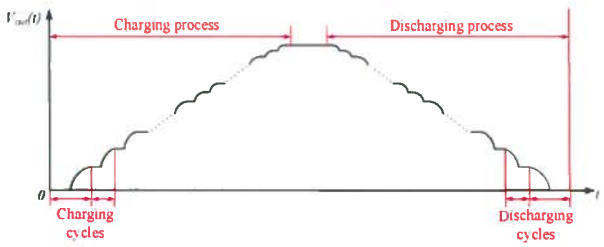


Fig. 2. The output voltage variation in the normal operation

B. Discussion of core loss and its equivalent resistance R_{ceqs}

It is reasonable to discuss the converter with capacitive load from the energy point of view, since there is no real output power for this type of converter. For charging mode, in a certain switching cycle, the input energy from power source can be assumed to be fixed if the corresponding current control mode is employed, thus, the energy increase over the capacitive load will depend on the energy losses for all the components in the converter. Therefore, in order to accurately predict the voltage variation of the load during this switching period, all the losses need to be taken into account, including the core loss. In terms of energy flow, the discharging mode can be considered to be the reverse process of charging mode. To establish the precise model, the core loss effect cannot be neglected as well.

The most commonly used method to calculate core loss is the Steinmetz equation. It should be noted that this equation is only valid for sinusoidal waveforms and cannot be directly applied in most power electronics systems [35] [36]. In order to overcome this limitation, several methodologies have been proposed. Among them, the widely adopted approach is the improved generalized Steinmetz equation (iGSE) [35] [36].

$$P_v = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{1}$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\theta|^{\alpha}2^{\beta-\alpha}d\theta} \tag{2}$$

where P_v is the time-average power loss per unit volume, T stands for the switching period, $\left|\frac{dB}{dt}\right|$ is the absolute value of

change rate of flux density, ΔB is the peak-to-peak flux density and α, β, k are material related parameters, which can be obtained or derived from the datasheet of the material.

As previously stated, resistive element can be utilized to represent the effect of core loss. If the analytical model in one switching cycle is known, the core loss can be calculated through (1), thus the secondary side equivalent resistance of core loss R_{ceqs} can be derived through (3) and the detailed behavior can be predicted [37].

$$R_{ceqs} = \frac{U_{sw}^2}{P_v} \tag{3}$$

However, the contradiction is that without knowing the equivalent resistance of core loss, the accurate analytical model cannot be obtained in advance. One feasible approach is proposed: 1) build the accurate behavior model in one switching cycle considering the impact of R_{ceqs}; 2) set R_{ceqs} to infinity in order to avoid the consideration of the core loss to achieve the estimated behavior model in one switching cycle; 3) based on the estimated model, through (1) and (3), the equivalent resistance of core loss can be obtained; 4) apply the acquired R_{ceqs} to the accurate model to achieve the precise behavior in one switching cycle. Hence, in the following derivation process, including the charging mode as well as the discharging mode, this methodology will be applied in order to acquire the accurate analytical behavior model in one switching cycle.

C. Analytical behavior modeling of charging mode

In charging mode, due to the employment of BCM, one switching cycle consists of 4 stages. In Fig. 3 (a)-(d), considering the equivalent resistance of core loss, the equivalent circuits of different operation stages with the practical current flow direction are depicted respectively. And the key waveforms concerning the operation stages, including the waveforms for low and high output voltages in the charging process, are shown in Fig. 4.

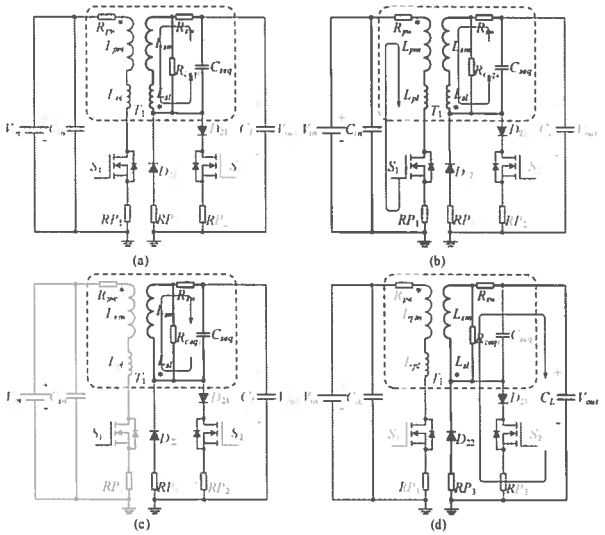


Fig. 3. Equivalent circuit schemes of different operation stages. (a) $t_0 < t < t_1$ (b) $t_1 < t < t_2$ (c) $t_2 < t < t_3$ (d) $t_3 < t < t_4 = t_0$.

Stage 1 [$t_0 < t < t_1$: Fig. 3 (a)]: In this stage, the secondary side equivalent stray capacitor C_{seq} resonates with secondary inductance L_s with the initial energy stored in the capacitor. At the beginning of this stage, the voltage over C_{seq} is

$$U_{csc01t0} = V_{oini} + V_{D22} \tag{4}$$

The subscript *c01* stands for the stage [t_0 t_1] in the charging mode and *t0* represents the time t_0. This rule for subscript will be applied throughout this paper. Due to the resonance in this stage, the voltage over C_{seq} and the secondary winding current I_{sw} can be derived as

$$U_{cs01}(t) = e^{-\frac{L_s+R_{swc01}\cdot C_{seq}\cdot R_{ceqs}}{2\cdot L_s\cdot C_{seq}\cdot(R_{swc01}+R_{ceqs})}\cdot(t-t_0)} \cdot \left\{U_{csc01t0} \cdot \cos[\omega_{c01}\cdot(t-t_0)] + \frac{R_{ceqs}\cdot C_{seq}\cdot R_{swc01}\cdot U_{csc01t0} - L_s\cdot U_{csc01t0}}{AP_{c01}} \cdot \sin[\omega_{c01}\cdot(t-t_0)]\right\} \tag{5}$$

$$I_{swc01}(t) = -\frac{2\cdot R_{ceqs}\cdot C_{seq}\cdot U_{csc01t0}}{AP_{c01}} \cdot e^{-\frac{L_s+R_{swc01}\cdot C_{seq}\cdot R_{ceqs}}{2\cdot L_s\cdot C_{seq}\cdot(R_{swc01}+R_{ceqs})}\cdot(t-t_0)} \cdot \sin[\omega_{c01}\cdot(t-t_0)] \tag{6}$$

Then secondary winding voltage can be written as

$$U_{swc01}(t) = L_s \cdot \frac{dI_{swc01}(t)}{dt} \tag{7}$$

In these equations, R_{swc01} is the secondary winding resistance at the resonance frequency in this stage:

$$R_{swc01} = R_{sw}@\frac{1}{2\pi\cdot\sqrt{L_s\cdot C_{seq}}} \tag{8}$$

In addition,

$$AP_{c01} = \sqrt{\begin{matrix}4\cdot L_s\cdot C_{seq}\cdot {R_{ceqs}}^2 \\ +2\cdot L_s\cdot C_{seq}\cdot R_{swc01}\cdot R_{ceqs} \\ -{L_s}^2 - {R_{swc01}}^2\cdot {C_{seq}}^2\cdot {R_{ceqs}}^2\end{matrix}} \tag{9}$$

$$\omega_{c01} = \frac{AP_{c01}}{2\cdot L_s\cdot C_{seq}\cdot(R_{swc01}+R_{ceqs})} \tag{10}$$

are valid.

In low voltage operation, the quasi-resonant characteristic can be achieved if the proper parameters are selected in the control circuits. Then, the end time for this stage can be calculated as

$$t_1 = t_0 + \frac{\pi}{\omega_{c01}} \tag{11}$$

However, this is not the case for other operation voltages. With the increase of the output voltage, the secondary winding voltage $U_{swc01}(t)$ tends to be capable of reaching the threshold voltage, defined as

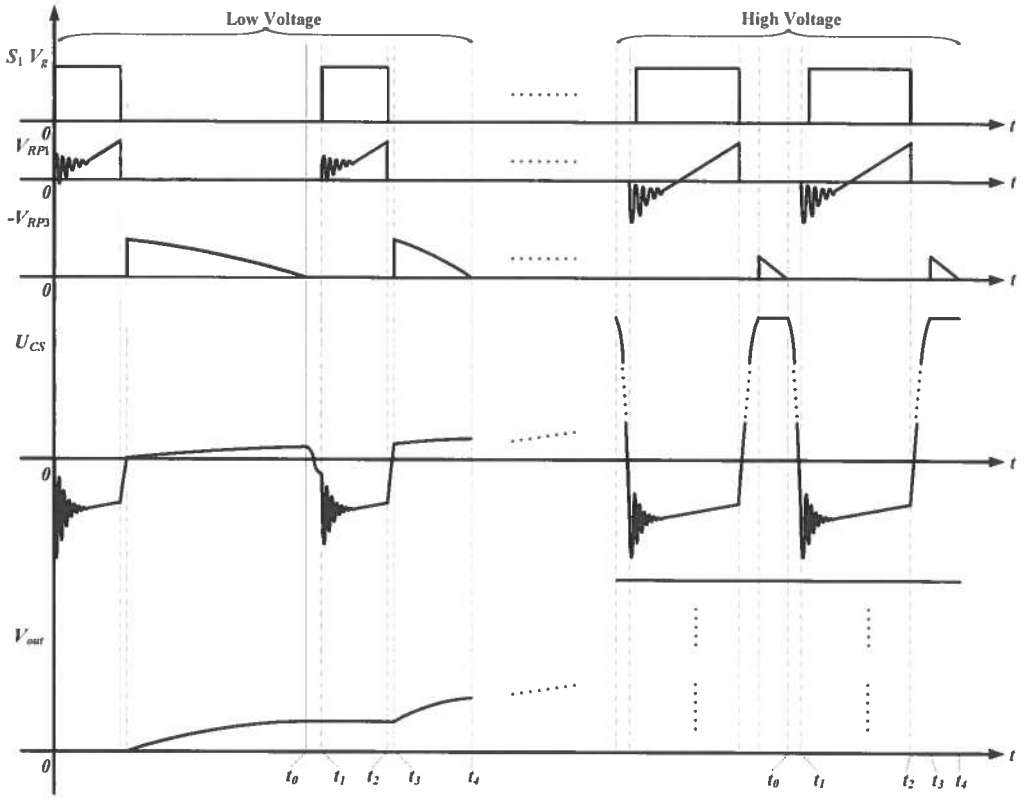


Fig. 4. Key waveforms of the operation stages under different output voltage levels

$$U_{th} = N \cdot (V_{in} + V_{bdS1}) \tag{12}$$

where N is the turns ratio of the transformer and defined as the secondary winding turns N_{sec} divided by primary winding turns N_{pri}. Once the threshold voltage is reached, the body diode of S_1 is forced to conduct. Hence, a minus voltage over RP_1, which represents the minus primary current, can be observed, as the V_{RP1} waveforms under high voltage in Fig. 4. After an extremely short while (also depending on the parameters in the control circuits), S_1 will be turned on and the minus current will switch to pass through S_1 instead of its body diode due to its low on-resistance. In order to simplify the analysis, it can be assumed that S_1 is turned on at exactly the time the body diode of S_1 is forced to conduct. Therefore, the end time t_1 can be obtained through numerically solving the following equation

$$U_{swc01}(t_1) = U_{th} \tag{13}$$

In fact, it can be summarized that if (13) does not have the real solution, then the converter is working at the low voltage operation; otherwise it is defined to be under non low voltage operations.

Stage 2 [$t_1 < t < t_2$: Fig. 3 (b)]: S_1 is switched on at the beginning of this stage. The dominant behavior in this stage is the primary magnetization. In addition, the resonance due to the primary leakage inductance and C_{seq} in the low voltage operation and the secondary leakage inductance and C_{seq} in other operating voltages cannot be neglected [31]. In fact, the core loss equivalent resistance is desired to be considered from the primary side in this phase, and from (1) and (3) it is easy to derive the relationship between the primary core loss equivalent resistance R_{ceqp} and its secondary side counterpart R_{ceqs}

$$R_{ceqp} = \frac{R_{ceqs}}{N^2} \tag{14}$$

The magnetizing current during this stage can be written

$$I_{pc12mag}(t) = \frac{V_{in}}{R_{pmeqc12}} + \left(I_{pc01t1} - \frac{V_{in}}{R_{pmeqc12}}\right) \cdot e^{-\frac{R_{pmeqc12} \cdot R_{ceqp}}{L_p \cdot (R_{pmeqc12} + R_{ceqp})}(t - t_1)} \tag{15}$$

In this equation, I_{pc01t1} is the initial primary current and can be obtained through

$$I_{pc12magt1} = \begin{cases} 0 & \text{if low voltage operation} \\ N \cdot I_{csc01}(t_1) & \text{if non low voltage operation} \end{cases} \tag{16}$$

and $R_{pmeqc12}$ stands for the primary magnetizing equivalent resistance and can be calculated as

$$R_{pmeqc12} = R_{pwc12} + R_{dsonS1} + RP_1 \tag{17}$$

where R_{pwc12} is the primary winding resistance at the switching frequency for the current cycle. So far, the exact switching frequency is unknown. But an estimated value can be achieved by ignoring the influence of the stages (a) and (c) in Fig. 3 and only considering the ideal situations for the stages (b) and (d) in Fig. 3

$$f_{swideal} = \frac{1}{\frac{(I_{pp}-I_{po1t1})\cdot L_p}{V_{in}} + \tan^{-1}\left(\frac{I_{pp}\cdot\sqrt{L_{sm}}}{N\cdot V_{oini}\cdot\sqrt{CL}}\right)\cdot\sqrt{L_{sm}\cdot CL}} \tag{18}$$

where I_{pp} is the primary peak current set by the inner current loop control. Then,

$$R_{pwc12} \approx R_{pw}@f_{swideal} \tag{19}$$

The primary winding voltage caused by the magnetization is

$$U_{pwc12mag}(t) = (V_{in} - I_{pc01t1}\cdot R_{pmeqc12})\cdot e^{-\frac{R_{pmeqc12}\cdot R_{ceqp}}{L_p\cdot(R_{pmeqc12}+R_{ceqp})}\cdot(t-t_1)} \tag{20}$$

Concerning the resonance part, if the converter is under low voltage operation, the primary winding resonant voltage and primary resonant current can be written

$$U_{pwc12rl}(t) = -\left(\frac{U_{csc01t1}}{N} + V_{in}\right)\cdot e^{-\frac{R_{preqc12}}{2\cdot L_{pl}}\cdot(t-t_1)}\cdot \left\{\cos[\omega_{c12rl}\cdot(t-t_1)] + \frac{C_{preq}\cdot R_{preqc12}}{AP_{c12rl}}\cdot\sin[\omega_{c12rl}\cdot(t-t_1)]\right\} \tag{21}$$

$$I_{pc12rl}(t) = \frac{2\cdot C_{preq}}{AP_{c12rl}}\cdot\left(\frac{U_{csc01t1}}{N} + V_{in}\right)\cdot e^{-\frac{R_{preqc12}}{2\cdot L_{pl}}\cdot(t-t_1)}\cdot \sin[\omega_{c12rl}\cdot(t-t_1)] \tag{22}$$

The parameters and initial conditions involved in the above equations can be obtained through the corresponding equations listed in Table VII of the Appendix.

Likewise, if the converter is working at non low voltage operation, the primary winding resonant voltage and primary resonant current can be derived as

$$U_{pw12rh}(t) = -\frac{2\cdot L_{sl}\cdot I_{csc01t1}}{N\cdot AP_{c12rh}}\cdot e^{-\frac{R_{swc12rh}}{2\cdot L_{sl}}\cdot(t-t_1)}\cdot\sin[\omega_{c12rh}\cdot(t-t_1)] \tag{23}$$

$$I_{pc12rh}(t) = -I_{pc01t1}\cdot e^{-\frac{R_{swc12rh}}{2\cdot L_{sl}}\cdot(t-t_1)}\cdot\left\{\cos[\omega_{c12rh}\cdot(t-t_1)] - \frac{C_{seq}\cdot R_{swc12rh}}{AP_{c12rh}}\cdot\sin[\omega_{c12rh}\cdot(t-t_1)]\right\} \tag{24}$$

Similarly, the parameters and initial conditions used here are summarized in Table VII of the Appendix. Hence, the total primary winding voltage and primary current can be obtained through

$$U_{pwc12}(t) = \begin{cases} U_{pwc12mag}(t) + U_{pwc12rl}(t) & \text{if low voltage operation} \\ U_{pwc12mag}(t) + U_{pwc12rh}(t) & \text{if non low voltage operation} \end{cases} \tag{25}$$

$$I_{pc12}(t) = \begin{cases} I_{pc12mag}(t) + I_{pc12rl}(t) & \text{if low voltage operation} \\ I_{pc12mag}(t) + I_{pc12rh}(t) & \text{if non low voltage operation} \end{cases} \tag{26}$$

Considering no current in the secondary side during this stage, the secondary winding voltage and the voltage over C_{seq} can be calculated through

$$U_{swc12}(t) = -U_{csc12}(t) = N\cdot U_{pwc12}(t) \tag{27}$$

and at the end of this stage

$$I_{pc12}(t_2) = I_{pp} \tag{28}$$

can be written. By numerically solving this equation, the end time t_2 can be acquired.

Stage 3 [$t_2 < t < t_3$; Fig. 3 (c)]: S_1 is switched off at the beginning of this stage. However, the secondary freewheeling diode D_{22} cannot conduct immediately due to the reverse voltage. In this stage, in order to simplify the analysis, the primary side resonance between the leakage inductance and output capacitance of S_1 will not be considered and the dominant behavior tends to be the resonance between secondary magnetizing inductance L_{sm} and stray capacitance C_{seq}. In terms of energy, C_{seq} is charged in this stage from the energy already stored in the transformer until its voltage can force D_{22} to conduct. The voltage over C_{seq} and the secondary winding current can be derived as

$$U_{csc23}(t) = e^{-\frac{L_{sm}+R_{swc23}\cdot C_{seq}\cdot R_{ceqs}}{2\cdot L_{sm}\cdot C_{seq}\cdot(R_{swc23}+R_{ceqs})}\cdot(t-t_2)}\cdot\{U_{csc12t2}\cdot\cos[\omega_{c23}\cdot(t-t_2)] + \frac{2\cdot R_{ceqs}\cdot L_{sm}\cdot I_{swc12t2}+R_{ceqs}\cdot C_{seq}\cdot R_{swc23}\cdot U_{csc12t2}-L_{sm}\cdot U_{csc12t2}}{AP_{c23}}\cdot\sin[\omega_{c23}\cdot(t-t_2)]\} \tag{29}$$

$$I_{swc23}(t) = e^{-\frac{L_{sm}+R_{swc23}\cdot C_{seq}\cdot R_{ceqs}}{2\cdot L_{sm}\cdot C_{seq}\cdot(R_{swc23}+R_{ceqs})}\cdot(t-t_2)}\cdot\{I_{swc12t2}\cdot\cos[\omega_{c23}\cdot(t-t_2)] - \frac{2\cdot R_{ceqs}\cdot C_{seq}\cdot U_{csc12t2}+R_{ceqs}\cdot C_{seq}\cdot R_{swc23}\cdot I_{swc12t2}-L_{sm}\cdot I_{swc12t2}}{AP_{c23}}\cdot\sin[\omega_{c23}\cdot(t-t_2)]\} \tag{30}$$

The parameters and conditions in these equations can refer to Table VII in Appendix. At the end of the stage,

$$U_{csc23}(t_3) = U_{csc23t3} = V_{oini} + V_{D22} \tag{31}$$

then the end time t_3 can be obtained through numerically solving the equation.

Stage 4 [$t_3 < t < t_4$: Fig. 3 (d)]: D_{22} is forced to conduct at the beginning of this stage and the freewheeling phase starts. The energy still stored in the flyback transformer will be transferred to the capacitive load. Normally, compared to the capacitance of the load, the stray capacitance can be neglected. Hence, in the analysis for this stage, C_{seq} is not considered. In this phase, the output voltage V_{out} and secondary winding current I_{sw} can be expressed as

$$V_{outc34}(t) = e^{-\frac{L_{sm}+R_{fwc34}\cdot C_L\cdot R_{ceqs}}{2\cdot L_{sm}\cdot C_L\cdot\left(R_{fwc34}+R_{ceqs}\right)}\cdot(t-t_3)}\cdot\left\{U_{csc23t3}\cdot\cos[\omega_{c34}\cdot(t-t_3)]+\frac{2\cdot R_{ceqs}\cdot L_{sm}\cdot I_{swc23t3}+R_{ceqs}\cdot C_L\cdot R_{fwc34}\cdot U_{csc23t3}-L_{sm}\cdot U_{csc23t3}}{AP_{c34}}\cdot\sin[\omega_{c34}\cdot(t-t_3)]\right\}-V_{D22} \quad (32)$$

$$I_{swc34}(t) = e^{-\frac{L_{sm}+R_{fwc34}\cdot C_L\cdot R_{ceqs}}{2\cdot L_{sm}\cdot C_L\cdot\left(R_{fwc34}+R_{ceqs}\right)}\cdot(t-t_3)}\cdot\left\{I_{swc23t3}\cdot\cos[\omega_{c34}\cdot(t-t_3)]-\frac{2\cdot R_{ceqs}\cdot C_L\cdot U_{csc23t3}+R_{ceqs}\cdot C_L\cdot R_{fwc34}\cdot I_{swc23t3}-L_{sm}\cdot I_{swc23t3}}{AP_{c34}}\cdot\sin[\omega_{c34}\cdot(t-t_3)]\right\} \quad (33)$$

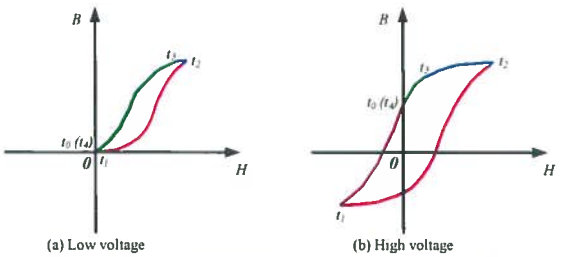
And secondary current I_s can be acquired by

$$I_{sc34}(t) = C_L\cdot\frac{dV_{outc34}(t)}{dt} \quad (34)$$

The parameters and conditions used here can refer to Table VII in Appendix. At the end of this stage, the freewheeling current will reach 0. Hence, the end time of this interval t_4 can be achieved by numerically solving the following equation

$$I_{sc34}(t_4) = 0 \quad (35)$$

So far, the accurate analytical model for one switching cycle during the charging process has been built. However, the unknown parameter – equivalent resistance of core loss R_{ceqs}, prevents the application of the model. As previously stated, an estimated model can be established by setting the R_{ceqs} to infinity in the related equations listed above in order to ignore the influence of the core loss. In this estimated model, the secondary winding voltages and time intervals for each stage can be obtained and utilized to calculate the equivalent resistance of core loss R_{ceqs}.



(a) Low voltage (b) High voltage

Fig. 5. *B-H* curves under different output voltage levels.

Referring to (1), the averaged core power loss is determined by $\left|\frac{dB}{dt}\right|$ as well as ΔB. And $\left|\frac{dB}{dt}\right|$ can be obtained through

$$\left|\frac{dB}{dt}\right| = \left|\frac{U_{sw}}{N_{sec}\cdot A}\right| \quad (36)$$

where N_{sec} is the number of turns for the transformer secondary winding and A stands for the cross-sectional area of magnetic core. As previously defined, U_{sw} is winding voltage of transformer secondary side. Neglecting the influence of winding resistances, then through the current waveforms (V_{RP1} and $-V_{RP3}$) and the voltage waveform (U_{cs}) shown in Fig. 4, the rough *B-H* curves for low and high output voltages with the identification of operation stages can be obtained, depicted in Fig. 5. It can be observed that the peak-to-peak flux density ΔB is, in fact, the flux density change in the stage [t_1-t_2]. Hence, it can be calculated with

$$\Delta B = \int_{t_1}^{t_2}\frac{U_{swc12}(t)}{N_{sec}\cdot A}dt \quad (37)$$

as previously illustrated, U_{swc12} is the secondary winding voltage corresponding to stage [t_1-t_2] in the charging mode.

In addition, the switching period T affects the determination of core loss as well. However, if energy instead of power is chosen to be the standpoint and considering the 4 stages in one charging cycle, the core energy loss per cycle can be expressed as

$$E_v = V_e\cdot\frac{k_i\cdot\Delta B^{\beta-\alpha}}{|N_{sec}\cdot A|^{\alpha}}\cdot\sum_{m=0,1,2,3}\int_{t_m}^{t_{m+1}}\left|U_{swcm,m+1}(t)\right|^{\alpha}dt \quad (38)$$

where $U_{swcm,m+1}(t)$ $(m=0,1,2,3)$ (i.e. $U_{swc01}(t)$, $U_{swc12}(t)$, $U_{swc23}(t)$ and $U_{swc34}(t)$) are the voltages over secondary winding for 4 stages in the charging mode and V_e stands for the volume of the magnetic core. Referring to the general definition of equivalent resistance in terms of power, from secondary side, the core loss equivalent resistance can be derived as

$$R_{ceqs} = \frac{\sum_{m=0,1,2,3}\int_{t_m}^{t_{m+1}}U_{swcm,m+1}^2dt}{E_v} \quad (39)$$

After applying the achieved equivalent resistance of core loss R_{ceqs} to the established accurate analytical model, the detailed behavior of one switching cycle during the charging process can be acquired.

D. Analytical behavior modeling of discharging mode

As previously stated, the discharging mode is going to be analyzed with DCM working in the fixed operation frequency (denoted as f_{fsd}) and one switching cycle will consist of 5 stages. Similar to the analysis in charging mode, the equivalent circuits for each operation stage are depicted in Fig. 6 (a)-(e) respectively. And the key waveforms for the operation stages, including the waveforms for high as well as low output voltages in the discharging process, are provided in Fig. 7.

Similar to the situation in charging mode, the accurate analytical behavior model needs to be established first, which is presented below.

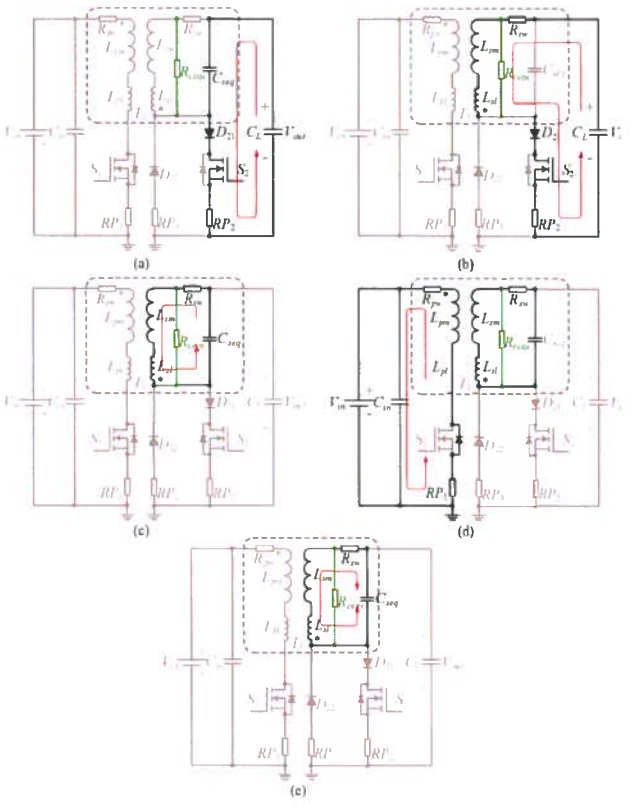


Fig. 6. Equivalent circuit schemes of different operation stages. (a) $t_0 < t < t_1$ (b) $t_1 < t < t_2$ (c) $t_2 < t < t_3$ (d) $t_3 < t < t_4$ (e) $t_4 < t < t_5 = t_0$.

Stage 1 [$t_0 < t < t_1$: Fig. 6 (a)]: At the beginning of this stage, S_2 is switched on and the secondary side equivalent stray capacitor C_{seq} starts to be charged. Normally, the load capacitance is more than thousand times larger than the capacitance of C_{seq}, so in this stage, the capacitive load can be assumed to be a constant voltage source. It should be noted that the equivalent resistance of core loss R_{ceqs} does not contribute in this period, since only the parasitic capacitor is charged and the core has not been magnetized yet. Thus, in this interval, the voltage over and the current through C_{seq} can be written as

$$U_{csd01}(t) = (V_{oini} - V_{D21}) + (U_{csd01t0} - (V_{oini} - V_{D21})) \cdot e^{-\frac{t-t_0}{T_{ccd01}}} \quad (40)$$

$$I_{csd01}(t) = \frac{V_{oini}-V_{D21}-U_{csd01t0}}{R_{ccd01}} \cdot e^{-\frac{t-t_0}{T_{ccd01}}} \quad (41)$$

In these equations,

$$R_{ccd01} = R_{dsonS2} + RP_2 \quad (42)$$

$$T_{ccd01} = R_{ccd01} \cdot C_{seq} \quad (43)$$

As previously mentioned, the subscript *d01* represents the stage [t_0 t_1] in the discharging mode and *t0* stands for the time t_0. In the entire discharging process, the initial condition of U_{cs} (i.e. $U_{csd01t0}$) for each switching cycle can be obtained through the end condition of last cycle. However, if only one independent switching cycle is investigated, the worst case in terms of charging current (i.e. $I_{csd01}(t)$) needs to be considered, which means the minimum value of $U_{csd01t0}$ needs to be applied in this stage. Considering the stage [t_4-t_5] of last switching cycle and ignoring the damping effect of the winding resistance, in the high voltage operation, U_{cs} can fluctuate between $-N\cdot(V_{in}+V_{bdS1})$ and $N\cdot(V_{in}+V_{bdS1})$. But this is not the case for low voltage operation, due to the voltage clamp caused by the final output voltage of previous cycle (i.e. the initial output voltage for the current cycle) and V_{D22}, the fluctuation range for U_{cs} is $[-(V_{oini}+V_{D22})\ (V_{oini}+V_{D22})]$. Thus, the initial condition for U_{cs} can be written as

$$U_{csd01t0} = \begin{cases} -(V_{oini} + V_{D22}) & if\ low\ voltage\ operation \\ -N \cdot (V_{in} + V_{bdS1}) & if\ non\ low\ voltage\ operation \end{cases} \quad (44)$$

And the operation status (i.e. low voltage or non low voltage operation) can be determined by the comparison of $N\cdot(V_{in}+V_{bdS1})$ and $(V_{oini}+V_{D22})$. If the former one is smaller, then the converter is working under low voltage operation, otherwise, it is defined to be under non low voltage operation.

Theoretically, at the end of this stage, the voltage over C_{seq} needs to reach V_{oini}-V_{D21}. However, based on the model built above, this terminal condition will lead to an infinite time for the interval. In order to solve this issue, the final voltage over C_{seq} is assumed to reach only 95% of $(V_{oini}$-$V_{D21})$. Then, the end time can be written as

$$t_1 = t_0 + \ln\left(\frac{V_{oini}-V_{D21}-U_{csd01t0}}{(1-95\%)\cdot V_{oini}-V_{D21}}\right) \cdot T_{ccd01} \quad (45)$$

In terms of reliability, it is critical to build the model for this stage in order to predict the maximum voltage over the current sensing resistor RP_2. Thus, the parameters of a RC filter, which is utilized to suppress this voltage spike before the current signal goes into the control IC, can be determined.

Stage 2 [$t_1 < t < t_2$: Fig. 6 (b)]: The flyback transformer is magnetized during this stage until the magnetizing current reaches the pre-set value of the controller. The energy transfers from the capacitive load to the coupled inductor in this stage. To simplify the model, it is reasonable to neglect the effect of C_{seq} due to its really small value compared to the capacitance of the load. The output voltage, secondary side current I_s as well as the secondary winding current I_{sw} can be expressed as

$$V_{outd12}(t) = (V_{outd12t1} - V_{D21}) \cdot e^{\frac{L_s+R_{smd12}\cdot C_L\cdot R_{ceqs}}{2\cdot L_s\cdot C_L\cdot(R_{smd12}+R_{ceqs})}(t-t_1)} \cdot \{\cos[\omega_{d12}\cdot(t-t_1)] + \frac{R_{ceqs}\cdot C_L\cdot R_{smd12}-L_c}{AP_{d12}} \cdot \sin[\omega_{d12}\cdot(t-t_1)]\} + V_{D21} \quad (46)$$

$$I_{sd12}(t) = \frac{(V_{outd12t1}-V_{D21})}{R_{smd12}+R_{ceqs}} \cdot e^{-\frac{L_s+R_{smd12}\cdot C_L\cdot R_{ceqs}}{2\cdot L_s\cdot C_L\cdot(R_{smd12}+R_{ceqs})}(t-t_1)} \cdot \{-\cos[\omega_{d12}\cdot(t-t_1)] + \frac{L_s-2\cdot R_{ceqs}{}^2 C_L-R_{ceqs}\cdot C_L\cdot R_{smd12}}{AP_{d12}} \cdot \sin[\omega_{d12}\cdot(t-t_1)]\} \quad (47)$$

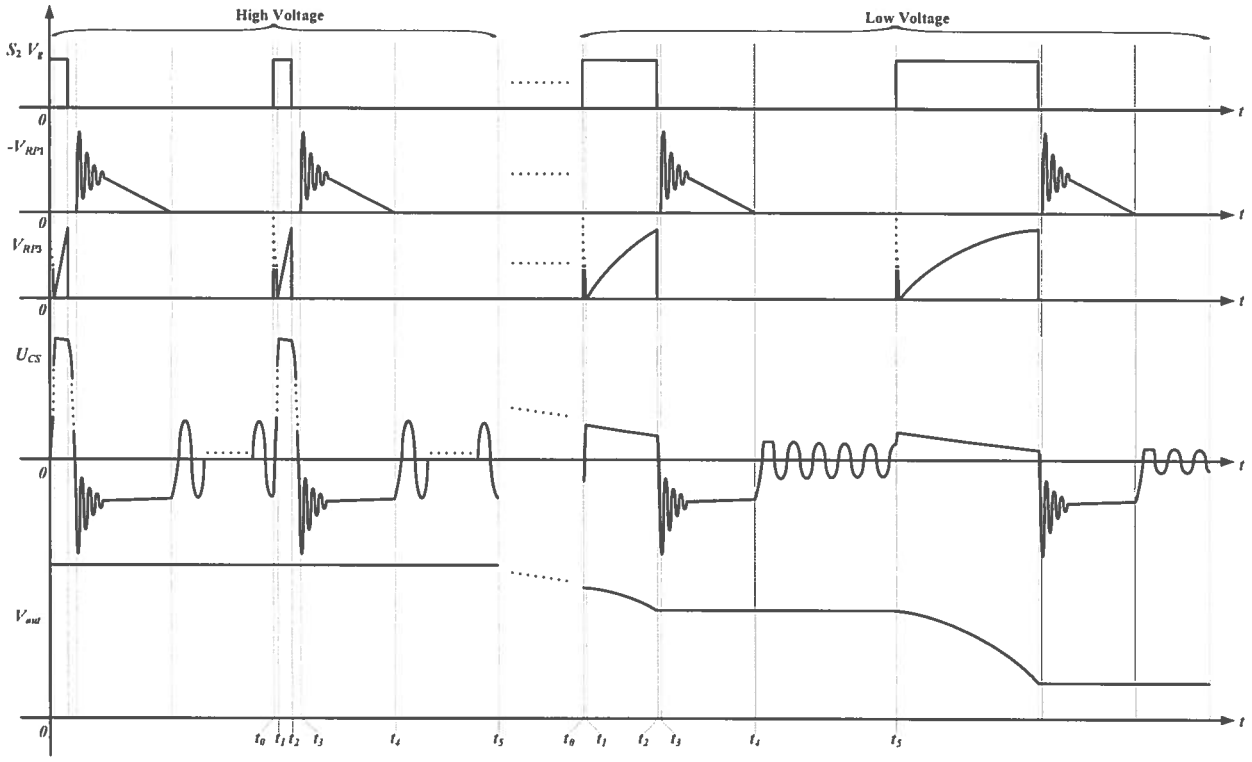


Fig. 7. Key waveforms of the operation stages under different output voltage levels.

$$I_{swd12}(t) = -\frac{2\cdot R_{ceqs}\cdot C_L\cdot(V_{outd12t1}-V_{D21})}{AP_{d12}}\cdot e^{-\frac{L_s+R_{smd12}\cdot C_L\cdot R_{ceqs}}{2\cdot L_s\cdot C_L\cdot(R_{smd12}+R_{ceqs})}(t-t_1)}\cdot \sin[\omega_{d12}\cdot(t-t_1)] \quad (48)$$

Then secondary winding voltage can be written as

$$U_{swd12}(t) = L_s\cdot\frac{dI_{swd12}(t)}{dt} \quad (49)$$

In these equations,

$$R_{smd12} = R_{dsonS2} + RP_2 + (R_{sw}@f_{fsd}) \quad (50)$$

$$AP_{d12} = \sqrt{\begin{matrix}4\cdot L_c\cdot C_L\cdot {R_{ceqs}}^2 \\ +2\cdot L_s\cdot C_L\cdot R_{smd12}\cdot R_{ceqs} \\ -{L_s}^2-{R_{smd12}}^2\cdot {C_L}^2\cdot {R_{ceqs}}^2\end{matrix}} \quad (51)$$

$$\omega_{d12} = \frac{AP_{d12}}{2\cdot L_s\cdot C_L\cdot(R_{smd12}+R_{ceqs})} \quad (52)$$

The capacitive load is assumed to be a constant voltage source in the previous stage and this assumption is beneficial in modeling the behavior in a simple way. However, this is not the real case and the voltage over capacitive load actually slightly decreases since the energy transfers to C_{seq}. Taking this into account, the initial condition of output voltage for stage [t_1-t_2] can be derived through the terminal voltage of C_{seq}, expressed as

$$V_{outd12t1} = U_{csd01}(t_1) + V_{D21} + I_{csd01}(t_1)\cdot R_{ccd01} \quad (53)$$

If the secondary peak current set by the inner current loop control is denoted as I_{sp}, the end time t_2 can be obtained through numerically solving the following equation

$$I_{sd12}(t_2) = -I_{sp} \quad (54)$$

Stage 3 [$t_2 < t < t_3$; Fig. 6 (c)]: When S_2 is switched off at the beginning of this stage, the energy stored in the coupled inductor cannot be immediately transferred to the primary side due to the reverse voltage over the body diode of S_1. In this stage, the behavior is the same as that in the stage [t_0-t_1] of the charging mode. However, the initial conditions are different here, which lead to a more complex model, expressed as

$$U_{csd23}(t) = e^{-\frac{L_s+R_{swd23}\cdot C_{seq}\cdot R_{ceqs}}{2\cdot L_s\cdot C_{seq}\cdot(R_{swd23}+R_{ceqs})}(t-t_2)}\cdot\{U_{csd12t2}\cdot \cos[\omega_{d23}\cdot(t-t_2)] + \frac{2\cdot R_{ceqs}\cdot L_s\cdot I_{swd12t2}+R_{ceqs}\cdot C_{seq}\cdot R_{swd23}\cdot U_{csd12t2}-L_s\cdot U_{csd12t2}}{AP_{d23}}\cdot \sin[\omega_{d23}\cdot(t-t_2)]\} \quad (55)$$

$$I_{swd23}(t) = e^{-\frac{L_s+R_{swd23}\cdot C_{seq}\cdot R_{ceqs}}{2\cdot L_s\cdot C_{seq}\cdot(R_{swd23}+R_{ceqs})}(t-t_2)}\cdot\{I_{swd12t2}\cdot \cos[\omega_{d23}\cdot(t-t_2)] - \frac{2\cdot R_{ceqs}\cdot C_{seq}\cdot U_{csd12t2}+R_{ceqs}\cdot C_{seq}\cdot R_{swd23}\cdot I_{swd12t2}-L_s\cdot I_{swd12t2}}{AP_{d23}}\cdot \sin[\omega_{d23}\cdot(t-t_2)]\} \quad (56)$$

$$U_{swd23}(t) = L_s \cdot \frac{dI_{swd23}(t)}{dt} \quad (57)$$

The parameters and conditions in these equations are summarized in Table VIII of Appendix. When the secondary winding voltage reaches previously defined U_{th}, the body diode of S_1 is forced to conduct and this interval ends. Hence, the end time can be obtained by numerically solving the following equation

$$U_{swd23}(t_3) = U_{th} \quad (58)$$

Stage 4 [$t_3 < t < t_4$: Fig. 6 (d)]: In this stage, the energy stored in the transformer will be transferred to the primary source. In addition, the energy which cannot be transferred to the primary side (i.e. the energy stored in the secondary side leakage inductance) will result in a resonance between the leakage inductance and the stray capacitance C_{seq}. During this period, it is more reasonable to consider the core loss equivalent resistance in the primary side, which can be calculated through (14). Hence, the primary winding voltage and current can be derived as

$$U_{pwd34}(t) = (U_{pwd23t3} - I_{pd34t3} \cdot R_{dmd34}) \cdot e^{-\frac{R_{dmd34} \cdot R_{ceqp}}{L_{pm} \cdot (R_{dmd34} + R_{ceqp})} \cdot (t - t_3)} + \frac{e^{-\frac{R_{swrd34}}{2 \cdot L_{sl}} \cdot (t - t_3)}}{N} \cdot \left\{ -R_{swrd34} \cdot I_{swd23t3} \cdot \cos[\omega_{d34} \cdot (t - t_3)] + \frac{(R_{swrd34}^2 \cdot C_{seq} - 2 \cdot L_{sl}) \cdot I_{swd23t3}}{AP_{d34}} \cdot \sin[\omega_{d34} \cdot (t - t_3)] \right\} \quad (59)$$

$$I_{pd34}(t) = \frac{U_{pwd23t3}}{R_{dmd34}} + e^{-\frac{R_{dmd34} \cdot R_{ceqp}}{L_{pm} \cdot (R_{dmd34} + R_{ceqp})} \cdot (t - t_3)} \cdot (I_{pd34t3} - \frac{U_{pwd23t3}}{R_{dmd34}}) + N \cdot e^{-\frac{R_{swrd34}}{2 \cdot L_{sl}} \cdot (t - t_3)} \cdot \left\{ I_{swd23t3} \cdot \cos[\omega_{d34} \cdot (t - t_3)] - \frac{R_{swrd34} \cdot C_{seq} \cdot I_{swd23t3}}{AP_{d34}} \cdot \sin[\omega_{d34} \cdot (t - t_3)] \right\} \quad (60)$$

The secondary winding voltage can be achieved through

$$U_{swd34}(t) = U_{pwd34}(t) \cdot N \quad (61)$$

The parameters and conditions used here can refer to Table VIII in the Appendix. At the end of this stage, the primary current reaches 0. Thus, the end time t_4 can be obtained by numerically solving the following equation

$$I_{pd34}(t_4) = 0 \quad (62)$$

Stage 5 [$t_4 < t < t_5$: Fig. 6 (e)]: This stage is the discontinuous conduction phase in the discharging mode and equivalent resistance of core loss does not affect in this stage. Due to the energy stored in the secondary side stray capacitor C_{seq} at the beginning of this stage, the secondary side inductance L_s starts to resonate with C_{seq}. The voltage over C_{seq} can be written as

$$U_{csd45}(t) = U_{csd34t4} \cdot e^{-\frac{R_{swd45}}{2 \cdot L_s} \cdot (t - t_4)} \cdot \left\{ \cos[\omega_{d45} \cdot (t - t_4)] + \frac{R_{swd45} \cdot C_{seq}}{AP_{d45}} \cdot \sin[\omega_{d45} \cdot (t - t_4)] \right\} \quad (63)$$

The parameters and conditions in these equations are summarized in Table VIII of Appendix.

Similar to the approach in analytical modeling for charging mode, based on the above derived accurate model, the estimated model can be achieved through setting the equivalent resistance of core loss R_{ceqs} to infinity to ignore the influence of core loss. The secondary winding voltages and time intervals for each stage of the estimated model can be acquired and utilized to calculate the equivalent resistance of core loss.

According to the current and voltage waveforms in Fig. 7, the rough *B-H* curves for high and low output voltages in the discharging process can be acquired, shown in Fig. 8. Thus, in discharging mode, the peak-to-peak flux density ΔB, core energy loss per cycle and the secondary side core loss equivalent resistance can be derived as

$$\Delta B = \int_{t_3}^{t_4} \frac{U_{swd34}(t)}{N_{sec} \cdot A} dt \quad (64)$$

$$E_v = V_e \cdot \frac{k_l \cdot \Delta B^{\beta - \alpha}}{|N_{sec} \cdot A|^{\alpha}} \cdot \sum_{m=1,2,3} \int_{t_m}^{t_{m+1}} \left| U_{swdm,m+1}(t) \right|^{\alpha} dt \quad (65)$$

$$R_{ceqs} = \frac{\sum_{m=1,2,3} \int_{t_m}^{t_{m+1}} U_{swdm,m+1}^2 dt}{E_v} \quad (66)$$

where $U_{swdm,m+1}(t)_{(m=1,2,3)}$ (i.e. $U_{swd12}(t)$, $U_{swd23}(t)$ and $U_{swd34}(t)$) are the voltages over secondary winding in stages [t_1-t_2] [t_2-t_3] and [t_3-t_4] in the discharging mode. It should be noted that stage [t_0-t_1] corresponds to the inrush charge of stray capacitance C_{seq} and does not contribute to the core loss. In stage [t_4-t_5], if neglecting the effect of winding resistance, the symmetric sinusoidal AC voltage of U_{cs} leads to the average zero change of the flux density (i.e. $\Delta B_{[t4\text{-}t5]} = 0$). Hence, this stage does not need to be considered in the core loss equivalent resistance calculation as well.

The achieved equivalent resistance of core loss R_{ceqs} then can be applied to the established accurate analytical model to obtain the detailed behavior of one switching cycle during the discharging process.

IV. Experimental Verification of Analytical Modeling

A prototype of bidirectional HV flyback converter was performed in order to validate the theoretical analytical

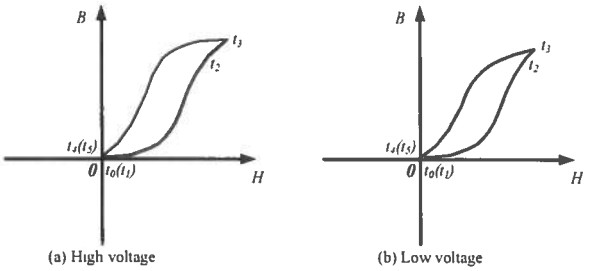


Fig. 8. *B-H* curves under different output voltage levels.

switching cycle modeling of the converter in terms of charging as well as discharge mode. The specifications, design parameters and the employed components are summarized in Table I. The implemented and measured data for the HV flyback transformer as well as the parameters for the core loss calculation are listed in Table II. The adoption of double layer Kapton tape between the primary and secondary winding can guarantee the galvanic isolation of the flyback transformer to reach at least 4 kV. The primary and secondary winding ac resistance of the transformer are frequency dependent and the measured resistance versus frequency characteristic up to 2 MHz are shown in Fig. 9 (a) and (b), respectively. The photograph of the prototype is shown in Fig. 10.

A. *Validation of analytical model of charging mode*

In charging mode, the analytical model is verified for both low voltage and high voltage operations. Fig. 11 (a) and (b) show the estimated and accurate analytical model based calculation waveforms, which are represented with dash line and solid line respectively, and experiments based measurement waveforms for low voltage operation. The end time for each stage of accurate model based waveforms in Fig. 11 (a) and measured waveforms in Fig. 11 (b) as well as the time intervals are summarized in Table III. Likewise, the estimated and accurate calculated waveforms and measured waveforms in high operation voltage are shown in Fig. 12 (a) and (b), respectively. The corresponding end time and time intervals for high voltage operation are listed in Table IV.

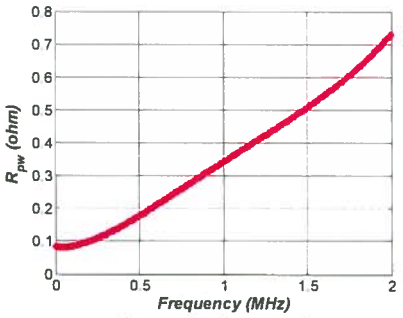
The waveforms in Fig. 11 (a) indicate that, in the entire switching cycle, the estimated model based waveforms are almost equal to that based on the accurate model. Only slight differences can be observed in the gray zoom boxes. During the high voltage operation (Fig. 12 (a)), the waveforms based on estimated model are obviously different from that based on accurate model due to the severe influence of core loss. Even in the cases with slight differences, it is still crucial to build the accurate model for each cycle. Since the whole charging process consists of large number of switching cycles, the slight error in one cycle tends to be accumulated accordingly, which eventually leads to the large error in the efficiency evaluation. For the converter with only capacitive load, energy efficiency is more applicable rather than the power efficiency. The charging efficiency can be defined as the final energy stored in the capacitive load (E_{stored}) divided by the total input energy into the converter E_{in}, which can be

TABLE I HV FLYBACK CONVERTER SPECIFICATIONS AND COMPONENTS LIST

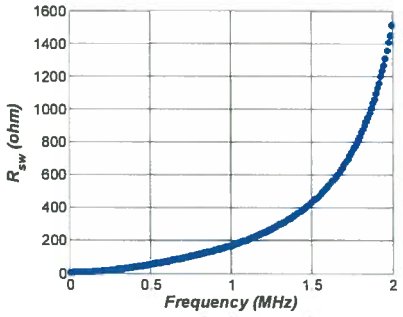
Parameters	Values
V_{in}	3 V
Maximum V_{out}	2 kV
C_L	220 nF
I_{pp}	4 A
I_{sp}	100 mA
S_1	BSC320N20NS3 G
S_2	IXTV03N400S
D_{21} & D_{22}	VMI6525
RP_1	20 mΩ 1 %
RP_2 & RP_3	1 Ω 1 %

TABLE II HV FLYBACK TRANSFORMER IMPEMENTED AND MEASURED PARAMETERS

Parameters	Values
Core type (material)	EF20 (Ferrite N27)
N_{pri}	6
N_{sec}	232
N	38.7
L_{pm}	12.7 μH
L_{pl}	300 nH
L_{sm}	18.4 mH
L_{sl}	450 μH
C_{seq}	30 pF
k	12.97
α	1.26
β	2.02
A	32.8 mm^2
V_e	1564 mm^3



(a) Primary winding ac resistance



(b)Secondary winding ac resistance

Fig. 9 HV flyback transformer winding ac resistance.

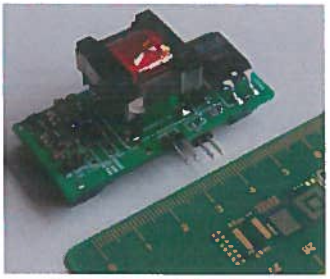
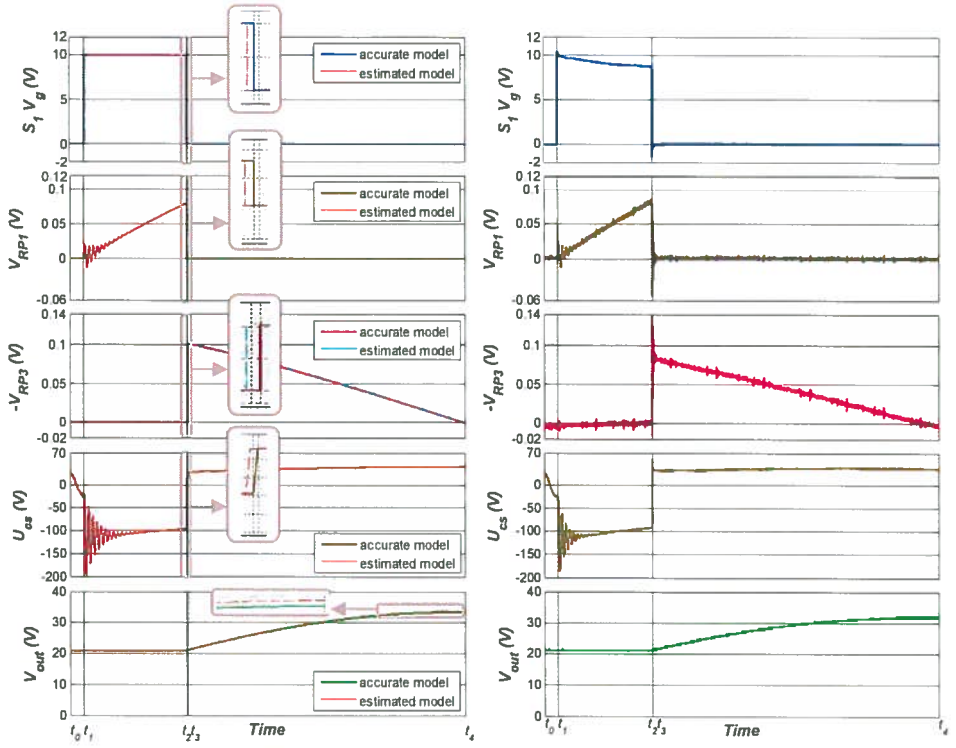
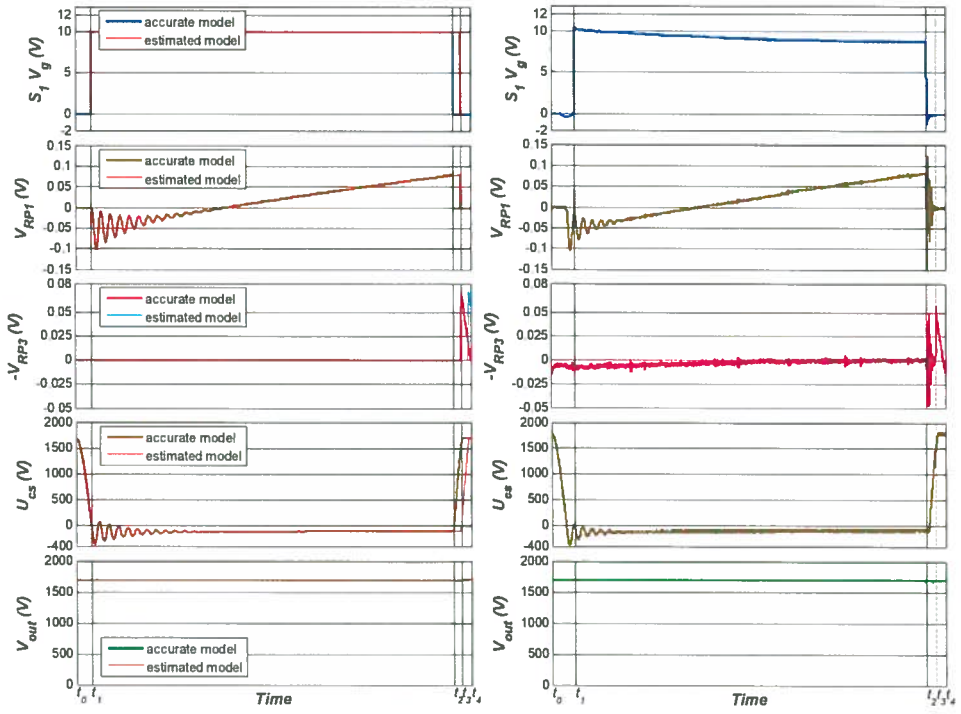


Fig. 10 Picture of the implemented bidirectional HV flyback converter.



(a) Analytical model based calculated waveforms (b) Experimental waveforms

Fig. 11. Low voltage operational key waveforms of charging mode.



(a) Analytical model based calculated waveforms (b) Experimental waveforms

Fig. 12. High voltage operational key waveforms of charging mode.

expressed as

$$\eta_{charge} = \frac{E_{stored}}{E_{in}} \tag{67}$$

The measured efficiency as well as the analytical model based efficiency is shown in Fig. 13, which can effectively prove the necessity to build the accurate model.

TABLE III TIME DATA AND TIME INTERVALS IN FIG. 11

Time or Time Intervals	Accurate Model based Calculated Time / μs	Measured Time / μs
t_0	0	0
t_1	2.58	2.52
t_2	21.70	19.75
t_3	21.75	19.79
t_4	73.23	72.43
$t_{01} = t_1 - t_0$	2.58	2.52
$t_{12} = t_2 - t_1$	19.12	17.23
$t_{23} = t_3 - t_2$	0.05	0.04
$t_{34} = t_4 - t_3$	51.48	52.64

TABLE IV TIME DATA AND TIME INTERVALS IN FIG. 12

Time or Time Intervals	Accurate Model based Calculated Time / μs	Measured Time / μs
t_0	0	0
t_1	1.32	1.84
t_2	31.37	29.76
t_3	32.07	30.50
t_4	32.82	31.24
$t_{01} = t_1 - t_0$	1.32	1.84
$t_{12} = t_2 - t_1$	30.05	27.92
$t_{23} = t_3 - t_2$	0.7	0.74
$t_{34} = t_4 - t_3$	0.75	0.74

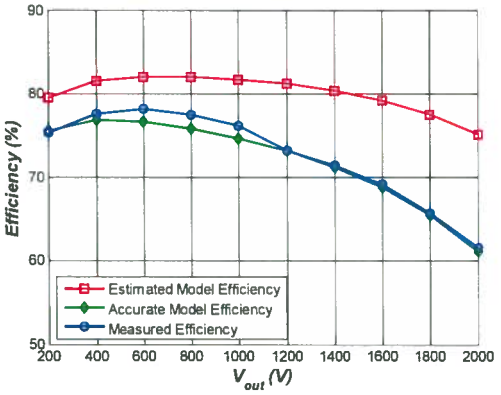


Fig. 13. Comparison of analytical model based charging efficiency and experimentally measured efficiency.

Even with the accurate model, due to the difficulty in accurately calculating the core loss, the parasitic capacitance introduced by the measuring probes in the high voltage side as well as the measuring errors caused by the oscilloscope, the calculated secondary side current and the output voltage cannot be exactly the same as the measured ones. In addition, the measurement error in the winding resistances will greatly affect the damping phenomenon in stage $[t_1 < t < t_2]$. In the high voltage operation, since the on time for the body diode of S_1 in stage $[t_1 < t < t_2]$ is neglected in the calculation for simplifying the model, thus, the time t_1 in the measurement is much larger than the time in the calculation. Furthermore, as previously stated, the resonance phenomenon when S_1 is switched off is ignored in the analytical model as well. Moreover, due to the intrinsic property of the control IC, the driving voltage for S_1 has a slight decline. However, in general, the mismatch between the calculated time data and the measured ones are under acceptable range and the analytical model can well represent the behavior in one switching cycle for charging mode.

B. *Validation of analytical model of discharging mode*

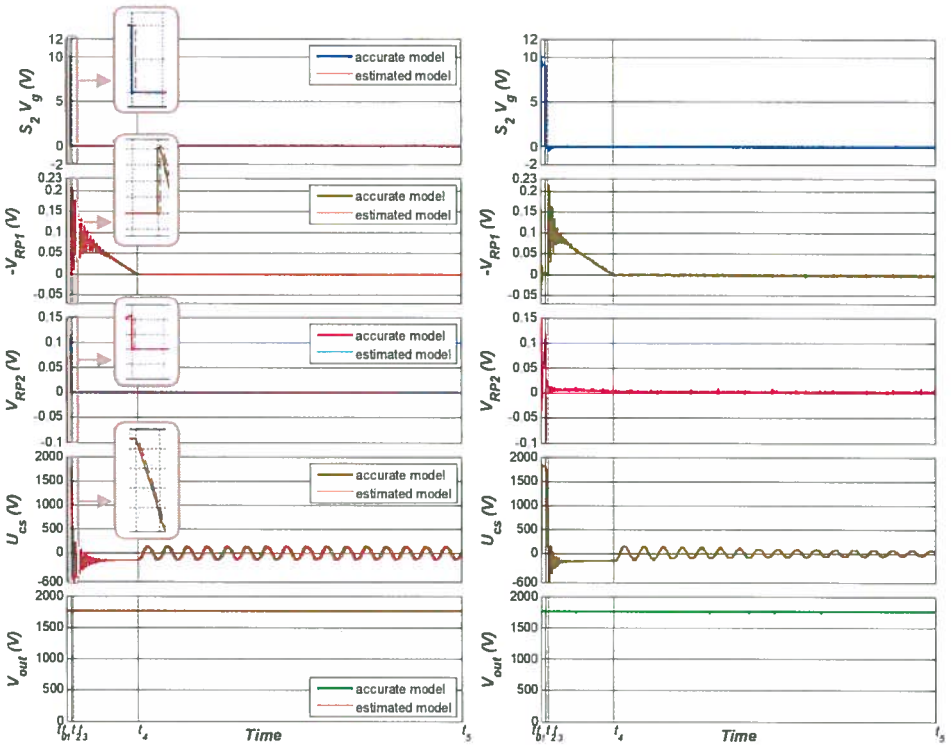
The analytical model is also validated for both high and low operational voltages in the discharging mode. Fig. 14 (a) and (b) illustrate both the estimated model and accurate model based calculation waveforms and experiment waveforms for high voltage operation. The end time for each stage based on accurate model in Fig. 14 and the time intervals are summarized in Table V. Similarly, the calculated and measured waveforms in low operational voltage are shown in Fig. 15 (a) and (b), respectively. The corresponding end time and time intervals for low voltage operation are listed in Table VI. Similar to the situation in charging mode, the estimated model based waveforms in Fig. 14 (a) and Fig. 15 (a) look nearly the same to that based on accurate model and only slight difference can be observed in the gray zoom boxes. Since the discharging process also consists of a lot of successive switching cycles, the slight error in one switching cycle tends to result in the large error in the efficiency calculation. Similarly, the discharging efficiency can be defined as the recovered energy $E_{recovered}$ divided by the stored energy, which can be expressed as

$$\eta_{discharge} = \frac{E_{recovered}}{E_{stored}} \tag{68}$$

The large error between the estimated model based discharging efficiency and its measured counterpart is illustrated in Fig. 16. It should be noted that, in the discharging process, the secondary side peak current varies with the output voltage due to the intrinsic issue of the control IC. Even with the accurate model based calculated waveforms, end time and time intervals cannot exactly match with the measured counterparts. The reasons for the mismatch have already been stated in the charging mode verification. In general, the difference can be accepted and the analytical model can also well represent the behavior in one switching cycle for discharging mode. It can be observed that the discharging efficiencies shown in Fig. 16 are much lower than the charging efficiencies. This is mainly due to the high on resistance of HV MOSFET S_2 as well as the body diode of S_1, which only work in the discharging mode.

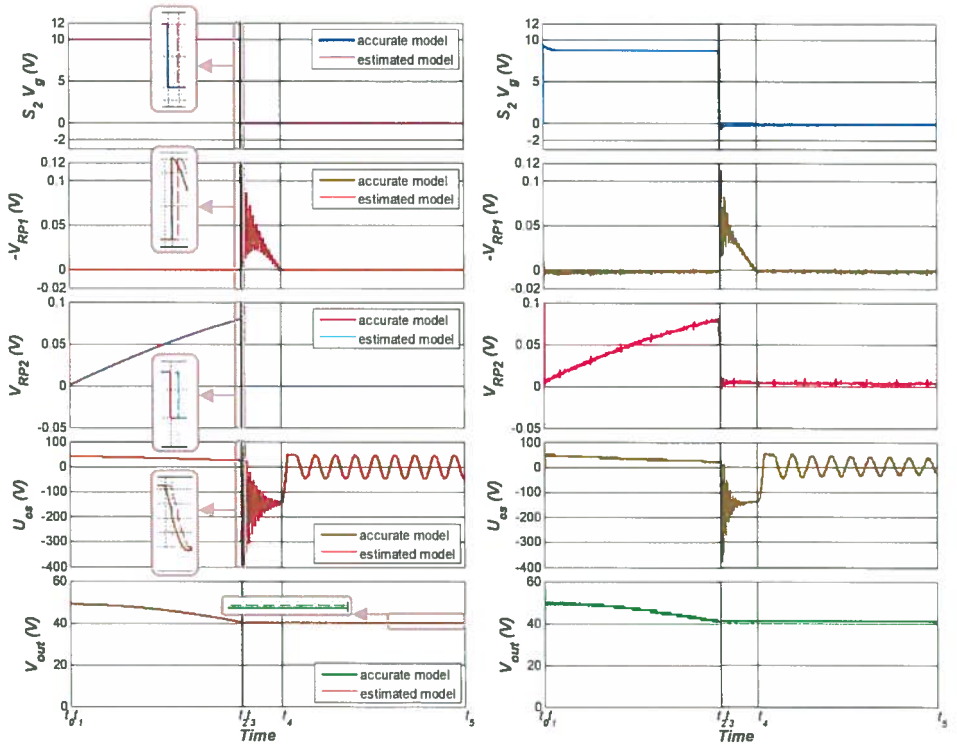
V. CONCLUSION

In this paper, the HV bidirectional flyback converter utilized to drive the capacitive load is introduced in terms of configuration and fundamental operational principles. For both charging and discharging mode, an accurate behaviour model has been established first. By ignoring the effect of core loss in accurate model, an estimated model is achieved in order to derive the core loss equivalent resistance. Afterwards,



(a) Analytical model based calculated waveforms (b) Experimental waveforms

Fig. 14. High voltage operational key waveforms of discharging mode



(a) Analytical model based calculated waveforms (b) Experimental waveforms

Fig. 15. Low voltage operational key waveforms of discharging mode

an accurate behaviour can be predicted with the accurate model as well as the derived core loss equivalent resistance. The analytical model is verified by the comparison between the model based calculation waveforms and the experiment

TABLE V. TIME DATA AND TIME INTERVALS IN FIG. 14

Time or Time Intervals	Calculated Time / μs	Measured Time / μs
t_0	0	0
t_1	0.011	0.0120
t_2	1.21	1.25
t_3	1.71	1.85
t_4	18.11	18.39
t_5	100	99.39
$t_{01} = t_1 - t_0$	0.011	0.012
$t_{12} = t_2 - t_1$	1.199	1.238
$t_{23} = t_3 - t_2$	0.5	0.6
$t_{34} = t_4 - t_3$	16.4	16.54
$t_{45} = t_5 - t_4$	81.89	81

TABLE VI. TIME DATA AND TIME INTERVALS IN FIG. 15

Time or Time Intervals	Calculated Time / μs	Measured Time / μs
t_0	0	0
t_1	0.013	0.016
t_2	43.73	44.6
t_3	43.8	44.66
t_4	53.8	53.93
t_5	100	99.43
$t_{01} = t_1 - t_0$	0.013	0.016
$t_{12} = t_2 - t_1$	43.717	44.584
$t_{23} = t_3 - t_2$	0.07	0.06
$t_{34} = t_4 - t_3$	10	9.27
$t_{45} = t_5 - t_4$	46.2	45.5

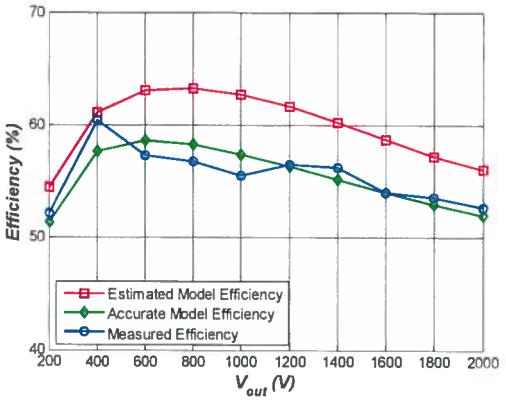


Fig. 16. Comparison of analytical model based discharging efficiency and experimentally measured efficiency.

based measurement waveforms. Even though the accuracy of the parasitic parameters and the core loss calculation affect the agreement between the calculated and measured results, the difference is still under accepted level and the analytical model can well represent the behavior in one switching cycle for both charging and discharging mode. The estimated and accurate model based calculated efficiency as well as the measured data are compared to verify the necessity of employing the accurate model as well as to validate the importance of considering the core loss. The switching cycle based analytical model can be dedicated to the components stress analysis, energy efficiency investigation and optimizing the design for HV bidirectional converter driving capacitive load.

APPENDIX

TABLE VII. PARAMETERS AND INITIAL CONDITIONS OF DIFFERENT STAGES IN CHARGING MODE

Stages	Stage 2 *[$t_1 < t < t_2$: Fig. 3 (b)]*	Stage 3 *[$t_2 < t < t_3$: Fig. 3 (c)]*	Stage 4 *[$t_3 < t < t_4$: Fig. 3 (d)]*
Parameters and initial conditions	**Low voltage operation:** $U_{csc01t1} = U_{csc01}(t_1)$ $C_{preq} = C_{seq} \cdot N^2$ $R_{preqc12} = \frac{R_{swc12rl}}{N^2} + R_{dsonS1} + RP_1$ $R_{swc12rl} = R_{sw}@\frac{1}{2\pi \cdot \sqrt{L_{pl} \cdot C_{preq}}}$ $AP_{c12rl} = \sqrt{\frac{4 \cdot L_{pl} \cdot C_{preq}}{-R_{preqc12}{}^2 \cdot C_{preq}{}^2}}$ $\omega_{c12rl} = \frac{AP_{c12rl}}{2 \cdot L_{pl} \cdot C_{preq}}$ **Non low voltage operation:** $I_{csc01t1} = I_{csc01}(t_1)$ $R_{swc12rh} = R_{sw}@\frac{1}{2\pi \cdot \sqrt{L_{sl} \cdot C_{seq}}}$ $AP_{c12rh} = \sqrt{\frac{4 \cdot L_{sl} \cdot C_{seq}}{-R_{swc12rh}{}^2 \cdot C_{seq}{}^2}}$ $\omega_{c12rh} = \frac{AP_{c12rh}}{2 \cdot L_{sl} \cdot C_{seq}}$	$R_{swc23} = R_{sw}@\frac{1}{2\pi \cdot \sqrt{L_{sm} \cdot C_{seq}}}$ $AP_{c23} = \sqrt{\frac{4 \cdot L_{sm} \cdot C_{seq} \cdot R_{ceqs}{}^2 + 2 \cdot L_{sm} \cdot C_{seq} \cdot R_{swc23} \cdot R_{ceqs} - L_{sm}{}^2}{-R_{swc23}{}^2 \cdot C_{seq}{}^2 \cdot R_{ceqs}{}^2}}$ $\omega_{c23} = \frac{AP_{c23}}{2 \cdot L_{sm} \cdot C_{seq} \cdot (R_{swc23} + R_{ceqs})}$ $U_{csc12t2} = U_{csc12}(t_2)$ $I_{swc12t2} = N \cdot (I_{pc12}(t_2) - \frac{U_{pwc12}(t_2)}{R_{ceqp}})$	$I_{swc23t3} = I_{swc23}(t_3)$ $R_{fwc34} \approx RP_3 + R_{sw}@f_{swideal}$ $AP_{c34} = \sqrt{\frac{4 \cdot L_{sm} \cdot C_L \cdot R_{ceqs}{}^2 + 2 \cdot L_{sm} \cdot C_L \cdot R_{fwc34} \cdot R_{ceqs} - L_{sm}{}^2}{-R_{fwc34}{}^2 \cdot C_L{}^2 \cdot R_{ceqs}{}^2}}$ $\omega_{c34} = \frac{AP_{c34}}{2 \cdot L_{sm} \cdot C_L \cdot (R_{fwc34} + R_{ceqs})}$

TABLE VIII. PARAMETERS AND INITIAL CONDITIONS OF DIFFERENT STAGES IN DISCHARGING MODE

Stages	Stage 3 *[$t_2 < t < t_3$: Fig. 6 (c)]*	Stage 4 *[$t_3 < t < t_4$: Fig. 6 (d)]*	Stage 5 *[$t_4 < t < t_5$: Fig. 6 (e)]*
Parameters and initial conditions	$U_{csd12t2} = V_{outd12}(t_2) + I_{sd12}(t_2) \cdot RP_2 - V_{D21}$ $I_{swd12t2} = \frac{V_{outd12}(t_2) + I_{sd12}(t_2) \cdot (RP_2 + R_{swd23}) - V_{D21}}{R_{ceqs}} + I_{sd12}(t_2)$ $R_{swd23} = R_{sw}@\frac{1}{2\pi \cdot \sqrt{L_s \cdot C_{seq}}}$ $AP_{d23} = \sqrt{\frac{4 \cdot L_s \cdot C_{seq} \cdot {R_{ceqs}}^2}{-{L_s}^2 - {R_{swd23}}^2 \cdot {C_{seq}}^2 \cdot {R_{ceqs}}^2 + 2 \cdot L_s \cdot C_{seq} \cdot R_{swd23} \cdot R_{ceqs}}}$ $\omega_{d23} = \frac{AP_{d23}}{2 \cdot L_s \cdot C_{seq} \cdot (R_{swd23} + R_{ceqs})}$	$U_{pwd23t3} = V_{in} + V_{bdS1}$ $I_{swd23t3} = I_{swd23}(t_3)$ $I_{pd34t3} = I_{swd23t3} \cdot N + \frac{U_{pwd23t3}}{R_{ceqp}}$ $R_{dmd34} = RP_1 + (R_{pw}@f_{fsd})$ $R_{swrd34} = R_{sw}@\frac{1}{2\pi \cdot \sqrt{L_{sl} \cdot C_{seq}}}$ $AP_{d34} = \sqrt{\frac{4 \cdot L_{sl} \cdot C_{seq}}{-{R_{swrd34}}^2 \cdot {C_{seq}}^2}}$ $\omega_{d34} = \frac{AP_{d34}}{2 \cdot L_{sl} \cdot C_{seq}}$	$U_{csd34t4} = -N \cdot U_{pwd34}(t_4)$ $R_{swd45} = R_{sw}@\frac{1}{2\pi \cdot \sqrt{L_s \cdot C_{seq}}}$ $AP_{d45} = \sqrt{\frac{4 \cdot L_s \cdot C_{seq}}{-{R_{swd45}}^2 \cdot {C_{seq}}^2}}$ $\omega_{d45} = \frac{AP_{d45}}{2 \cdot L_s \cdot C_{seq}}$

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