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Analytical Threshold Voltage Modeling of Surrounding Gate Silicon Nanowire Transistors with Different Geometries

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Abstract – In this paper, we propose new physically based threshold voltage models for short channel Surrounding Gate Silicon Nanowire Transistor with two different geometries. The model explores the impact of various device parameters like silicon film thickness, film height, film width, gate oxide thickness, and drain bias on the threshold voltage behavior of a cylindrical surrounding gate and rectangular surrounding gate nanowire MOSFET. Threshold voltage roll-off and DIBL characteristics of these devices are also studied. Proposed models are clearly validated by comparing the simulations with the TCAD simulation for a wide range of device geometries.

Keywords: Junction Based Cylindrical Surrounding Gate (JBCSG) silicon nanowire transistor, Rectangular surrounding gate silicon nanowire transistor, Threshold voltage, Parabolic approximation, silicon thickness, Channel Length, drain Bias.

1. Introduction

The requirement for Nano electronic devices to have large computing power with less power consumption and smaller dimensions has lead to device miniaturization. There are a number of drawbacks in the downscaling process of a conventional MOSFET, such as the short channel effects and the gate-leakage-current. Hence in these conditions, Silicon Nanowire Transistors have garnered a huge attention in the modern semiconductor industry as the alternate option for the conventional MOSFETs due to their highly improved electrical and optical properties [1]. Devices based on silicon nanowires are bound to have high electrostatic control over the channel and reduced short channel effects.

Modeling of nanowire field effect transistors have been the subject of several investigation, both analytical and numerical. Analytical models are based on two assumptions, 1) an undoped semiconductor nanowire and 2) Boltzmann statistics [2-6]. These assumptions allow, in fact, for a closed form solution of Poisson's Eqs. [2, 3], that makes it possible to work out an intrinsic analytical relationship between the gate voltage and surface potential. Alternatively, the assumption is taken of a completely depleted nanowire, consistently with the investigation of Sub threshold Slope (SS) and short channel effects [7]. A new study on the gate capacitance of a surrounding gate nanowire transistor studies the acceptor type doping [8] such that the carriers are confined only within the inversion layer.

Numerical approaches, instead, account for nearly all of the relevant effects that exert an impact on the device behavior, including motion quantization, sub band splitting, Fermi statistics, quasi ballistic transport, surface and channel orientation, and band structure [9-11]. The classical single gate MOSFET is approaching its minimum channel length due to the limits imposed by gate oxide tunneling. For extending the scalability of CMOS technology several non classical MOSFETs have been proposed that are being the subject of intense research. Fig. 1 shows some of the non planar MOSFET devices with different geometries.

The use of several gates has shown good electrostatic control of the channel and, therefore, the possibility of higher reduction in channel length compared to traditional bulk MOSFETs. Structures such as FINFETs, Double Gate, Tri Gate, Surrounding Gate, Omega Gate and Gate-All-Around MOSFETs are preferred to planar structures as

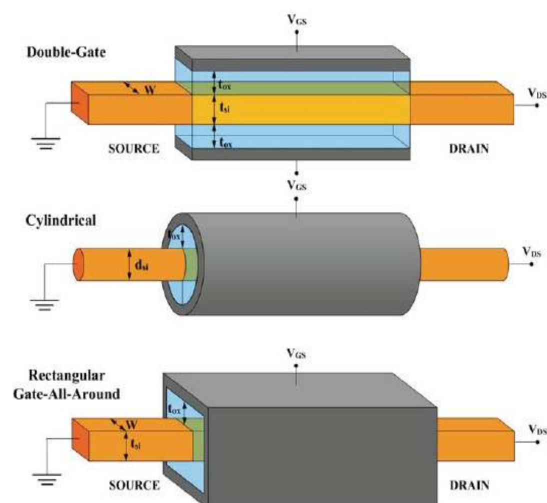

Fig. 1. Non Planar MOSFETs with different geometric specifications

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they have a steep sub threshold voltage and reduced leakage currents for very short channel lengths [12]. Drain Induced Barrier Lowering (DIBL), threshold voltage roll-off, and off-state leakage current are greatly reduced in these devices [13, 14].

Surrounding Gate MOSFETs are one of the most promising structures beyond bulk CMOS. Since early investigations on Surrounding Gate / SOI devices [15], most recent experiments have demonstrated GAA Silicon Nanowires with controlled diameters on the order of 3-6 nm using conventional CMOS technology [16]. Theoretically, Surrounding Gate MOSFETs provide better gate electrostatic control capability than planar and double gate devices. We propose to develop a feasible physics based analytical model for the Surrounding Gate Nanowire MOSFET with two different geometries; a Junction Based Cylindrical Surrounding Gate Device and a Rectangular Surrounding Gate Device.

2. Modeling of Cylindrical SG Nanowire MOSFET

A number of analytical models for the Surrounding Gate devices have been proposed in the past by various research scholars. A simple threshold voltage model for a Surrounding Gate MOSFET transistor has been proposed by C.P. Auth and James D. Plummer in 1998 [17]. This model determines the channel potential using perimeter weighted summation method. Threshold voltage model for a Omega Gate Transistor was proposed by Biswajit Ray and Santanu Mahapathra in 2008 [18]. This model can be considered as the generalized model for the Surrounding Gate and Semi-Surrounding Gate Cylindrical Transistors. Te-Kuang Chiang proposed a model on surrounding gate MOSFET with localized interface charges with potential approximation using parabolic approximation in 2010 [19] and using an alternative approach of perimeter weighted summation method in 2011 [20]. M. Jagadesh Kumar et.al. have proposed a threshold voltage model for the dual material surrounding gate that includes the physical properties of both the materials used in the gate [21]. A new threshold voltage model for a short channel Junction Less Cylindrical Surrounding Gate MOSFET has been developed by T.K.Chiang in 2012 [22].

In the sub threshold operation of a Junction Based device, the channel region is fully depleted by the flat band voltage and the gate bias is used to induce the minority carriers at the semiconductor – insulator interface. Due to the 3-D channel potential, $\varphi(r, z, \theta)$ is symmetrical in the θ direction. Hence the 2-D Poisson equation for a Junction Based Cylindrical Surrounding Gate Transistor with a uniform impurity distribution is given by [22].

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\varphi(r,z)\right)+\frac{\partial^2}{\partial z^2}\varphi(r,z)=\frac{qN_A}{\varepsilon_{si}} \tag{1}$$

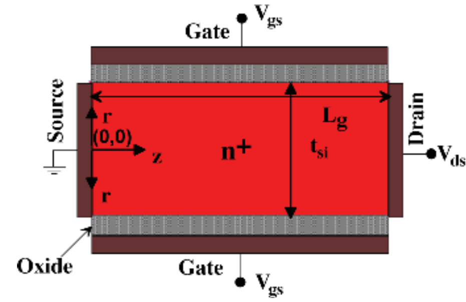

Fig. 2. Junction Based Cylindrical Surrounding Gate (JBCSG) MOSFET.

where $\varphi(r,z)$ is the 2-D channel potential and N_A is the channel doping density.

Using the parabolic potential approximation method, the 2-D potential vertical to the channel is given by [22],

$$\varphi(r,z)=C_1(z)+C_2(z)r+C_3(z)r^2 \tag{2}$$

Certain assumptions are done to determine the channel potential [22]. They are as given below:

1) The electrical flux between the silicon film and surrounding gate oxide must be continuous.
2) The electrical field at $r=0$ must be zero due to the symmetry of the channel potential along the r-direction.

Now the channel potential can be obtained as

$$\varphi(r,z)=\varphi_c(z)+\frac{C_{ox}\left(V_{gs}-V_{fb}-\varphi_s(z)\right)}{\varepsilon_{si}t_{si}}r^2 \tag{3}$$

Where V_{fb} is the flat band voltage, C_{ox} is the gate oxide capacitance per unit area, and t_{si} is the silicon film thickness. $\varphi_s(z)$ and $\varphi_c(z)$ are the surface and centre potential respectively that should satisfy the following Eq. [22].

$$\varphi_s(z)=\varphi_c(z)+\frac{C_{ox}t_{si}\left(V_{gs}-V_{fb}-\varphi_s(z)\right)}{4\varepsilon_{si}} \tag{4}$$

In case of a Junction Based Transistor, we are concerned about the surface potential and the centre potential has to be eliminated.

Hence by substituting Eqs. (3) and (4) in Eq. (1) we get,

$$\frac{d^2\varphi_s(z)}{dz^2}-\frac{1}{\lambda^2}\left(\varphi_s(z)-\varphi_s\right)=0 \tag{5}$$

φ_s is the surface potential and λ is the scaling length. Their values are given by,

$$\frac{1}{\lambda^2}=\frac{4C_{ox}}{\varepsilon_{si}t_{si}} \tag{6}$$

$$\varphi_s = V_{gs} - V_{fb} - \frac{qN_A t_{si}}{4C_{ox}} \quad (7)$$

where t_{ox} is the oxide film thickness. The general solution of the differential equation in (5) is given by,

$$\varphi_s(z) = ae^{z/\lambda} + be^{-z/\lambda} + \varphi_s \quad (8)$$

The coefficients of a and b can be determined by applying the boundary conditions as $\varphi_s(z=0)=0$ and $\varphi_s(z=L_{eff})=V_{ds}$. By applying the above conditions we get,

$$a + b + \varphi_s = 0 \quad (9)$$

$$a.e^{L_{eff}/\lambda} + b.e^{L_{eff}/\lambda} + \varphi_s = V_{ds} \quad (10)$$

By solving and rearranging, the values of a and b are obtained as,

$$a = \frac{V_{ds} - \varphi_s(1 - e^{-L_{eff}/\lambda})}{2\sinh(L_{eff}/\lambda)} \quad (11)$$

$$b = \frac{-V_{ds} + \varphi_s(1 - e^{L_{eff}/\lambda})}{2\sinh(L_{eff}/\lambda)} \quad (12)$$

The surface potential is given by,

$$\varphi_s(z) = \alpha V_{gs} + \beta \quad (13)$$

$$\varphi_s(z) = \gamma V_{gs} + \kappa \quad (14)$$

Where,

$$\alpha V_{gs} + \beta = a \quad (15)$$

$$\gamma V_{gs} + \kappa = b \quad (16)$$

And here the effective length is given by,

$$L_{eff} = L_g - L_s - L_d - 2L_D \quad (17)$$

L_g is the gate length while L_s and L_d are source and drain depletion widths respectively. Now L_d, the Debye length, by accounting for the transition regions separating the drift and diffusion regions of the channel, is given by [23].

$$L_D = \sqrt{\frac{2\varepsilon_{si}KT}{q^2 N_A}} \quad (18)$$

where T is the absolute temperature and K is the Boltzmann constant. The Minimum Surface Potential in (8) is now derived from the previous equations as,

$$\varphi_{s,\min}(z) = 2\sqrt{ab} + \varphi_s = 2\varphi_B \quad (19)$$

The bulk potential φ_B is now given by

$$\varphi_B = \frac{KT}{q}\ln\left(\frac{N_A}{n_i}\right) \quad (20)$$

n_i is the intrinsic carrier concentration of silicon.

Setting the Minimum Surface Potential (MSP) to be two times the bulk potential and solving for the gate voltage V_{gs}, the threshold voltage for the Junction Based transistor is obtained.

$$V_{th,JB} = \frac{B_{JB} + \sqrt{B_{JB}^2 - A_{JB}C_{JB}}}{A_{JB}} \quad (21)$$

The values of A_{JB}, B_{JB} and C_{JB} and the associated fitting parameters are listed here.

$$A_{JB} = 1 - 4\alpha\gamma \quad (22)$$

$$B_{JB} = 2(\beta\gamma + \alpha\kappa) + (\omega + 2\varphi_B) \quad (23)$$

$$C_{JB} = (\omega + 2\varphi_B)^2 - 4\beta\kappa \quad (24)$$

$$\omega_{JB} = V_{fb} + \frac{qN_A t_{si}}{4C_{ox}} \quad (25)$$

$$\alpha = \frac{\left(e^{-L_{eff}/\lambda} - 1\right)}{2\sinh\left(L_{eff}/\lambda\right)} \quad (26)$$

$$\beta = \frac{V_{ds} - \omega\left(e^{-L_{eff}/\lambda} - 1\right)}{2\sinh\left(L_{eff}/\lambda\right)} \quad (27)$$

$$\gamma = \frac{1 - e^{L_{eff}/\lambda}}{2\sinh\left(L_{eff}/\lambda\right)} \quad (28)$$

$$\kappa = \frac{-V_{ds} + \omega(e^{L_{eff}/\lambda} - 1)}{2\sinh\left(L_{eff}/\lambda\right)} \quad (29)$$

3. Modeling of Rectangular SG Nanowire MOSFET

An analytical threshold voltage model for GAA Nanoscale MOSFETs considering the hot carrier induced interface charges have been proposed by Z.Ghoggali et al., in 2008 [24]. Quantum confinement and its effects on threshold voltage variations in short channel GAA devices have been studied by Y.S.Wu and Pin Su in 2009 [25]. A

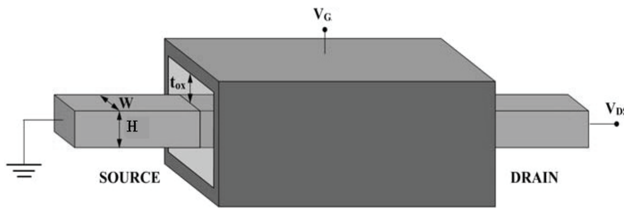

Fig. 3. Schematic Diagram of a Rectangular Surrounding Gate Nanowire MOSFET

physically based classical model for body potential of a GAA nanowire transistor has been proposed by Biswajit Ray and Santanu Mahapathra in 2008 [26]. A quasi and analytical model for predicting the potential of a nanowire FET has been proposed by De Michielis in 2010 [27]. Here, we consider a lightly doped rectangular surrounding gate nanowire MOSFET, bound to have high gate control, in the weak inversion region, where both fixed and mobile charge densities in the channel are negligible. In modeling the threshold voltage, the quantum effects are also considered, as the quantization of the electron energy in ultra thin devices can never be ignored. One important consequence of the quantum mechanical carrier distribution, in accordance with the device behavior, occurs when the device geometries and silicon thickness are varied, so a reliable compact model for the nanowire transistors must also take into account the quantum effects resulting out of these variations.

The proposed physically based closed form model holds good for ultra thin and ultra short channel surrounding gate devices and does not employ any unphysical fitting parameter. The compact threshold voltage model is obtained by solving the 3D Poisson equation and 2D Schrodinger equations in the inversion region. These equations are then consistently solved to obtain the potential distribution and inversion charge density.

In the weak inversion regime, we have approximated the Poisson equation as Laplace equation with the inversion charge density neglected, and thus the two equations are decoupled. Assuming a flat potential on the plane perpendicular to the source-drain direction in the nanowire, neglecting the charge densities ensure that no self consistency problems arise in the nanowire. The mid gap metals are used for gate, intended to suppress the silicon gate poly depletion induced parasitic capacitances. The 3-D Poisson equation is solved to obtain the threshold voltage in the weak inversion region, including the parabolic band approximation. Hence the potential distribution in the insulator and silicon regions can be expressed as [28].

$$\frac{\delta^2\psi(x,y,z)}{\delta x^2}+\frac{\delta^2\psi(x,y,z)}{\delta y^2}+\frac{\delta^2\psi(x,y,z)}{\delta z^2}=0 \quad (30)$$

The potential ψ in terms of x (width), y (height) and z (length) is to be determined. The boundary conditions defined by the physics of the device [9] are given by,

$$\psi(x,-H/2-T_{OX},z)=V_g \quad (31)$$

$$\psi(-W/2-T_{OX},y,z)=Vg` \quad (32)$$

$$\frac{\delta\psi}{\delta x}\Big|_{x=0}=0 \quad (33)$$

$$\frac{\delta\psi}{\delta y}\Big|_{y=0}=0 \quad (34)$$

$$\psi(x,y,0)=\psi_{bi} \quad (35)$$

$$\psi(x,y,L)=\psi_{bi}+V_{ds} \quad (36)$$

Where, V_g is the gate voltage, ψ_{bi} is the built in potential, L is the channel length, V_{ds} is the drain to source voltage which is negligible for low V_{ds}. For a rectangular surrounding gate device, we have to find the insulator potential on all sides of the channel under consideration. So the height and width of the channel is also taken into account. The insulator potential is now expressed as,

$$\psi(x,y,z)=\frac{V_g-\psi_{bi}-\Phi_{ms}}{T_{OX}}(x-\frac{W}{2})+\psi_{bi}$$

$$\text{for} \quad \frac{W}{2}<x<\frac{W}{2}+T_{OX} \text{ and } 0<y<\frac{H}{2} \quad (37)$$

$$\psi(x,y,z)=\frac{V_g-\psi_{bi}-\Phi_{ms}}{T_{OX}}(y-\frac{H}{2})+\psi_{bi}$$

$$\text{for} \quad 0<x<\frac{W}{2} \text{ and } \frac{H}{2}<y<\frac{H}{2}+T_{OX} \quad (38)$$

Here Φ_{ms} is the work function difference. By applying the superposition principle, the electrostatic potential can be now written as

$$\psi(x,y,z)=U_L(x,y,z)+U_R(x,y,z)+V_g(x,y) \quad (39)$$

Here $V_g(x, y)$ is the 1-D solution of the Poisson equation that satisfies the gate boundary conditions. U_L satisfies the source boundary condition but it is bound to have a null value on the gate and drain boundaries. Similarly U_R satisfies the drain boundary condition and it is bound to have a null value on the gate and source boundaries. On further evaluation, the term V_g+U_L is found to satisfy the potential equation when U_R is on null value and in an exact repetition the term V_g+U_R satisfies the potential equation when U_L is on null value. From Eq. (30),

$$\psi_{xx}+\psi_{yy}+\psi_{zz}=0 \quad (40)$$

By solving the above equation using LDE method we obtain the value of ψ. The Potential equation is deduced after rigorous analytical calculations as,

$$\psi(x,y,z) = V_g + (V_g - \psi_{bi})\sum_n \sum_m \rho_{nm} \sinh(\textstyle\sum_{nm}(L-z))$$
$$+(V_g - \psi_{bi} - V_{ds})\sum_n \sum_m \sinh(\textstyle\sum_{nm} z) \quad (41)$$

Where,

$$\rho_{nm}(x,y) = -\omega_{nm}\gamma_{nm}\frac{\cos(\Lambda_n x)\cos(M_{my})}{\sinh(\sum_{nm} L)} \quad (42)$$

Threshold voltage for the undoped body devices is defined as the gate voltage when the integrated charge at the virtual source becomes equal to the critical charge (Q_T). The first series term in Eq. (41) is enough to find the potential at the virtual source; it is only taken into account for the further calculations. Once the potential distribution at every point of the cross section of the channel is known we calculate the inversion charge density by using surface integral over the surface area of the channel. Hence the inversion charge can be expressed as,

$$Q = \int_{-H/2}^{H/2} \int_{-W/2}^{W/2} q n_i e^{(\psi/U_T)} dx dy \quad (43)$$

Where, q is the elementary charge, U_T is thermal voltage, and n_i is the intrinsic carrier concentration. The charge equation can now be approximated as,

$$Q \approx WHqn_i e^{\left(\frac{\psi((3W/14),(3H/14),z_c)}{U_T}\right)} \quad (44)$$

Here, z_c is the virtual source position, which is half of the channel length for low V_{ds}. Using the inversion charge we can obtain the classical threshold model as,

$$V_{TC} = \frac{U_T \ln\frac{Q}{WHqn_i} + 2V_{bi}\rho_{11}(\frac{3W}{14},\frac{3H}{14})\sinh(\frac{\sum_{11} L}{2})}{1 + 2\rho_{11}(\frac{3W}{14},\frac{3H}{14})\sinh(\frac{\sum_{11} L}{2})} \quad (45)$$

As MOSFET devices are further scaled into the deep nanometer regime, it has become necessary to include quantum mechanical effects while modeling their device behavior. The potential distribution obtained in (41) is quasi-parabolic in nature. Therefore in this paper, we approximate the actual potential as well as the square well potential since it is difficult to solve the Schrodinger equation to obtain the potential.

In the square potential well approximation, the minima of conduction band energy at the centre position is given by,

$$E_{co} = \frac{E_g}{2} - q\psi(0,0,z_c) \quad (46)$$

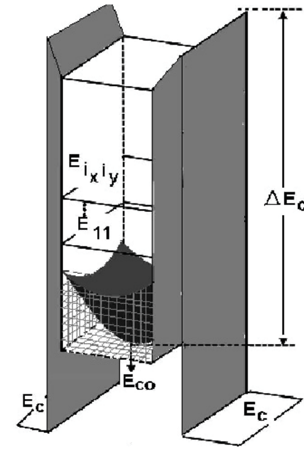

Fig. 4. Band diagram perpendicular to the gate - square well potential of a Rectangular Gate Silicon Nanowire MOSFET

Using the above value of potential energy in (46), the Schrodinger equation becomes,

$$\frac{\hbar^2}{2m_x}\frac{\partial^2\zeta}{\partial x^2} + \frac{\hbar^2}{2m_y}\frac{\partial^2\zeta}{\partial y^2} + (E - E_{co})\zeta = 0 \quad (47)$$

Here $\hbar = h/2\pi$ and h is the planks constant, ζ is the wave function and E is the energy of the electron wave. The solution for this equation is obtained by variable separation method as,

$$E_{i_x i_y} = E_{co} + \frac{\hbar^2\pi^2}{2}\left[\frac{1}{m_x}\left(\frac{i_x}{I_x}\right)^2 + \frac{1}{m_y}\left(\frac{i_y}{I_y}\right)^2\right] \quad (48)$$

The transverse and longitudinal masses and lengths in x and y directions tae different values based on the direction of quantization. The energy reaches its minimum when the masses reach the maximum value (48). In silicon, six energy valleys are found to be present in its band structure (two lower energy valleys, two middle energy valleys, and two higher energy valleys). If the thin film of device has equal height and width, the two lower energy valleys and two middle energy valleys combine together to produce four lower energy valleys and the other two higher energy valleys remain in their own state. Thus the charge per unit length per valley of silicon is expressed as,

$$Q = \sum_{i_x}\sum_{i_y} q \int_{E_{i_x i_y}}^{\infty} N1Df(E)dE \quad (49)$$

Where, N_{1D} is the 1D density-of-states and f (E) is the Fermi-Dirac distribution function. E is the energy of the electron wave. The terms i_x and i_y are positive natural numbers.

Now, the charge is given by,

$$Q = q\sum_{i_x}\sum_{i_y}\sqrt{(\frac{m_z}{2\pi\hbar^2})}\int_{E_{i_x i_y}}^{\infty}\frac{(E-E_{i_x i_y})^{\frac{-1}{2}}}{1+e((E-E_F)/kT)}dE \quad (50)$$

Where, m_z is the mass of the valley which is perpendicular to the direction of quantization. The Fermi energy level is much lower than the conduction band energy in weak inversion region. Hence the charge equation can be approximated using Boltzmann equation as,

$$Q = q\sqrt{(\frac{m_z}{2\pi\hbar^2})}\sum_{i_x}\sum_{i_y}\int_{E_{i_x i_y}}^{\infty}\frac{e^{((E_F-E)/kT)}}{(E-E_{i_x i_y})^{½}}dE \quad (51)$$

Using (48) and (51), the total integrated charge at the virtual source can be obtained as,

$$\begin{aligned} Q = q\sqrt{(\frac{2kTm_t}{\hbar^2})}\sum_{i_x}\sum_{i_y}\exp(-\frac{E_{co}+E_1(i_x,i_y)}{kT}) \\ +q\sqrt{(\frac{2kTm_t}{\hbar^2})}\sum_{i_x}\sum_{i_y}\exp(-\frac{E_{co}+E_2(i_x,i_y)}{kT}) \\ +q\sqrt{(\frac{2kTm_t}{\hbar^2})}\sum_{i_x}\sum_{i_y}\exp(-\frac{E_{co}+E_3(i_x,i_y)}{kT}) \end{aligned} \quad (52)$$

Where,

$$\begin{aligned} E_1(i_x,i_y) = \frac{\hbar^2\pi^2}{2}[\frac{1}{m_1}(\frac{i_x}{W})^2 + \frac{1}{m_t}(\frac{i_y}{H})^2 \\ E_2(i_x,i_y) = \frac{\hbar^2\pi^2}{2}[\frac{1}{m_t}(\frac{i_x}{W})^2 + \frac{1}{m_1}(\frac{i_y}{H})^2] \\ E_3(i_x,i_y) = \frac{\hbar^2\pi^2}{2}[\frac{1}{m_t}(\frac{i_x}{W})^2 + \frac{1}{m_t}(\frac{i_y}{H})^2] \end{aligned} \quad (53)$$

Here the m_t and m_1 are the transverse and longitudinal effective masses of the energy valleys of silicon. The lengths i_x and i_y carry distinct values contingent on the direction of quantization. Finally, the quantum threshold voltage model becomes,

$$V_{TQ} = \frac{\frac{E_g}{2q} + (\frac{kT}{q})In(\frac{Q_T}{\tau}) + 2\psi_{bi}\rho_{11}(0,0)\sinh(\frac{\sum_{11}L}{2})}{1+2\rho_{11}(0,0)\sinh(\frac{\sum_{11}L}{2})} \quad (54)$$

Where,

$$\begin{aligned} \tau = q\sqrt{(\frac{2kTm_t}{\hbar^2})}\exp(-\frac{E_1(1,1)}{kT}) \\ +q\sqrt{(\frac{2kTm_t}{\hbar^2})}\exp(-\frac{E_2(1,1)}{kT}) \\ +q\sqrt{(\frac{2kTm_t}{\hbar^2})}\exp(-\frac{E_3(1,1)}{kT}) \end{aligned} \quad (55)$$

The impacts on the threshold voltage due to quantum effects is acquired by using the following equation,

$$V_{TC} = V_{TQ} + \Delta V_T \quad (56)$$

Here, ΔV_T is the difference between the quantum threshold voltage and the classical threshold voltage.

4. Results and Discussions

The Junction Based Cylindrical Surrounding Gate Transistor is simulated with the following specifications for the device: V_{ds}= 0.1 V, N_A=1x10^{17}cm^{-3} and N_D=1x10^{19} cm^{-3} are the drain voltage, doped p-type silicon film and the high n-type doping densities, respectively. The model simulations are validated by comparing the MATLAB simulation results with the results of the TCAD simulations.

Fig. 5 shows the relation between the threshold voltage roll-off and effective channel length for varying oxide thicknesses of a cylindrical surrounding gate device. Three different oxide thicknesses of 1, 3 and 5 nm are used. The thinnest gate oxide thickness of 1 nm shows the minimum threshold voltage degradation. As the gate oxide thickness increases, the threshold voltage roll-off also increases leading to the subdued performance of the device. The threshold voltage tends to remain constant in a range of 0.4V with the effective channel length of 35nm.

Fig. 6. shows the variation of the threshold voltage roll-off versus effective channel length for different silicon film thicknesses of a cylindrical surrounding gate device. Decreasing the effective channel length shows that the threshold voltage roll-off of the device is highly increased.

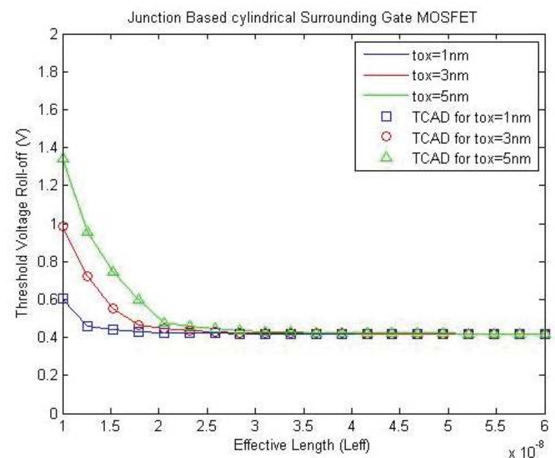

Fig.5. Threshold voltage roll-off versus effective channel length for a Junction Based Cylindrical Surrounding Gate Nanowire Transistor with different oxide thicknesses

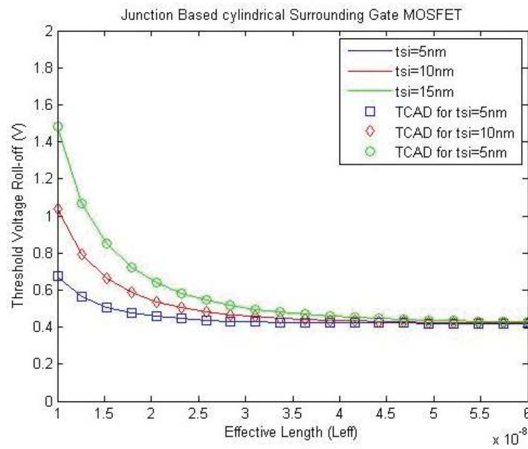

Fig. 6. Threshold voltage roll-off versus effective channel length for a Junction Based Cylindrical Surrounding Gate Nanowire Transistor with different silicon thicknesses

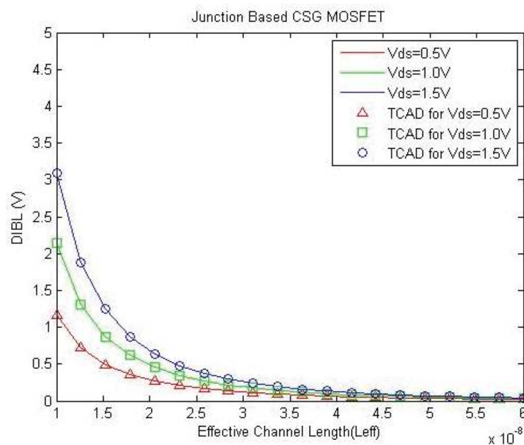

Fig. 7. DIBL versus effective channel length for a Junction Based Cylindrical Surrounding Gate Transistor

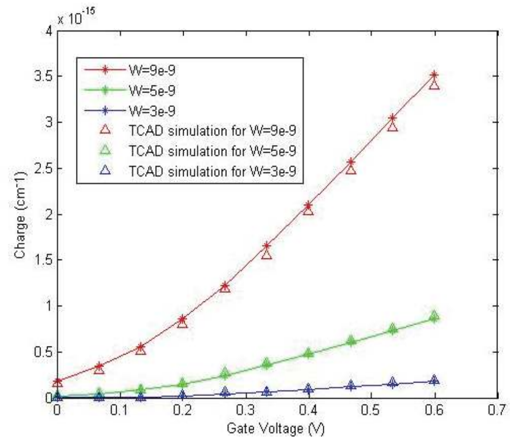

Fig. 8. Variation of quantum integrated charge at virtual source with gate voltage for a Rectangular Surrounding Gate Nanowire Transistor with different film widths

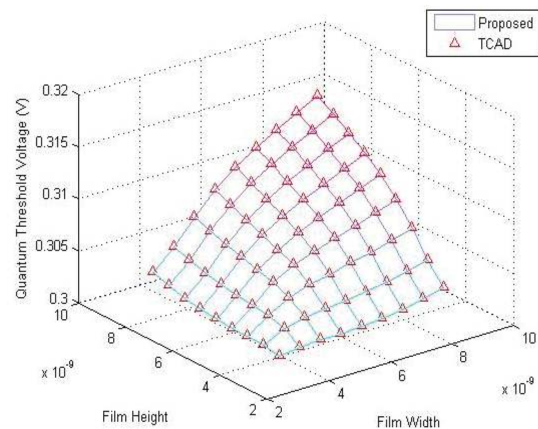

Fig. 9. Variation of quantum threshold voltage with film height and width for a Rectangular Surrounding Gate Nanowire Transistor (L=20nm)

Three different silicon thicknesses of t_{si} = 5, 10, and 15 nm are used in the simulations. Reducing thickness of the silicon film leads to the reduction of threshold voltage. As the thickness is less than 10 nm, the device tends to show abnormal variations in terms of threshold voltage. The simulations are further compared with TCAD simulations and are found to be in excellent coordination.

Any transistor whose channel length is reduced to a nanometer range, there enters the problem of short channel effects (SCE). DIBL (Drain Induced Barrier Lowering) is one among these SCE that affects the performance of the transistor. Fig. 7. shows the impact of the effective channel length on DIBL for different drain biases of a cylindrical surrounding gate device.

In Fig. 7, the minimum V_{ds} is kept as 0.1V and as they are gradually increased to higher values of 0.5, 1.0 and 1.5 V, the DIBL is plotted as the difference between the lower and higher bias values. It shows that an increasing drain bias and decreasing effective channel length will lead to the device suffering high Short Channel Effects.

Fig. 8. represents the variation of total quantum integrated charge of a rectangular surrounding gate device with the gate voltage at 0.3V for different film widths. Eq. (45) is used to obtain the integrated charge with only one energy level and one series term. It clearly shows that the decrease in the film thickness leads to the increase in the quantum threshold voltage which is actually due to the increase in energy quantization of the transistor.

Fig. 9 shows the variation of quantum threshold voltage with width and height of the film for a rectangular surrounding gate device at a channel length of 20 nm. The impact of the device dimensions like film height and width on the quantum threshold voltage of the device is explained. The short channel effects tend to decrease along with the energy quantization and this can be further explained as a result of increase in the effective band gap of silicon due to quantum effects. The effect of confinement, expressed as the difference in the threshold voltage and its variation with the channel length L, of a Rectangular surrounding gate device is illustrated in Fig. 10. The most important

thing about this gate all around nanowire transistor is that any change in one of the dimensions can be nullified by proper tuning of other dimensions as the transistor is symmetric about its height and width.

Fig. 11 shows the variation of the classical threshold voltage and quantum threshold voltage with the film height of a Rectangular surrounding gate device at a constant width of 9 nm. The value of the classical threshold voltage ranges from 0.27 V to 0.29 V for the corresponding changes in the film height. Similarly the quantum threshold voltage ranges from 0.3 V to 0.31 V. It shows that the device has a highly improved control over the threshold voltage. The process parameters are almost same for the cylindrical gate and surrounding gate devices except for the fact that radius is the main factor in the cylindrical gate device while width plays a very important role in the rectangular gate device.

As the thickness of the silicon film increases and the effective channel length decreases, threshold voltage roll-off increases in a cylindrical gate device. Similarly as the film width increases, the threshold voltage decreases in a rectangular gate device. This will lead to simultaneous increase in the off current, resulting in the performance degradation of device. In the cylindrical gate device, increase in gate oxide thickness and reduction in effective channel length leads to higher threshold voltage roll-off. In a rectangular gate device, as the film height increases and the channel length decreases, threshold voltage also decreases but the short channel effects are reduced due to energy quantization. The increase in drain bias and reducing channel length is bound to increase the short channel effects in both geometries. The major difference between the two geometries is that the rectangular gate device is bound to get affected by corner effects much more in comparison with the cylindrical gate device.

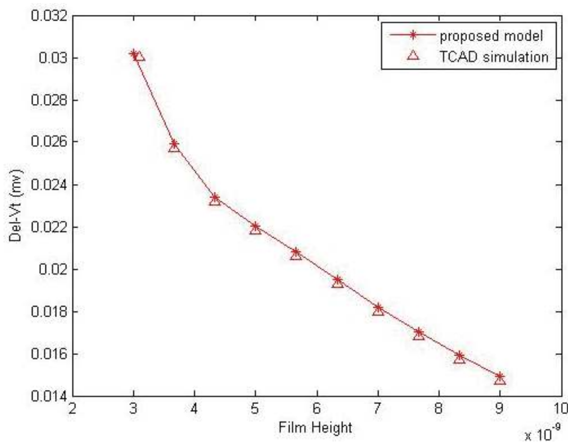

Fig. 10. Variation of threshold voltage with film height for a Rectangular Surrounding Gate Nanowire Transistor (L= 20nm and W=9nm)

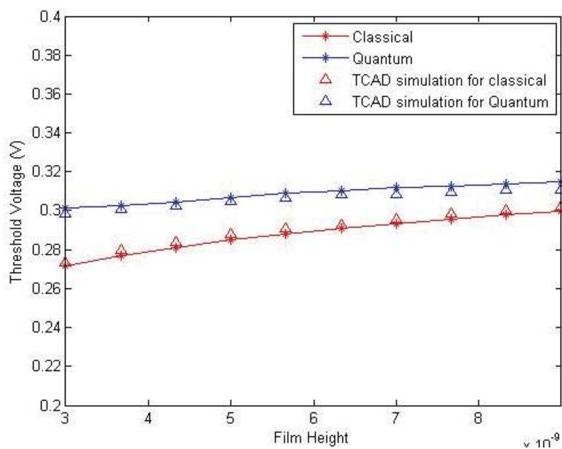

Fig. 11. Variation of quantum and classical threshold voltage with film height for a Rectangular Surrounding Gate Nanowire Transistor. Here L=20nm and W=9nm.

5. Conclusion

A new physically based threshold voltage models for a Junction Based Cylindrical Surrounding Gate Nanowire Transistor and Rectangular Gate Surrounding Gate Nanowire Transistor have been developed. The simulations are validated by using the TCAD results. This physics based models can be extended to study the I-V characteristics of the devices affording to their simplicity and computational efficiency.

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