Analytical Transient Response and Propagation Delay Model for Nanoscale CMOS Inverters

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Abstract–**This paper presents a new analytical propagation delay model for a nanoscale CMOS inverter. By using a non-saturation current model, the analytical input-output transfer responses and propagation delay model are derived. The model is used for calculating inverter delays with different input transition times, load capacitances and supply voltages. Delays predicted by proposed model are in good agreement with that of transistor level simulation results from SPICE, and errors are less than 3%.**

I. INTRODUCTION

As one of the most important performance parameters in CMOS digital circuits, the propagation delay is of concern to designers and users. A circuit's speed/frequency and dynamic power dissipation are both affected significantly by propagation delay, and hence timing analysis has been investigated for several decades [1-7]. With the increasing complexity of modern very large scale integration (VLSI) systems, transistor level simulation consumes much more computation time because of the nonlinear transfer characteristics of CMOS gates [8-10]. Therefore, an analytical delay model that does not need numerical iterations is needed to extract delay efficiently, and much work has been published on the topic [3, 6-19].

For extracting the propagation delay, development of a delay model for a CMOS inverter is considered as the first step [14], and a number of inverter delay models have been developed [6-15]. The first inverter delay expression was introduced by Burns [1]. Early models were based on Shockley's square law MOSFET model which does not include the carrier velocity saturation effect [1, 2]. As the drain current (I_{ds}) deviates significantly from the Shockley model in the submicron region, Sakurai et al. [3] proposed a model using an α-power law current model which includes the carrier velocity saturation effect of short channel devices. Several analytical delay expressions based on the α-power law model were introduced thereafter [10, 13]. However, in modern small dimension MOSFETs, I_{ds} does not show saturation [20-22]. Therefore, α-power law based delay models would underestimate inverter propagation delay by using higher I_{ds} (at V_{ds}=V_{dd}) as the saturation current in the nominal saturation region.

On the other hand, some delay models did not take the current through the loading transistor into account [3, 13], including both the overshooting and short-circuit current [10, 14, 23]. Moreover, with continuous scaling down of transistor dimensions, the charging/discharging of input-output coupling capacitance (C_M) inevitably affects inverter characteristics and propagation delays, which should be considered in developing delay models [7, 8, 10, 12, 14, 16, 23].

The reported propagation delay expressions for a submicron inverter are complex [8-10, 14], which limits the extensive use of them. The objective of this work is to develop a new analytical propagation delay model for a Nanoscale CMOS inverter. A non-saturation I_{ds} model for a MOSFET is proposed, and the effects of I_{ov} and C_M are considered. The analytical expression of the output response is derived by solving differential equations in each transition region, giving the propagation delay of a CMOS inverter.

II. NON-SATURATION DRAIN CURRENT MODEL AND INVERTER TRANSIENT RESPONSE

A. PROPOSED DRAIN CURRENT MODEL FOR NANO MOSFETS

The MOSFET output characteristics are simulated in SPICE using the BSIM4 model. The model parameters were extracted from 35nm technology bulk devices with an oxide thickness of 0.86nm. Fig. 1(a) shows the output characteristics of an n-MOSFET with both width and length of 35 nm; I_{ds} predicted by an α-power law model is also shown. The non-saturation phenomena and obvious discrepancy between the α-power law and simulation are observed.

It is seen that I_{ds} shows piecewise linearity versus V_{ds}, the first segment corresponds to the triode region and the second is observed before the substrate current induced body effect takes effect. Linear fitting to the second segment is shown in Fig. 1(a), and linear equations are used in describing the driving current of dynamic inverter behaviour.

During a rising input transient, V_{ds} (=V_{out}) of the driving n-MOSFETs varies with gate voltage (V_{gs}=V_{in}), so I_{ds} lies on different lines in Fig. 1(a). To obtain I_{ds} at any transition point, linear equations for the second region at any V_{gs} should be known, which can be derived by the two-point method. For example, two simulated or measured points are taken to achieve the objective at V_{gs}=V_{dd}, one is I_{ds0} (I_{ds} at V_{gs}=V_{ds}=V_{dd}), and the other is chosen at the near transition point of I_{ds}–V_{ds} such as I'_{ds0} (I_{ds} at V_{gs}=2V_{ds}=V_{dd}). For the case of V_{gs} being less than V_{dd}, the two points can be estimated by the α-power law as illustrated in Fig. 1(b).

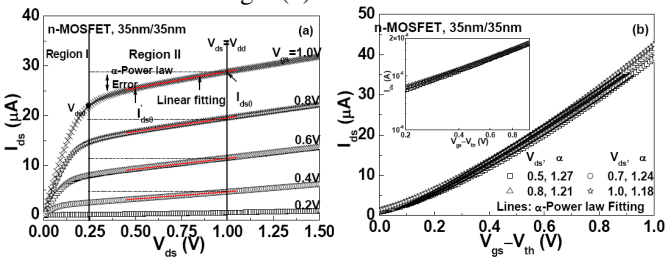

Fig. 1. Simulated output characteristics of n-MOSFET, linear fitting of I_{ds} from V_{ds}=0.5V_{dd} to V_{dd} are shown (a). α-power fitting of I_{ds}~(V_{gs}–V_{th}), inset is log–log plot of the same group data, α~1.2 for Nano MOSFETs (b).

It is found that I_{ds} is proportional to $(V_{gs}-V_{th})^{\alpha}$ from Fig. 1(b), where α is about 1.2 (which is reasonable for submicron devices [3]). Therefore, I_{ds} in region II of Fig. 1(a) can be expressed as follows:

$$I_{ds}=I_{ds0}\left(\frac{V_{gs}-V_{th}}{V_{dd}-V_{th}}\right)^{\alpha}+2\left(I_{ds0}-I_{ds0}^{'}\right)\left(\frac{V_{gs}-V_{th}}{V_{dd}-V_{th}}\right)^{\alpha}\frac{V_{ds}-V_{dd}}{V_{dd}} \quad (1)$$

V_{th} is the threshold voltage, α is the fitting parameter reflecting velocity saturation effects. Eq. (1) will be used in deriving the inverter analytical propagation delay model.

B. CMOS INVERTER SWITCHING CHARACTERISTICS ANALYSIS

The schematic of a CMOS inverter is shown in Fig. 2(a). The ratio of the channel widths (W) between p-MOSFET and n-MOSFET is set at 1.74. C_L includes output capacitance and load capacitance, C_M is input-to-output coupling capacitance which is given as follows:

$$C_M=C_{ox}\left(\frac{W_{peff}L_{peff}}{2}+L_{Dp}W_{peff}+L_{Dn}W_{neff}\right), \quad (2)$$

where W_{peff} and W_{neff} are the effective channel widths of the p-MOSFET and n-MOSFET, respectively. L_{peff} is the effective channel length of the p-MOSFET; L_{Dp} and L_{Dn} are the gate-drain under-diffusion of p-MOSFET and n-MOSFET.

The dynamic behaviour of the inverter can be derived from Kirchhoff's current law at the output node:

$$C_L\frac{dV_{out}}{dt}=C_M\frac{d\left(V_{in}-V_{out}\right)}{dt}+I_p-I_n, \quad (3)$$

where V_{out} and V_{in} are the output and input voltages, I_p and I_n are the I_{ds} values of the p-MOSFET and n-MOSFET, respectively. In this work, the differential equation is solved for a rising input where the n-MOSFET is the driving transistor and the p-MOSFET is the loading transistor. The rising input signal is expressed as:

$V_{in}=0$ at $t\le 0$, $V_{in}=V_{dd}\times t/tr$ for $0\le t\le tr$ and $V_{in}=V_{dd}$ at $t\ge tr$,

where tr is the riseime. Therefore, the propagation delay, $tpHL$ (high to low) which is the time interval from $V_{in}=50\%V_{dd}$ to $V_{out}=50\%V_{dd}$ will be derived.

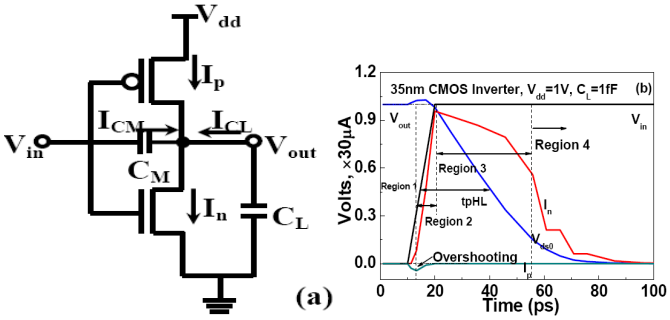

Fig. 2. (a) A CMOS inverter discharging model, (b) input-output voltage and current evolution for a linear rising input signal, inverter operation regions and $tpHL$ definition are shown.

Fig. 2(b) shows both the input-output relation and I_p and I_n for a rising input case. I_p is negative at the beginning of the transition because of overshooting [10, 14]. The overshooting time (t_{ov}) cannot be ignored in nanoscale digital circuits [23]. I_p becomes positive after n-MOSFET turns on, which called the short-circuit current but it is ignored for fast input ramps.

For a fast rising input ramp, the trajectory of V_{out} is shown by arrowed lines in Fig. 3. The driving current (I_n) is estimated as follows:

Region 1, $I_n\approx I_{subn}$, $0\le t\le V_{thn}\times tr/V_{dd}$, $0\le V_{in}\le V_{thn}$, cut-off and subthreshold region.

Region 2, $I_n=I_{ds0}\left(\frac{V_{gs}-V_{th}}{V_{dd}-V_{th}}\right)^{\alpha}$, $V_{thn}\times tr/V_{dd}\le t\le tr$, $V_{thn}\le V_{in}\le V_{dd}$, Region II in Fig. 1(a) at $V_{ds}=V_{dd}$.

Region 3, $I_n=I_{ds0}+2\left(I_{ds0}-I_{ds0}^{'}\right)\frac{V_{ds}-V_{dd}}{V_{dd}}$ $t\ge tr$, Region II in Fig. 1(a) at $V_{gs}=V_{dd}$ and $V_{ds}\ge V_{ds0}$.

Region 4, $I_n=\beta\left(V_{dd}-V_{th}-\frac{1}{2}V_{ds}\right)V_{ds}$, $t\ge tr$, Region I in Fig. 1(a) at $V_{gs}=V_{dd}$ and $V_{ds}\le V_{ds0}$.

where I_{subn} is the subthreshold current, $V_{gsn}=V_{in}$, $V_{dsn}=V_{out}$, $\beta=W_n\mu_eC_{oxn}/L_n$ and μ_e is the electron mobility.

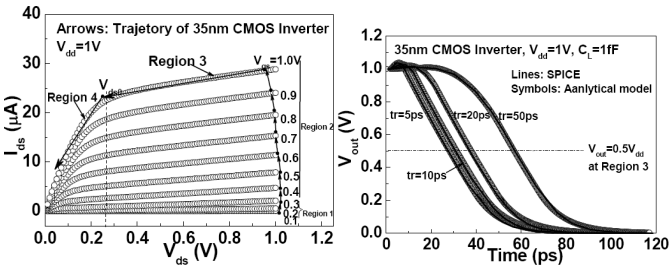

Fig. 3. Trajectory of V_{out} at rising input ramp, the operation regions are corresponding to that of Fig. 2(b)'s.

Fig. 4. Comparison of V_{out} between predictions of the model and transistor level simulations of SPICE, with input rising time increases from 5ps to 50ps.

III. ANALYTICAL INVERTER TRANSIENT RESPONSE ANALYSIS AND PROPAGATION DELAY

A. ANALYTICAL SOLUTIONS OF INVERTER TRANSIENT RESPONSE

By connecting the switching behavioural of CMOS inverter in Fig. 2(b) and the suggested driving current model, corresponding forms of Eq. (3) can be rewritten and solved as follows.

Region 1: $0\le t\le V_{thn}\times tr/V_{dd}$, $0\le V_{in}\le V_{thn}$

The n-MOSFET operates in the subthreshold region and the p-MOSFET in the linear region with $V_{dsp}>0$ because of effects of the gate-to-drain coupling capacitance. Since expressions of the overshooting and subthreshold current are complex, one cannot solve analytically the differential equation for this region. So the average value of I_{subn} (at $V_{in}=V_{thn}/2$) is used to substitute for I_n and I_p. Therefore, Eq. (3) is:

$$C\frac{dV_{out}}{dt}=C_M\frac{dV_{in}}{dt}-2I_{subn}=C_M\frac{V_{dd}}{tr}-2I_{subn} \quad (4)$$

where $C=C_L+C_M$, considering the boundary condition of $V_{out}=V_{dd}$ at $t=0$,

$$V_{out1}=\left(\frac{C_MV_{dd}}{Ctr}-\frac{2I_{subn}}{C}\right)t+V_{dd} \quad (5)$$

Region 2, $V_{thn}\times tr/V_{dd}\le t\le tr$, $V_{thn}\le V_{in}\le V_{dd}$

The n-MOSFET switches on and V_{dsn} (V_{out}) stays at almost V_{dd} for fast input ramps cases, I_n is calculated by α-power law. p-MOSFET current equals approximately to zero because V_{dsp} is almost zero. The differential equation is:

$$C\frac{dV_{out}}{dt}=C_M\frac{V_{dd}}{tr}-I_{ds0}\left(\frac{V_{in}-V_{thn}}{V_{dd}-V_{thn}}\right)^{\alpha} \quad (6)$$

The solution is obtained by using the boundary condition of V_{out2} ($t=V_{thn}\times tr/V_{dd}$)$=V_{out1}$ ($t=V_{thn}\times tr/V_{dd}$):

$$V_{out2}=\frac{\left(t/tr-V_{thn}\right)^{\alpha+1}}{\left(V_{dd}-V_{thn}\right)^{\alpha}}\left(\frac{tr}{C(\alpha+1)}\right)+\frac{C_MV_{dd}t}{Ctr}+V_{dd}-\frac{2V_{thn}I_{subn}}{C}tr \quad (7)$$

Region 3, t≥tr, $V_{in}=V_{dd}$ and $V_{out}\geq V_{ds0}$.

The n-MOSFET operates in linear region II, $V_{gsn}=V_{in}=V_{dd}$. p-MOSFET turns off. The dynamic behaviour is described by:

$$C\frac{dV_{out}}{dt}=-I_{ds0}-2\left(I_{ds0}-I_{ds0}^{'}\right)\frac{V_{out}-V_{dd}}{V_{dd}} \tag{8}$$

The above first order differential equation can be solved analytically with $V_{out3}=V_{out2}$ at $t=tr$.

$$V_{out3}=A_1+\left(A_2-A_3-A_1\right)e^{A_4(t-tr)} \tag{9}$$

where $A_1=\frac{2I_{ds0}^{'}-I_{ds0}}{2(I_{ds0}^{'}-I_{ds0})}V_{dd}$, $A_2=\left(1+\frac{C_M}{C}\right)V_{dd}-\frac{2I_{subn}V_{thn}}{CV_{dd}}tr$,

$A_3=\frac{I_{ds0}(V_{dd}-V_{thn})}{CV_{dd}(\alpha+1)}tr$, $A_4=\frac{2(I_{ds0}^{'}-I_{ds0})}{CV_{dd}}$

Region 4, t≥tr, $V_{in}=V_{dd}$ and $V_{out}\leq V_{ds0}$.

The n-MOSFET operates in the linear region I of Fig. 1(a), $V_{gsn}=V_{in}=V_{dd}$ and p-MOSFET is off.

$$C\frac{dV_{out}}{dt}=-\beta\left(V_{dd}-V_{th}-\frac{1}{2}V_{ds}\right)V_{ds} \tag{10}$$

The equation can be simplified by neglecting the second order term. By continuity conditions,

$$V_{out4}=V_{ds0}\exp(-Bt_0)\exp(Bt) \tag{11}$$

$B=\beta(V_{th}-V_{dd})/C$, t_0 is calculated from Eq. (9) at $V_{out3}=V_{ds0}$.

B. INVERTER PROPAGATION DELAY EVALUATION

The high-to-low propagation delay (*tpHL*) is calculated by:

$$tpHL=t_{V_{out}=50\%V_{dd}}-0.5tr \tag{12}$$

The $50\%V_{dd}$ level of V_{out} always occurs in region 3 for fast input ramp cases, and *tpHL* is derived from Eq. (9),

$$tpHL=\frac{1}{A_4}\ln\left(\frac{0.5V_{dd}-A_1}{A_2-A_3-A_1}\right)+\frac{1}{2}tr \tag{13}$$

For very slow input transitions, $V_{out}=0.5V_{dd}$ would occur in region 2, *tpHL* can be obtained from Eq. (7). The parameters in the *tpHL* formula can be obtained from either simulation or measurement. Both the overshoot current of the p-MOSFET and subthreshold current of the n-MOSFET are taken into account. The non-saturating driving current is considered for nano MOSFETs, which reduces the delay errors compared with models using a saturated driving current [3, 10, 13].

IV. RESULTS AND DISCUSSIONS

In this section, V_{out} and *tpHL* calculated by the proposed model are compared with those obtained from SPICE. The physical and electrical parameters of both transistors are listed in table I.

Table. I. MOSFET PHYSICAL AND ELECTRICAL PARAMETERS USED IN CALCULATIONS OF PROPAGATION DELAY

Device	L(nm)	W(nm)	I_{ds0} ($V_{gs}=V_{ds}=1$)	I'_{ds0} ($V_{gs}=2V_{ds}=1$)
n-MOS	**35**	**35**	**28.84μA**	**25.46μA**
P-MOS	35	61	28.84μA	25.46μA
$I_{sub(ave)}$	V_{th} (V)	α	C_{ox} (F)	C_{gdo} (F)
0.54μA	**0.26148**	**1.2**	**0.0492f**	**0.0216f**
0.54μA	-0.26148	1.2	0.0857f	0.0376f

Fig. 4 is a comparison of V_{out} from calculation and simulation. V_{dd} and C_L are 1V and 1fF, respectively, with input rising time varying from 5ps to 50ps. It is shown that the proposed model results are very close to that produced by SPICE, which means the approximation of the currents and the derivation is good.

Fig. 5 shows *tpHL* at different *tr* (≤50ps) with V_{dd}=1V and C_L=1fF. The input transition time has little effect on the currents (I_{ov}, I_{subn} and I_{dsn} at $V_{gsn}=V_{dd}$), and *tpHL* is calculated by using the parameters in Table I. Simulated *tpHL* is plotted for comparison; it is observed that the two set of results are close to each other with an average error of about 1.43%. The calculated *tpHL* from the analytical model of Ref. [3] is also given, from which significant deviations from the simulated results are observed. Inaccuracies of reported models may result from ignoring I_{ov}, I_{sub} and the coupling capacitance, as well as from using a constant driving current.

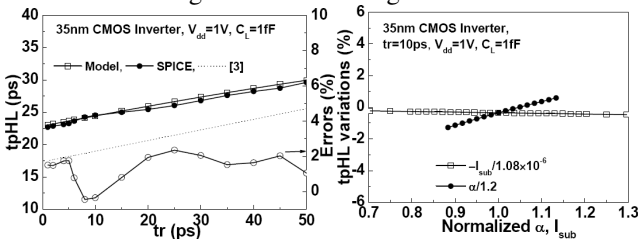

Fig. 5. *tpHL* calculated by proposed analytical model are compared with that simulated by SPICE with *tr* varying, the average error is acceptable. *tpHL* predicted by previous model are also plotted for comparison.

Fig. 6. The calculated *tpHL* are not affected significantly by variations of delay model parameters of I_{sub} and α.

It is noticed that variations of average $I_{sub(ave)}$ do not give the variation of *tpHL* shown in Fig. 6. One of the reasons is the active time of I_{ov} and I_{sub} is shorter during switching. On the other hand, the range of α in Fig. 1(b) does not result in significant fluctuations of *tpHL*. Therefore, the usability of proposed model is increased.

Fig. 7 shows *tpHL* as a function of C_L at V_{dd}=1V and *tr*=10ps. C_L affect I_{ov} but its effects on the driving current is negligible. The discrepancies between the proposed analytical model and simulation results are negligible, with errors within 3%. Application of this analytical model on different C_L is useful for extending its use in more complex digital circuits by the "collapsing" technique, which reduces gates to equivalent inverters [16].

V_{dd} decreases continuously with MOSFET dimension scaling. Lower V_{dd} has the advantages of lowering power dissipation and reducing high electric field effects. However, CMOS intrinsic delay increases rapidly with V_{dd} decreasing if V_{th} does not reduce in proportion to V_{dd}, which is mainly due to the loss of large-signal transcondutance (I_{ds}/V_{dd}) [24]. The adverse effects are alleviated to some extent by lowering V_{th}. Nevertheless, V_{th} cannot be always reduced in proportion to V_{dd} in view of subthreshold current (and hence the power) as well as gate oxide electric field. Therefore, delays increase at lower V_{dd}.

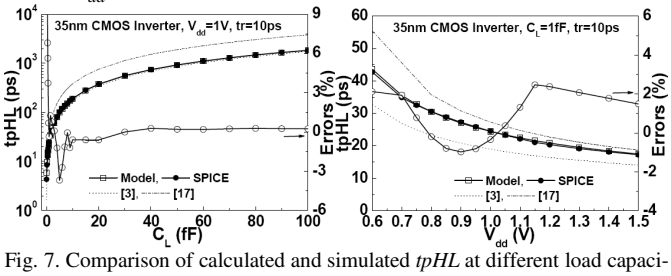

Fig. 7. Comparison of calculated and simulated *tpHL* at different load capacitance, the average error is about 1.08%. Delays calculated by previous models are also shown.

Fig. 8. The proposed inverter propagation delay model can be used at relative larger range of V_{dd}, with errors from SPICE simulation are not more than 2.5%. The predictions of previous analytical models are shown for comparison.

Fig. 8 shows SPICE simulations and model predictions of *tpHL* versus V_{dd} at *tr*=10ps and C_L=1fF. The errors are

smaller than 2.5% when V_{dd} is in the range 0.6 to 1.5V, which confirms the validity of the proposed analytical model. It should be pointed that I_{ds0} and I'_{ds0} are different from the values of Table I when V_{dd} is not equal to 1.0V, and the currents are simulated at $V_{gs}=V_{ds}=V_{dd}$ and $V_{gs}=2V_{ds}=V_{dd}$, respectively.

tpHL calculated by reported analytical models are compared for different cases in Figs. 5, 7 and 8. As analysed above, α-power law based models [3, 10, 13] use I_{ds0} as the saturation current, which is larger than the actual driving current and they underestimate *tpHL*. On the contrary, the model of [17] takes the inverter switching trajectory from $V_{ds}=V_{dd}=2V_{gs}$ ($I_{ds}=I_L$) to $V_{gs}=2V_{ds}=V_{dd}$ ($I_{ds}=I_H$) which is not suitable for a nano inverter. The method of taking half the sum of I_H and I_L as the effective current in [17] underestimates the driving current and predicts higher delays. To the best of our knowledge, the analytical delay expression presented in this work has the advantages of simple, accurate and operable for Nanoscale CMOS digital circuits compared with the reported models.

V. CONCLUSIONS

For nanoscale MOS transistors, the drain current in the saturation region does not show saturation characteristics any more. Therefore, reported propagation delay models, such as the series of α-power models, underestimate the delays of nano CMOS inverters. This paper developed an analytical propagation delay model based on a 35nm technology CMOS inverter. The effects of non-saturation current, input-to-output coupling capacitance, overshooting current and subthrehsold current are considered in proposed model.

The input waveform slope, load capacitance and supply voltage significantly affect inverter delay, which is predicted by the presented model. The accuracy and validity of the model is verified by comparing with transistor level simulation results of SPICE, with acceptable errors (less than 3%) at large ranges of input transition times, load capacitances and supply voltages.

We presented accurate and direct analytical expressions of output transient response and propagation delays for a nanoscale CMOS inverter. By simplifying more complex digital gate circuits to an equivalent inverter, this model will be valuable in supplying accurate and fast estimated delays for designers.

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