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Analysis of Reverse Feedback Distributed Oscillators with m-derived Artificial Transmission Lines

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Abstract — This paper presents a linear analysis of the reverse feedback distributed oscillator, which is a wideband voltage controlled oscillator proposed by Skvor, *et al.* [1] based on the distributed amplifier. The theoretical analysis presented in [1] was generalized for a distributed oscillator employing m-derived artificial transmission lines. The resulting equations allow predicting the circuit oscillation frequency behavior and the corresponding required minimum transistor transconductances. A design example is described for a three-octave oscillator.

Index Terms — Distributed amplifier, microwave integrated circuits, microwave FET oscillators, MMIC oscillators, tunable oscillators.

I. INTRODUCTION

Demand for microwave wideband circuits has been increasing over the last years. However, commercial VCO's have tuning range limited by about one octave [2].

In order to achieve wideband tuning range, Skvor et al. [1] proposed in 1992, an oscillator topology based on the reverse feeding back of the distributed amplifier. Such topology was implemented as a 4 GHz hybrid circuit [2], using pHEMT transistors, but it is also suitable to be implemented in MMIC technology in order to achieve higher operation frequencies.

Linear analysis proposed in [1]-[2] for the reverse feedback distributed voltage controlled oscillator – DVCO, considered k-constant artificial lines that are a special case of m-derived artificial lines. This paper generalizes that analysis by using m-derived artificial lines. It allows a more realistic modeling of the DVCO, since inductive parasitics at transistor ports may be taken into account. Based on this general analysis, a three-octave tunable reverse feedback DVCO design is presented.

II. DISTRIBUTED AMPLIFIER

The distributed amplifier is a wideband topology based on two artificial transmission lines coupled through active devices periodically distributed [3]. When using field effect transistors – FETs, as active devices, the artificial transmission lines are called gate and drain lines. The basic topology of the distributed amplifier is presented in Fig.1:



Fig. 1. Schematic of an n-stage distributed amplifier.

Input signal propagates along the gate line and dissipates on the termination resistor, Rg. That way, signal drives all transistor gates and is amplified to the drain line along which it propagates in both directions.

Design rules impose that the propagation velocity of drain and gate lines, as well as electric distance between transistors are identical. Thus, the contribution of the transistors adds in phase at the output. On the other hand, drain line reverse traveling waves from each transistor are added out of phase, and any remaining energy is dissipated in the drain line termination resistor, *Rd*.

The input and output shunt capacitances of the transistor parasitics form an integral part of the transmission lines. Hence, these capacitances do not limit the gain-bandwidth product of the distributed amplifier as in a traditional amplifier; witch allows larger bandwidths to be achieved.

III. REVERSE FEEDBACK DVCO

The basic topology of the reverse feedback DVCO is presented in Fig. 2. It is obtained by taking off the drain termination resistor Rd of the distributed amplifier (Fig. 1) and feeding back to the input port the signal that propagates in the reverse direction [1].



Fig. 2. Schematic of an n-stage reverse feedback DVCO.

Reverse feedback DVCO operates with just a pair of transistors independently biased in the active region, so that its reverse gain is high enough to build up oscillation. Each transistor pair is responsible for tuning a frequency interval, by complementary sweeping the gate-source bias voltage of the active transistor pair, from saturation to cut-off. A crossed transistor, named *T12*, must be introduced to guarantee oscillation phase condition in over the entire band.



Fig. 3. Lossless model of DVCO with m-derived artificial transmission lines.

Fig. 3 shows the schematic circuit of an *n*-stage DVCO whose gate and drain lines are lossless mderived artificial transmission lines and FETs are represented by their lossless unilateral model [4]. Transistor T12 is not considered in this point of the analysis, but it will be taken in to account later on. Cg and Cd are gate and drain FET capacitances, respectively. Lpg and Lpd represent the parasitic inductances of gate and drain ports, added to inductive effect of short microstriplines connected to them.

IV. M-DERIVED ARTIFICIAL TRANSMISSION LINES

Artificial transmission lines are a cascade of identical two-port networks made of lumped components. They are normally characterized by network theory [5] in terms of image impedances Z_i and propagation factor θ . For a reciprocal symmetric two-port network, Z_i is defined as the impedance towards each port, when the other is also terminated by Z_i . Propagation factor θ is a complex number, whose real part θ_r defines network losses, and imaginary part θ_i defines phase shift.

Low pass k-constant artificial transmission line is the lumped version of the uniform lossless transmission line model. It can be composed by cascading low-pass *LC* T-sections (Fig. 4a). Its image impedance is Z_T , and its cut-off frequency is given by

$$\omega_c = \frac{2}{\sqrt{LC}} \,. \tag{1}$$

This topology can be modified to the structure known as m-derived artificial transmission line (Fig. 4b), where the series inductance and parallel capacitance are multiplied by a positive *m* factor smaller or equal to 1, and an additional inductor Lp is connected in series with capacitor mC/2. If m=1, the m-derived structure is reduced to the k-constant structure.



Fig. 4. Low-pass T-sections: (a) k-constant; (b) m-derived.

The cut-off frequency of m-derived structure is also determined by (1) and m-derived T-section image impedance Z_{Tm} is calculated by:

$$Z_{Tm} = \sqrt{1 - \frac{\omega^2}{\omega_c^2}} \sqrt{\frac{L}{C}} . \qquad (2)$$

In order to avoid signal reflection at the ends of artificial transmission lines, their frequency dependent image impedance must be matched to the system reference impedance, usually $Z_0=50 \ \Omega$ at microwave frequencies.

At low frequencies, the impedance matching is obtained by a proper choice of L and C values, so that:

$$Z_{Tm} \cong \sqrt{\frac{L}{C}} = Z_0 \quad , \quad \omega << \omega_c \,. \tag{3}$$

The desired impedance matching may be extended to frequencies close to ω_c , by using mderived half section networks with m=0.6 [3] to transform the image impedance of the artificial transmission line to the system reference impedance Z_0 , as shown in Fig. 5a.



Fig. 5. Low pass m-derived sections: (a) half section; (b) π -section.

Low pass m-derived π -section can be obtained by associating two half sections back to back, in a manner that the shunt arms are kept at the edges (Fig. 5b). Its cut-off frequency is also ω_c , and its image impedance $Z\pi$ m is calculated by:

$$Z_{\pi m} = \frac{1 - \frac{\omega^2}{\omega_c^2} (1 - m^2)}{\sqrt{1 - \frac{\omega^2}{\omega_c^2}}} \sqrt{\frac{L}{C}} \,. \tag{4}$$

Low pass m-derived propagation factor θ_m has the same value for π and T sections. It varies from purely imaginary at lower frequencies to purely real at ω_c . Its imaginary part θ_{mi} in pass-band can be obtained from [6] as

$$\theta_{mi} = 2 \cdot \arcsin\left(\frac{\omega}{\omega_c} \cdot \sqrt{\frac{m^2}{1 - \frac{\omega^2}{\omega_c^2}(1 - m^2)}}\right) \quad , \quad \omega < \omega_c \quad .$$
(5)

V. DVCO MODEL

A simplified linear model for the *n*-stage reverse feedback DVCO [1] without the crossed transistor

T12 is presented in Fig. 6. It is supposed that drain and gate line sections are equalized by external components to achieve the same phase shift θ_{mi} in the pass-band. Furthermore, the artificial transmission lines are considered to be terminated by their image impedances.



Fig. 6. Simplified lossless model of the DVCO, composed by m-derived artificial lines without the crossed transistor T12.

A. Analysis with only one transistor in the active region at the time.

If the only DVCO transistor biased in the active region is Tr (Fig. 6), open loop r gain [6] will have module R calculated by:

$$R = \frac{Z_{\pi n} \cdot g_{mr}}{2} \tag{6}$$

and phase φ_r , as

$$\varphi_r = -\pi - (2r - 1) \cdot \theta_{mi}. \tag{7}$$

Oscillations will build up if the open loop gain has its module greater or equal to 1 and its phase is an integer multiple of 2π . This phase condition can be written as

$$\pi + (2r - 1) \cdot \theta_{mi} = 2q\pi \tag{8}$$

where q is an integer.

A possible oscillation condition is achieved when q is equal to 1. Replacing this value in (8) and using (5) to obtain the propagation factor θ_{mi} , oscillation frequency ω_o can be obtained, assuming that the module of gain is greater or equal to 1:

$$\frac{\omega_o}{\omega_c} = \frac{\sin\left(\frac{\pi}{4r-2}\right)}{\sqrt{m^2 + (1-m^2) \cdot \sin^2\left(\frac{\pi}{4r-2}\right)}}$$
(9)

As an example, oscillation frequencies were calculated using (9), for a 9 stage DVCO, varying

the value of *m* factor. Results are shown in Table I. It can be seen that as *m* decreases, the circuit frequency band is reduced. A value of m=1 results in a decade tunable DVCO, whereas m=0.4 gives a two-octave DVCO.

TABLE I OSCILLATION FREQUENCIES OF A 9 STAGE DVCO WITH EACH TRANSISTOR BIASED IN THE ACTIVE REGION AT THE TIME

ω_o / ω_c										
r	1	(1.5)	2	3	4	5	6	7	8	9
1.0	1.00	(0.71)	0.50	0.31	0.22	0.17	0.15	0.12	0.10	0.09
0.8	1.00	(0.78)	0.59	0.38	0.27	0.22	0.18	0.15	0.13	0.12
0.6	1.00	(0.86)	0.69	0.48	0.36	0.28	0.23	0.20	0.17	0.15
0.4	1.00	(0.93)	0.82	0.63	0.50	0.40	0.34	0.29	0.25	0.23

B. Analysis with a transistor pair in the active region.

It has been shown how discrete oscillation frequencies in DVCO band can be obtained by biasing one transistor in the active region at the time. In order to continuously tune a DVCO over the entire band, it is necessary to bias pairs of transistors in the active region at the time, using complementary variation of transistor bias [1]. Each active transistor pair Tr and Ts (Fig. 6) will be used to tune a frequency interval of the total oscillation band.

Let *S* be the open loop gain module and φ_s the phase of the loop containing transistor *Ts*. In order to verify phase and minimum module of composite gain to obtain oscillation, one may write:

$$R_{\min} \cdot \cos \varphi_r + S_{\min} \cdot \cos \varphi_s = 1, \qquad (10)$$

$$[R_{\min} \cdot \sin\varphi_r + S_{\min} \cdot \sin\varphi_s]j = 0j, \qquad (11)$$

where R_{min} and S_{min} are the minimum open loop gain module to achieve limit oscillation conditions.

Minimum oscillation gain condition (10)-(11) at a given frequency can be geometrically represented by Fig. 7a. By changing open loop module gains to R` and S` in a complementary way (Fig. 7b), *i. e.* increasing one and decreasing the other, it is possible to modify phase condition keeping open loop gain module equal to 1. That new open loop phase condition will allow variation of the oscillation frequency.

By solving the system (10)-(11) it is possible to find minimum open loop gain modules R_{min} and S_{min} that leads to oscillation:

$$R_{\min} = \frac{\sin\varphi_s}{\sin(\varphi_r - \varphi_s)},$$
 (12)

$$S_{\min} = \frac{\sin\varphi_r}{\sin(\varphi_s - \varphi_r)}.$$
 (13)



Fig. 7. Phasorial representation of open loop r and s gain: (a) oscillation condition; (b) phase changing through transconductance variation.

Analyzing (12) and (13) one concludes that it is necessary to attend the phase condition

$$0 < \varphi_{\rm r} - \varphi_{\rm s} < \pi \,, \tag{14}$$

in order to avoid infinite and negative values of R_{min} and S_{min} . Thus (14) must be verified for each pair of transistors in order to guarantee that it can be used over the frequency range of interest.

Phase condition (14) can be observed for any consecutive transistor pair in the DVCO structure, except for *T1* and *T2* [2]. At $0,71\omega_c$, phase difference $\varphi_r - \varphi_s$ becomes equal to π . To solve this problem it was proposed [1] that a crossed transistor, named *T12* (Fig. 2), should be added between first and second DVCO stages. Its drain is connected to *T1* drain and its gate is placed with *T2* gate, as *T12* associated total loop phase shift is intermediary between *T1* and *T2* shifts. Oscillation frequencies for the case when the only transistor biased in the active region is *T12* also can be calculated trough (9), using *r*=1.5 [6]. They are also listed in Table I in the column *r*=1.5.

Given a DVCO with the transistors Tr and Ts biased in the active region, it is possible to calculate the minimum transconductance $g_{mr,min}$ that leads to open loop gain with module equal to 1 and phase equal to 2π . Replacing (7) in (12) and making (12) equal to (6) one obtains:

$$g_{mr,\min} = \frac{2 \cdot \sin[\pi + (2s-1) \cdot \theta_{mi}]}{Z_{\pi n} \cdot \sin[2 \cdot (s-r) \cdot \theta_{mi}]}.$$
 (15)

In an analogous manner, it is possible to obtain minimum Ts transconductance $g_{ms,min}$ that allows oscillation:

$$g_{ms,\min} = \frac{2 \cdot \sin[\pi + (2r-1) \cdot \theta_{mi}]}{Z_{\pi n} \cdot \sin[2 \cdot (r-s) \cdot \theta_{mi}]}.$$
 (16)

Equations (15) and (16) provide useful information to select the transistors to be used in the DVCO design.

VI. APPLICATION EXAMPLE

In order to exemplify numeric results from the linear analysis developed, an application example is described.

The objective first is to estimate the transconductance tuning function of an approximately three-octave feedback reverse DVCO, required to maintain open loop gain equal to 1. Lossless m-derived artificial transmission line with factor m=0.8 and system reference impedance $Z_0=50 \Omega$ may be used.

Table I shows that a 9 stage DVCO is able to cover the desired frequency range, for m=0.8.

Analysis of phase condition (14) shows that the strictly necessary transistors are *T1*, *T12*, *T2*, *T3*, *T5* and *T9* [6].

Transconductance tuning curves (Fig. 8) can be obtained from (15) and (16). Image impedance $Z_{\pi m}$ is calculated through (4), in which the *L/C* ratio is obtained from (3). Phase shift θ_{mi} is calculated through (5) at the frequencies in the DVCO band, *i. e.* from $0.12\omega_c$ to ω_c .

Limit operation frequencies of each transistor are calculated from (9), and the results can be extracted from Table I in the column m=0.8. For example, pair T5-T9 is active from $0.12\omega_c$ to $0.22\omega_c$.

Transconductance curves (Fig. 8) are separated by dashed lines, limiting the actuation range of each transistor pair. It is observed that the value of transistor transconductance necessary to satisfy minimum open loop gain for oscillation is larger for lowest frequencies. This occurs because the difference between open loop active stages r and s $(\varphi_r \cdot \varphi_s)$ is higher at lower frequencies, since some stages do not have transistors. In addition, image impedance $Z_{\pi m}$ (4) decreases as frequency drops, which demands larger values of transconductances as can be concluded from (15)-(16). The highest required value for transistor transconductance was 55 mS, which occurred for transistor *T5* at 0.19 ω_c .



Fig. 8. Minimum transconductance values required to obtain oscillation conditions, for a 9 stage DVCO with m=0.8 and $Z_{0}=50 \Omega$.

VII. CONCLUSION

A generalized linear model for the reverse feedback DVCO that applies m-derived artificial transmission lines was presented. It was shown that the increasing of m factor decreases the tuning range of DVCO. Useful equations were derived, which allow predicting circuit oscillation frequency behavior, as well as the minimum transistor transconductance required for oscillations to start-up. An application example is presented in this paper, and the obtained analysis results were also successfully applied to the design of a 1 to 3 GHz DVCO prototype [6].

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