IEEE Transactions on Nuclear Science, Vol. NS-28, No. 6, December 1981

Annealing of MOS Capacitors with Implications for Test Procedures to Determine Radiation Hardness

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Abstract

The short- and long-term anneal of radiation-induced flatband voltage shift in both Al- and Si-gate MOS capacitors following pulsed e-beam irradiation is examined. The short-term anneal was measured and found to be similar for both Al- and Si-gate capacitors. Experiments were performed to investigate the dependence of the long-term anneal on oxide thickness, temperature, and bias. The Al-gate capacitors exhibited a low interface-state buildup following irradiation and had a long-term annealing curve with a simple ln(t) dependence, while the Si-gate capacitors studied had a more complicated annealing curve due to the buildup of a larger number of interface states and lateral nonuniformities (LNUs). Thinning the gate oxide was found to dramatically reduce the effects of interface states and LNUs on the long-term anneal. In capacitors where the effects of interface states and LNUs are small the long term annealing was found to be only weakly temperature dependent over the range -60 to 100°C, and removal of bias following irradiation had little effect. On the other hand, the long-term annealing of capacitors with a significant buildup of radiation-induced interface states and LNUs exhibited a strong temperature and post-radiation bias dependence. Some implications of the experimental results for the proper design of test procedures for determining radiation susceptibility are discussed.

Introduction

In order to predict whether a CMOS device will operate at times of interest in nuclear weapon (high dose rate) or space satellite (low dose rate) environments, one must know the mechanisms governing the recovery of the device.[1-5] Because several of these mechanisms are operative over a long time scale, it is possible for a device in a weapon environment to operate at 1 s and fail at 1000 s, or to be inoperable at 1 s and recover by 1000 s; in a space satellite environment, where a large total dose (~1 Mrad) is accumulated over a long time period, it has been shown that the annealing of trapped charge, which occurs over an extended time, can improve the radiation tolerance of a device.[1] In addition, an understanding of the mechanisms involved in the recovery or anneal is essential in the proper design of test procedures for the prediction of device response at times and in environments of interest.[3,4]

The annealing processes that can occur in MOS structures are illustrated in Fig. 1, which is a plot of voltage shift, ΔV, versus time following pulsed irradiation of an MOS device or capacitor under positive bias. The short-term recovery (rapid anneal) of an MOS structure from its initial shift following irradiation, $\Delta V(0^+)$, has been shown to be governed by the transport of radiation-generated holes to the SiO_2/Si interface.[6-8] Although most of the holes transport to the interface in times less than 1 s, significant transport can occur to much later times because of the highly dispersive nature of the transport,[7,8] particularly at low fields, i.e., fields less than 1 MV/cm. When the holes arrive at the interface, a certain percentage are trapped and may be subsequently annealed. In addition, there may be the buildup of radiation-induced interface states and lateral nonuniformities (LNUs).[5,9] These processes largely govern the long-term anneal of the capacitor. For those capacitors where the effects of interface states and LNUs are small, the recovery has an approximate ln(t) dependence and will saturate at very late times ($\Delta V \to 0$ or some "permanent" value as $t \to \infty$). For those capacitors where there is a significant buildup of radiation-induced interface states and LNUs, the annealing curve will strongly deviate from a ln(t) dependence and the flatband voltage may anneal back well past its preirradiation value. Finally, radiation-induced interface states also anneal at late times, especially at elevated temperatures.[9]

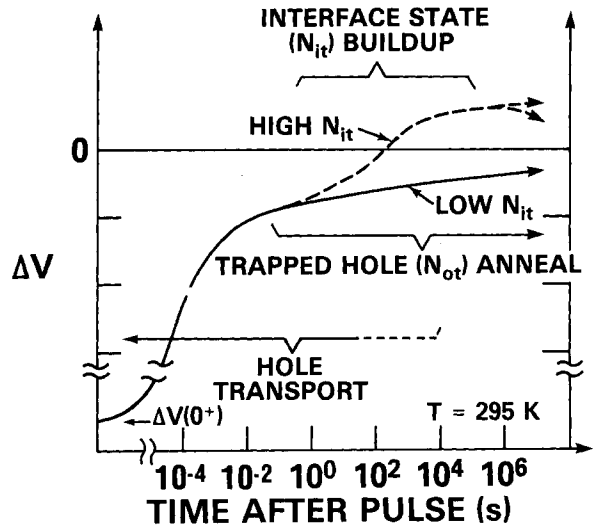

Fig. 1. Annealing processes in MOS structures following pulsed irradiation.

In this paper we investigate the short- and long-term recovery of both Al- and Si-gate MOS capacitors following pulsed e-beam irradiation. In the following sections we characterize the role of hole trapping, interface states, and LNUs on the recovery, and examine the dependence of the long-term anneal on gate-oxide thickness. Results of detailed experiments on the temperature and bias dependence of the long-term anneal will be presented, and interpreted in terms of their significance in the proper design of test procedures for determining radiation susceptibility.

Samples and Experimental Techniques

The MOS capacitor samples used in this study were supplied by Hughes Aircraft Corporation (HAC) and Sandia National Laboratories (SNL). The samples from

Hughes[7,9] had hardened wet and dry SiO_2 gate insulators grown on 3 to 5 Ωcm <100> n-type Si with 25-mil-diameter Al-gate electrodes. The wet-process oxide was pyrogenically grown at 950°C to a 96.5-nm thickness and annealed at 925°C in N_2 for 20 min; the dry-process oxide was grown at 1000°C to a 91-nm thickness and was not annealed. The samples from Sandia consisted of two sets of MOS capacitors with hardened SiO_2 gate insulators of varying thickness--one set had Al gates and the other set had poly-Si gates. All Sandia samples, dry grown at 1000°C on 3 to 5 Ωcm <100> n-type Si, were not annealed and had 40-mil-diameter electrode areas. Bias-temperature stressing the capacitors at 10 V and 200°C for 5 min resulted in flatband voltage shifts of less than 70 mV.

The pulsed e-beam irradiations reported in this paper were performed with the electron linear accelerator (LINAC) at the Armed Forces Radiobiology Research Institute. The LINAC produced a nominal 13-MeV, 1-A electron beam with a pulse width of 4 μs. The samples were irradiated in an evacuated sample holder which had provisions for electron-beam dosimetry and for control of sample temperature. For the rapid annealing measurements, each sample was exposed to a single low-dose (~20-krad[SiO_2]) pulse. A fast high-frequency capacitance-voltage (C-V) measurement apparatus[10] was used to record the preirradiation flatband voltage in the MOS test capacitors and to follow the flatband voltage, V_{FB}, at logarithmically spaced time intervals from 0.2 ms to 800 s following a LINAC pulse. This system employed a capacitance monitor operating at 5 MHz, and momentarily interrupts bias to apply 0.1-ms-duration voltage ramps to measure V_{FB}.

For the long-term annealing measurements, capacitors were exposed to single and multiple (at the rate of 60/s) ~140-krad(SiO_2) LINAC pulses to obtain total doses in the range from 140 krad(SiO_2) to 1 Mrad(SiO_2). The dose was varied to insure measurable and useful changes in experimental parameters of interest. A 1-MHz capacitance monitor was employed, and C-V curves were digitized and recorded using 50-ms-duration voltage ramps applied at logarithmically spaced time intervals from 20 ms to at least 4000 s. Generally, at times greater than 10^5 s, samples were removed from the fast C-V apparatus and placed on a mobile stressing station to maintain bias. The samples were periodically removed from this station to measure C-V traces using a system employing a 1-MHz capacitance meter and a 10-s-duration voltage ramp. All C-V curves were analyzed by the Terman technique[11] to obtain a distribution of interface states over the Si band gap. The resulting distribution was integrated from midgap to flatband to provide single values, $N_{it}(cm^{-2})$, of interface states. In addition, at late times a Gray-Brown shift[12] was measured to obtain a final integrated value of interface states and to check for the presence of LNUs.[13,14]

In the experiments described in the following sections we are investigating annealing mechanisms in MOS capacitors fabricated on n-type Si. The capacitors are irradiated under positive bias in an attempt to simulate radiation effects in n-channel MOS transistors (even though these transistors are fabricated on p-type Si). In suggesting that the results of this work can be applied to actual device response, we assume that the contributions to ΔV_{FB} in our capacitors (i.e., positive charge in the gate oxide trapped near the SiO_2/Si interface and negative charge from acceptor-like interface states in the upper half of the Si band gap between midgap and flatband) are similar to the charge contributions important in determining the threshold voltage shift in n-channel transistors.

Experimental Results

A. Short-term or Rapid Anneal

Figure 2 shows the time dependence of the anneal of ΔV_{FB} in HAC Al-gate dry-oxide capacitors as a function of sample temperature. The samples were irradiated in a single pulse to a dose of ~20 krad(SiO_2) under a 1-MV/cm bias at temperatures from ~79 K to 300 K. $\Delta V_{FB}(t)$ was recorded from 0.2 ms to 800 s following irradiation using 0.1-ms-duration voltage ramps. The data are normalized in each case to the flatband shift, $\Delta V_{FB}(0^+)$, obtained at low temperature (~79 K) at 0.2 ms after the LINAC radiation pulse. At 79 K, the normalized ΔV_{FB} shows little change with time out to 800 s. As the sample temperature is raised above ~130 K, significant ΔV_{FB} annealing within 800 s begins to occur. At 300 K, most of the annealing has evidently taken place by the time of the first measurement. This fast annealing behavior has been described in detail in terms of temperature- and field-activated dispersive transport of the radiation-generated holes through the oxide layer.[7-10] In the Continuous Time Random Walk (CTRW) model of hole transport in SiO_2,[7] the $\Delta V_{FB}(t)/\Delta V_{FB}(0^+)$ annealing curve is characterized by a form factor, α, which has been observed to fall in the range from 0.1 to 0.3 and is taken as a measure of the bulk transport properties of the oxide, i.e., the density of localized states in the oxide. From the data in Fig. 2, α for the Al-gate dry-oxide capacitors was found to be 0.22. The measured ΔV_{FB} also includes a contribution from holes which become trapped over the long term near the Si/SiO_2 interface; analysis of the data shows that this "permanent trapping" contribution corresponds to the capture of ~5 percent of the holes reaching the interface.

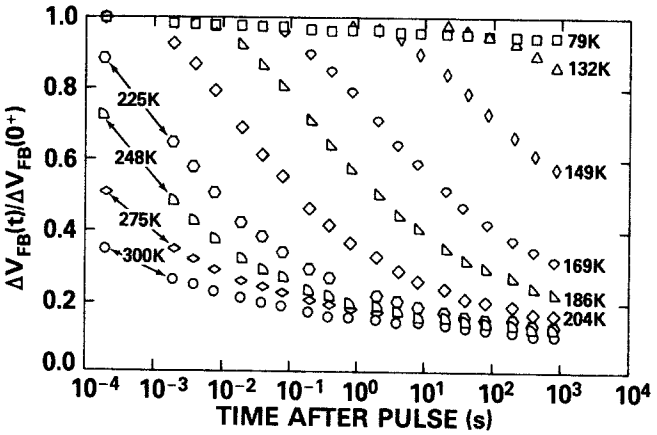

Fig. 2. Normalized flatband voltage shift in HAC Al-gate 91-nm dry-oxide capacitors following a single-pulse 20-krad(SiO_2) LINAC irradiation under a 1-MV/cm applied field at temperature from 79 to 300 K.

Figure 3 shows similar data for the effect of temperature on the time dependence of the rapid anneal of ΔV_{FB} in SNL Si-gate 66-nm dry-oxide capacitors. The samples were irradiated to a dose of ~38 krad(SiO_2) under a 1-MV/cm bias at temperatures from ~80 K to 380 K. For temperatures below ~275 K, the annealing curves for the Si-gate capacitors are qualitatively

similar to those for the Al-gate capacitors (Fig. 2). Analysis of the curves in this range yields an α value of 0.17 and ~5 percent "permanent" hole trapping. Evidently the use of aluminum or silicon gates has very little effect on the rapid annealing of ΔV_{FB}; this is not surprising, since hole transport depends on the bulk properties of the SiO_2 (hence the similar α value for Al and Si gate). However, differences in the annealing behavior for Al- and Si-gate capacitors do appear at temperatures above ~268 K. The Si-gate capacitors show apparently accelerated annealing at later times with respect to the Al-gate capacitors at these high temperatures. As will be shown later, this behavior is associated with a significant buildup of interface states in the Si-gate samples.

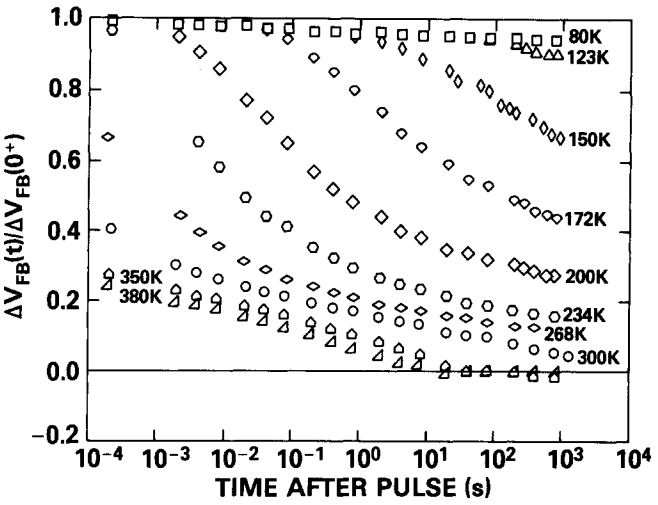

Fig. 3. Normalized flatband voltage shift in SNL Si-gate 66-nm dry-oxide capacitors following a single-pulse 38-krad(SiO_2) LINAC irradiation under a 1-MV/cm applied field at temperatures from 80 to 380 K.

B. Long-term or Slow Anneal

1. Oxide thickness dependence

In Fig. 4 the change in flatband voltage, ΔV_{FB}, is plotted versus time following irradiation for each of the capacitors in the SNL Al-gate set of varying gate oxide thickness, i.e., thicknesses of 25, 49, 57, and 85 nm. Each sample was exposed to seven LINAC pulses, delivered at the rate of 60/s to obtain a total dose of ~1 Mrad(SiO_2), and was irradiated with a field of 1 MV/cm applied across the oxide. ΔV_{FB} is shown for each sample from 20 ms to at least 4000 s (time is measured from the end of the last pulse). The resulting annealing curves for capacitors at the three smallest thicknesses show ΔV_{FB} linearly decreasing with the logarithm of time (ln(t)) for at least 5 decades beginning at ~0.2 s. For these capacitors, the increase in interface states from the preirradiation value (~10^{11} cm^{-2}) was determined by a Terman analysis of the C-V curves to be less than 30 percent. The annealing curve for the 85-nm capacitor less closely approximates a ln(t) behavior and was measured to have a 100 percent increase in the number of interface states following irradiation. Late-time Gray-Brown measurements indicate an increase in the final number of interface states as the gate oxide thickness increases, and show that the number of LNUs is small for all capacitors in this Al-gate set. Of course, at late times (times greater than 10^5 s) all annealing curves depart from their ln(t) behavior as $\Delta V_{FB} \rightarrow 0$. In addition, we have observed a ln(t) annealing behavior for hardened HAC Al-gate wet- and dry-grown oxides irradiated to a dose of ~10^5 rads; at this dose the buildup of interface states was found to be negligible in these samples.

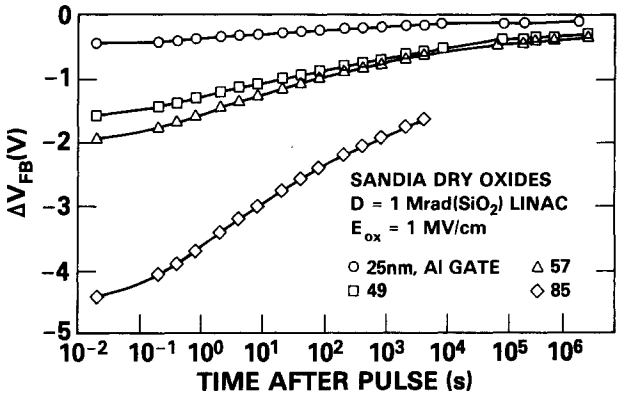

Fig. 4. Annealing curves for SNL Al-gate capacitors of varying gate-oxide thickness following a 1-Mrad(SiO_2) LINAC irradiation at an applied field of 1 MV/cm.

In Fig. 5 a family of C-V traces taken from 20 ms to 4000 s are shown for each of the samples in the SNL Si-gate set, i.e., thicknesses of 35, 55, 66, and 90 nm. These C-V traces were recorded for each sample following a 150-krad(SiO_2) LINAC irradiation with a field of 1 MV/cm applied across the oxide. Preirradiation C-V traces and flatband capacitances, C_{FB}, are marked for each of the samples on the figure. For the 35-nm sample, the first (20-ms) C-V trace following irradiation is shifted toward more negative voltage corresponding to an increase of positive charge in the oxide layer, but has essentially the same shape as the preirradiation trace, indicating no change in the interface-state density. As time progresses, the sample anneals or relaxes back toward the preirradiation condition and the corresponding C-V traces do not change in shape. For the 55- and 66-nm samples, the first trace following irradiation is once again shifted to more negative voltages with no change in shape or increase in distortion. However, as time progresses the sample anneals back toward the preirradiation condition and the C-V traces are seen to flatten out or increase in distortion. At 4000 s, the 55- and 66-nm capacitors have annealed back to their preirradiation flatband voltage. Finally, the 90-nm sample has a C-V trace taken at 20 ms that is already distorted compared with the preirradiation trace. As time progresses, the distortion in the traces steadily increases, with the flatband voltage taken from the trace at 4000 s indicating that the sample has annealed back well past its preirradiation flatband voltage.

Gray-Brown measurements taken before and after irradiation show an increase in the number of interface states in these Si-gate samples. However, the shape of the 77-K C-V trace used in the Gray-Brown determination is distorted from its preirradiation shape, indicating the presence of LNUs. Because the distortion in the C-V traces is due to a combination of interface states and LNUs, we cannot report actual values of interface states via a Terman analysis. Measurements we have performed on a wide variety of

samples suggest a relationship between the observation of LNUs and the buildup of radiation-induced interface states, specifically, that LNUs may result from a nonuniform distribution of interface states.[14] However, since (1) late-time Gray-Brown shifts indicate a definite increase in the number of interface states, and (2) the annealing of flatband voltage past its preirradiation value requires an increase in negative charge at the interface (interface states are acceptor-like in the upper half of the Si band gap and add a negative charge contribution), we feel that the annealing of flatband voltage past its preirradiation value for the 66- and 90-nm samples is largely due to a time-dependent buildup of interface states.[5,9] It is important to note that radiation-induced interface states and LNUs are significantly reduced as the oxide is thinned from 90 to 35 nm.[10]

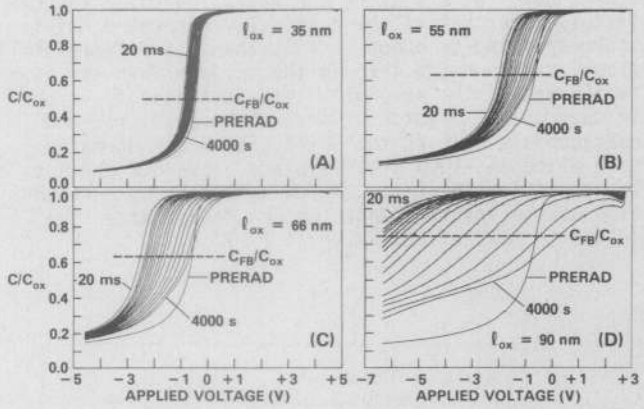

Fig. 5. Sets of C-V traces following a 150-krad(SiO_2) LINAC irradiation for Si-gate samples of varying gate-oxide thickness. Preirradiation, 20-ms, and 4000-s C-V traces and flatband capacitance, C_{FB}, are marked for each of the samples.

Figure 6 shows annealing curves for each of the Si-gate samples shown in Fig. 5. These curves were obtained by plotting the change in flatband voltage, ΔV_{FB} (taken from the C-V traces in Fig. 5), versus time following irradiation. The annealing curve for the 35-nm capacitor shows a ln(t) dependence. However, as the gate oxide thickness is increased, the effects of interface states and LNUs increase and the annealing behavior begins to deviate from a ln(t) dependence. This deviation from ln(t) is greatest for the 66- and 90-nm samples, where the effects of interface states actually result in ΔV_{FB} going positive.

2. Temperature dependence

Figure 7 shows the effect of temperature on the long-term anneal of ΔV_{FB} in HAC Al-gate dry-oxide capacitors. The samples were exposed to single 150-krad(SiO_2) LINAC pulses under a 1-MV/cm applied field at temperatures from 214 to 373 K. At times less than 1 s, where the annealing is still dominated by the late stages of the hole transport, reducing the temperature slows down the hole transport and consequently the annealing. This is evident if one compares ΔV_{FB} at 20 ms for samples irradiated at 214 and 295 K. The spread in ΔV_{FB} with temperature over the time scale from 20 ms to 1 s is not as pronounced as in Fig. 2, which shows the rapid anneal following a low-dose 20-krad(SiO_2) LINAC irradiation. The reason for this difference is that for the curves in Fig. 7, we delivered a much higher dose in a single pulse. This undoubtedly leads to some electric field modification during the rapid anneal (specifically, an increase in the field in the interface region), which tends to speed up the anneal and obscure the temperature dependence of the rapid anneal. At times greater than 1 s, field perturbations are reduced, and we observe the characteristic ln(t) dependence of the long-term anneal. We also observe essentially no temperature dependence for the anneal of ΔV_{FB} for times out to 10^6 s. (Capacitors at 214, 273, 323, and 373 K were returned to room temperature at later times and ΔV_{FB} was measured; these values are given as the solid data points in Fig. 7.) For these HAC Al-gate dry-oxide samples there was a negligible increase in the number of interface states following irradiation.

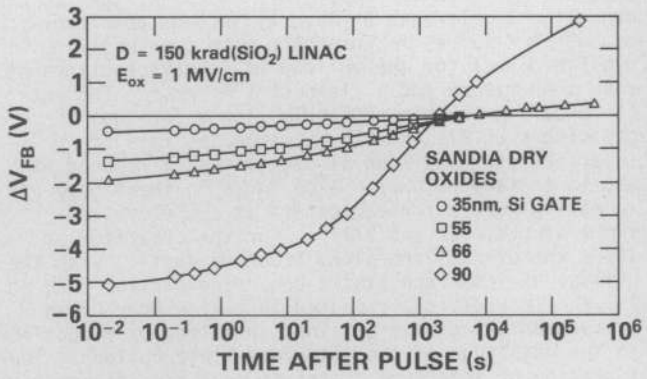

Fig. 6. Annealing curves for the samples shown in Fig. 5, obtained by plotting the change in flatband voltage, ΔV_{FB}, versus time following irradiation.

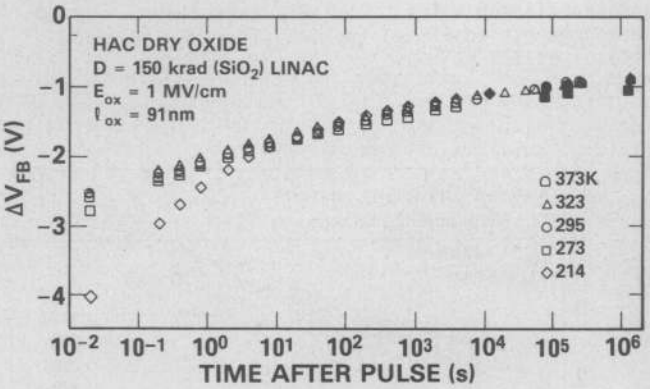

Fig. 7. Effect of temperature on the anneal of ΔV_{FB} in HAC Al-gate dry-oxide capacitors following a 150-krad(SiO_2) LINAC irradiation at an applied field of 1 MV/cm.

We also examined the effect of temperature on the long-term anneal of ΔV_{FB} in HAC Al-gate wet-oxide capacitors. These capacitors were exposed to seven LINAC pulses to obtain a total dose of 1 Mrad(SiO_2) under a 1-MV/cm applied field at temperatures of 295, 327, and 378 K. For these samples the buildup of

interface states was small, and the annealing curves showed a weak temperature dependence.

Figure 8 shows the effect of temperature on the long-term anneal of ΔV_{FB} in SNL 66-nm Si-gate capacitors. These capacitors were exposed to single 150-krad(SiO_2) LINAC pulses under a 1-MV/cm applied field at temperatures from 218 to 373 K. The annealing curves for the three lowest temperatures are relatively close and exhibit a weak temperature dependence from 0.2 to 20 s. As time progresses, the capacitor at 295 anneals far more rapidly than the capacitor at 218 K. This result can be explained by the time-dependent buildup of radiation-induced interface states and LNUs, which play a significant role in the long term anneal of the 66-nm Si-gate capacitors. The rate of buildup of interface states following pulsed e-beam irradiation has been established to be a strongly temperature-activated process.[9,15] For the capacitors at 295 K, the annealing accelerates at several seconds and levels off at ~5 x 10^4 s, in agreement with previously published data for the buildup of interface states at room temperature and a field of 1 MV/cm.[15] The rate of annealing is then obviously slower for the capacitors at 273 and 218 K, since the rate of interface-state buildup is significantly reduced at the lower temperatures. Also shown in the figure are annealing curves for capacitors at two elevated temperatures, 323 and 373 K. For the capacitor at 323 K the overall annealing proceeds faster, with the buildup of interface states occurring earlier than at 295 K. In addition, repeated late-time Gray-Brown measurements indicate a slight annealing or reduction in the magnitude of the interface-state buildup. The annealing of interface states is more significant in the response of capacitors at 373 K. At this elevated temperature, interface states are constantly being annealed during their buildup,[9] which is occurring much earlier than at room temperature. After this buildup saturates at ~40 s, interface states continue to slowly anneal out at later times. Since fewer interface states are present at later times in the sample at 373 K than in the sample at room temperature, the sample at 373 does not anneal back past its preirradiation value. Periodic late-time Gray-Brown measurements confirmed the annealing of interface states at 373 K.

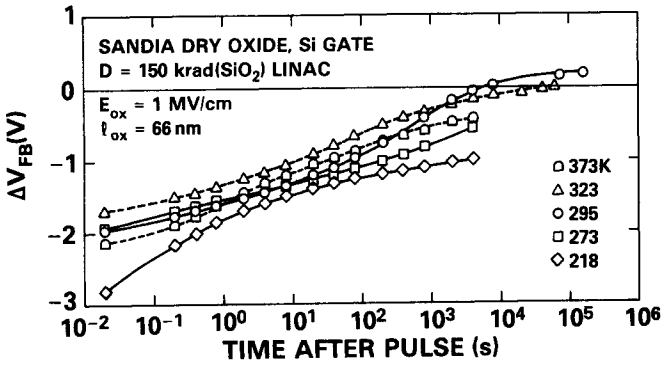

Fig. 8. Effect of temperature on the anneal of ΔV_{FB} in SNL Si-gate dry-oxide capacitors following a 150-krad(SiO_2) LINAC irradiation at an applied field of 1 MV/cm.

3. Bias dependence

Figure 9 shows the effect of applied bias on the slow anneal of ΔV_{FB} in HAC Al-gate dry-oxide capacitors. The samples were exposed to single LINAC pulses under 1 MV/cm applied field. For the curve labeled "(1)" the field was maintained at 1 MV/cm (E_{ox} = 1); the sample anneals smoothly with an approximate ln(t) characteristic. For the curves labeled E_{ox} = 4 and 0 the applied field was switched to these values (in MV/cm) at 2 s after the pulse. The annealing curve for the 1 to 4 MV/cm switch shows a stepwise reduction in ΔV_{FB} immediately after the switch, and then continues a slow recovery. Analysis of this curve suggests that the fraction of "permanently" trapped holes present does not change as a result of the bias switch. Instead, the step reduction in ΔV_{FB} may be attributed to the effect of increased electric field on the tail of the hole transport process. From the CTRW model,[7] at 2 s after the radiation pulse approximately 5 percent of the originally generated holes (corresponding to about -1 V flatband shift) are still slowly transporting through the oxide. When the bias is increased, the strongly field-activated transport is sped up by a factor of several hundred,[7,10] and consequently most of the shift that would normally take place in ~1000 s takes place between 2 and 4 s. The curve for the 1 to 0 MV/cm switch shows a reduction of the fraction annealed per decade after the switch to ~2/3 of its value at 1 MV/cm.

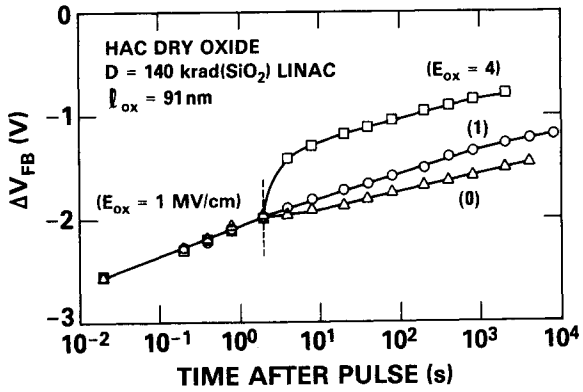

Fig. 9. Effect of switching applied bias on the long term anneal of HAC Al-gate dry-oxide capacitors following a 140-krad(SiO_2) LINAC irradiation at an applied field of 1 MV/cm.

We also examined the effect of maintaining bias on the slow anneal of ΔV_{FB} in HAC Al-gate wet-oxide capacitors. The samples were exposed to single LINAC pulses under a 1-MV/cm applied field, and the field was either maintained at 1 MV/cm or switched to 0 MV/cm at 2 s following irradiation. The results are nearly identical to those observed for the HAC Al-gate dry-oxide capacitors.

Figure 10 shows the effect of changing the bias voltage on the annealing in SNL 66-nm Si-gate capacitors. As for the Al-gate units, the applied field was either maintained at 1 MV/cm throughout or switched at 2 s to either 0 or 4 MV/cm. When the applied field was swtiched to 0, the sample anneals after the switch approximately as ln(t), but at a rate slightly reduced from that observed at 1 MV/cm before the switch. For the unswitched case, the annealing curve shows an accelerated positive shift from ~10 to

~1000 s, and ΔV_{FB} becomes positive at ~5000 s. As discussed previously (Fig. 7), this behavior is attributed to the enhanced buildup of interface states. This interface-state buildup is largely complete by ~5 x 10^4 s under a 1-MV/cm field, but is mostly suppressed at zero field.[15] In the case of the 1 to 4 MV/cm switch, a step reduction in ΔV_{FB} is observed immediately after the switch at 2 s similar to that shown in Fig. 9 for the Al-gate samples. ΔV_{FB} continues to shift rapidly positive following the switch out to ~100 s, then slows slightly and becomes positive at ~3000 s. Two processes evidently occur here. First, the bias switch induces a sudden speedup in hole transport as described earlier for the analogous Al-gate data (Fig. 9). Second, the bias switch accelerates the buildup of interface states. In this case, the buildup is completed by ~5000 s. Figure 10 also shows that the 1- and 4-MV/cm curves approach each other at late times (times greater than 5 x 10^4 s). This is expected, since it has been shown in previous work[9] that an increase in applied field (after most of the radiation-generated holes have transported) speeds up the buildup of interface states, but does not change the final number produced.

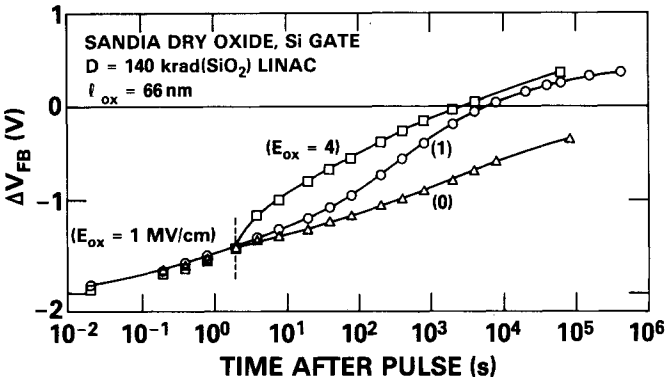

Fig. 10. Effect of switching applied bias on the long-term anneal of SNL Si-gate dry-oxide capacitors following a 140-krad(SiO_2) LINAC irradiation at an applied field of 1 MV/cm.

Discussion of Results and Implications for Test Procedures

We now interpret the results of the experiments we performed on the short- and long-term anneal of MOS capacitors following pulsed e-beam irradiation. We draw conclusions for two separate classes of samples, namely, those samples where the effects of radiation-induced interface states and LNUs are small (low N_{it}), and those samples where the effects of interface states and LNUs are more significant (high N_{it}). The first class of samples includes the HAC Al-gate capacitors, the SNL Al-gate capacitors (except the 85-nm capacitors), and the 35-nm SNL Si-gate capacitors. The second class of samples includes SNL Si-gate capacitors with oxide thicknesses of 55, 66, and 90 nm.

Measurements on the long-term annealing of ΔV_{FB} following pulsed e-beam irradiation show that samples with low N_{it}, e.g., Al-gate capacitors as well as 35-nm Si gate capacitors, anneal with a approximate ln(t) dependence. This characteristic ln(t) dependence of the long-term anneal has been reported by other investigators.[1,2,4,5] When the voltage shift following irradiation is linear with dose (i.e., interface state and saturation effects are small) one generally observes a ln(t) dependence of the long-term anneal. For samples where there is significant interface-state and LNU buildup, e.g., Si-gate capacitors at 55, 66, and 90 nm reported on in this work, the voltage shift or charge buildup is not linear with dose because of the presence of interface states and LNUs. In this case the annealing function is more complicated (Fig. 6), and may involve dose-rate dependent effects. Consequently, prediction schemes which assume a simple annealing function and linear device response to dose cannot be used to predict the very-late-time response of these samples.[1] It is important to note that the effects of interface states and LNUs on the long-term anneal can be dramatically reduced as the oxide is thinned, leading to the simpler ln(t) behavior for the long-term anneal, as was observed for 35-nm Si-gate capacitors.

For low-N_{it} samples, it is evident from the data (Fig. 7) that reducing the temperature to that near dry ice (~200 K) from room temperature has no appreciable effect on the anneal at times greater than 1 s. Consequently, placing such a device in dry ice following irradiation in no way slows down or retards any of the late-time annealing mechanisms, nor can elevating temperature be used to accelerate the decay and enable one to determine a room-temperature response valid over several years. We also found that the removal of bias following irradiation of a low-N_{it} device does not drastically affect the long-term anneal (Fig. 9). Although raising the field to 4 MV/cm soon after irradiation has an immediate effect on the "tail" of the rapid anneal due to hole transport, an analysis of the curves indicates that the higher field does not significantly affect the slow annealing of the "permanently" trapped holes or result in a change in their number.

For high-N_{it} samples, the long-term anneal is affected by both temperature and bias. Because the buildup of radiation-induced interface states and LNUs is strongly temperature-activated, the anneal was accelerated as the temperature was raised from 218 to 295 K (Fig. 8). Placing a sample in dry ice at 1 min following irradiation would retard the overall anneal by suppressing the interface-state buildup, but might have no effect on other contributing annealing mechanisms, e.g., direct tunneling of electrons from the Si substrate and subsequent recombination with trapped holes which we believe may be an annealing mechanism for both Al- and Si-gate capacitors. Elevating the temperature in these samples may accelerate the overall anneal by speeding up the buildup of interface states; however, raising the temperature may lead to significant annealing of interface states at late times, especially at 373 K. Therefore, since several contributing annealing mechanisms may have different temperature dependencies, the usefulness in raising or lowering temperature for controlling the annealing rate is questionable, and results may not accurately simulate the anneal of a device in an actual environment. From Fig. 10 we can clearly see the importance of maintaining bias in capacitors where the buildup of interface states plays an important role. If the bias is removed following irradiation, the buildup of interface states is severely inhibited, and the overall annealing rate is significantly reduced from that obtained when bias is maintained. Raising the bias following irradiation accelerates the rate of interface-state buildup and the overall anneal.

The weak temperature and bias dependence of the long-term anneal observed in low-N_{it} samples (e.g. HAC Al-gate wet- and dry-oxide capacitors), together with their ln(t) dependence, is consistent with an anneal-

ing mechanism involving direct tunneling of electrons from the Si substrate into localized traps in the oxide and subsequent recombination with trapped holes.[17] The weak temperature dependence we observe in these samples at temperatures from -60 to 100°C agrees with that reported by Danchenko et al[18] for n- and p-channel transistors, but is different from that reported by Derbenwick and Sander,[1] who found that the annealing process for irradiated n-channel transistors was temperature-activated with an activation energy of ∿0.33 eV. They and other investigators[1,2,4,5] suggest that annealing of trapped charge at the interface may involve thermal untrapping of holes. In addition, Derbenwick and Sander point out that for a temperature-activated process, elevated temperature can be used to great advantage to accelerate the decay, so a room-temperature response can be determined which is valid over several years. This is not the case for any of the Al- or Si-gate capacitors being reported on in this paper.

In summary, we have found that for capacitors where the effects of radiation-induced interface states and LNUs are small, the long-term anneal curves have a ln(t) dependence over several decades in time, display a weak temperature dependence from -60 to +100°C, and are not drastically affected by the removal of bias. For capacitors where the effects of radiation-induced interface states and LNUs are more significant, the long-term anneal curves have a more complicated behavior that does not follow a ln(t) dependence, exhibit a stronger temperature dependence over the range -60 to +100°C, and demonstrate the importance of maintaining bias at all times following irradiation. The effects of interface states and LNUs on the anneal can be drastically reduced as the oxide is thinned, leading to the simpler ln(t) behavior. Finally, the early or rapid anneal of ΔV_{FB} due to hole transport does not differ significantly for Al- or Si-gate MOS capacitors.

Acknowledgements

The authors wish to thank T. Taylor for his help in performing many of the experimental measurements.

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