Article

Antenna-on-Chip for Millimeter Wave Applications Using CMOS Process Technology

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Abstract: In this paper, a monopole patch antenna is designed, and the structure of the antenna is analyzed. The manufacturing process adopts TSMC 0.18 μm CMOS process technology. An artificial magnetic conductor (AMC) on the M1 layer is proposed in this paper to increase the radiation gain and reduce the reflection coefficient (S11) magnitude for impedance matching and antenna performance. This method can make up for the radiation efficiency and benefits of the antenna-on-chip that are affected by the high dielectric constant and low resistivity of the silicon substrate of the CMOS process. The antenna designed in this paper obtains a simulated bandwidth of 37.5 GHz to 69.5 GHz using the Electromagnetic Simulation Software, and the fractional bandwidth of the design is 60%. Among them, 62 GHz shows a maximum gain value of −2.64 dBi. Actual measurements have confirmed that the reflection coefficient of the antenna on the chip proposed in this paper is the same as the simulation trend, and a wider bandwidth is obtained from 20.9 GHz to 67 GHz, with a fractional bandwidth of 104.89%. This bandwidth covers millimeter wave 28 GHz, 38 GHz, and 60 GHz application frequencies.

Keywords: millimeter wave; antenna-on-chip; CMOS process

1. Introduction

In the future, communication frequency band, millimeter wave, and sub-terahertz (Sub-THz) technologies can meet the requirements of the fifth-generation (5G) communication system. Therefore, to provide a wider bandwidth and faster transmission speed in the communication frequency band at this stage, the communication frequency band is developing towards the millimeter wave frequency band [1–3]. However, in some countries such as China and South Korea that use the 6 GHz frequency band, 5G mobile communication has been listed as a commercial frequency band. Hence, many transmission requirements increase, and the frequency bands below 6 GHz can no longer satisfy the transmission requirements of existing users. The millimeter wave is one of the most efficient solutions in improving the transmission efficiency of fifth-generation mobile communication and meeting users' needs. Through the characteristics of a millimeter wave, it can achieve a low delay, high-speed transmission, and other characteristics to meet the transmission needs of communication users [4,5]. The millimeter wave frequency band has various applications, such as fifth-generation (5G) communication systems, satellite communications, synthetic aperture radars, wideband high-speed point-to-point communications, automotive radars, and other technologies. However, millimeter wave frequency bands have shorter wavelengths than other application frequency bands, so the assembly components are smaller, making wireless systems more compact [6,7].

With the advancement of chip-integrated circuit manufacturing in recent years, component miniaturization can be easily achieved. Additionally, because of the advancement of radio frequency integrated circuits (RFIC), society is gradually paying attention to the concept of the antenna-on-chip. The wavelength of the millimeter wave frequency band is shorter than that of other frequency bands, which is conducive to small-size assembly.

Therefore, millimeter wave antennas can be easily fabricated on wafers [6,8,9]. The method of the antenna-on-chip is suitable for making millimeter wave antennas. The antenna-on-chip can avoid mutual influence in the circuit through circuit design such as integrated circuits (IC) [10]. In a transceiver, the antenna is often used as the first and last element of the transmitter and receiver. However, the antenna and transceiver circuit must match the 50 ohm impedance system impedance. The requirement of 50 ohm impedance matching is overcome in the antenna-on-chip. This is because the RF front-end and antenna can be co-designed in the chip, saving the external design area and components [11,12]. There are many challenges in antenna-on-chips. First of all, the Si substrate of the CMOS process is not suitable for the structural design of the antenna because the typical six-layer metal layer CMOS process is the reason that affects the radiation performance and efficiency of the antenna. Second, the distance between the metal layers in the manufacturing process is only 10 μm, the thickness of the Si substrate is 500 μm, and the low resistivity is 10 Ω cm. The above reasons cause most of the electromagnetic waves of the antenna to propagate to the substrate, which greatly reduces the gain of the antenna-on-chip. The high dielectric constant of the Si substrate (ϵ_r = 11.9) is also a reason for the reduction in the radiation efficiency of the antenna-on-chip. The electromagnetic waves generated by the antenna will be absorbed by the Si substrate instead of propagating into the air, so the radiation efficiency and gain of the antenna-on-chip cannot be compared with traditional typical antennas [13–16].

Many problems and challenges are often faced in the design of antenna-on-chips. Due to the high dielectric constant and low resistivity of the Si substrate made of wafer CMOS, the gain and radiation efficiency of the antenna-on-chip decrease, resulting in a more significant transmission loss for the antenna-on-chip [14,15].

Recently, antenna-on-chip design has often been considered in area planning and antenna architectures—for example, patch antennas [8,15,17–19], numerous meander-line antennas [9], slot antennas [20,21], Yagi-Uda antennas [22], and zig-zag antennas [23]. Among the types of patch antennas, the literature [8] reports a 28 GHz antenna-on-chip for wearable devices, using TSMC 0.18 μm CMOS process technology. The antenna size is 1160 μm × 790 μm. The beam steering of the antenna-on-chip is controlled by a parallel coupler design, and the fractional bandwidth is 84.7%. In [15], the patch antenna is proposed and applied in a millimeter wave frequency band for a 5G communication compact front-end receiver and adopts 28 nm CMOS process technology. This structure enhances the radiation gain of the antenna through the PCB-grounded metal structure and reaches 9.8 dBi. In [17], a patch antenna is used to propose an antenna-on-chip with dual frequency bands. The operating frequencies are 77 GHz and 140 GHz, respectively. The frequency bands fall into 63 GHz–78 GHz and 101 GHz–157 GHz. The fractional bandwidth is 21.28% and 35.21%, and the antenna radiation gain is −3.24 dBi and −5.795 dBi. The dual-band antenna has more advantages in the application. In [18], monopole patch antennas are designed, as well as specially designed square split ring resonators. By coupling to the feeding antenna, additional resonance is generated to solve the disadvantage of the antenna-on-chip gain drop. The literature experiment adopts 0.13 μm SiGe process technology, the working frequency is 81.5 GHz, and it has a gain of 1.61 dBi and a working bandwidth of 77 GHz–87 GHz. In [19], an antenna-on-chip is proposed, which combines a patch antenna with a substrate-integrated waveguide (SIW) and a dielectric resonator antenna (DRA), uses a 65 nm CMOS process with an operating frequency of 94 GHz, and uses an artificial magnetic conductor (AMC) to increase radiation. In [9], a numerous meander-line antenna is proposed, which is applied to the antenna chip in the millimeter wave frequency band. The dual-band operating frequency is 28 GHz and 60 GHz, and it uses 65 nm CMOS process technology. A gain of −10 dBi and a fractional bandwidth of 5.3% were obtained when measured at 28 GHz. A gain of 0 dBi and a fractional bandwidth of 5.9% were obtained when measured at 60 GHz. This antenna-on-chip has the advantage of dual-band 28 GHz and 60 GHz operation in the millimeter wave frequency band. It is applied in the slot antenna of the antenna-on-chip. In [20], a rectangular ring slot

antenna is proposed, using a dielectric resonator antenna (DRA) to make the gain of the antenna-on-chip reach 0 dBi at 40 GHz. In [21], the authors specially designed a back-to-back E-type artificial magnetic conductor (AMC) surface-assisted double-diamond slot structure antenna-on-chip, and it is used in the W-frequency band. It adopts 0.13 μm CMOS process technology, and the working frequency band is 80–90 GHz. It has a maximum radiation gain of −0.58 dBi at 84 GHz. The diamond-shaped slot structure antenna array and parasitic elements proposed in this document can obtain a wider bandwidth. In addition, Yagi-Uda antennas are often used as antennas-on-chip. In [22], a solution to the low-gain disadvantage of the antenna-on-chip is proposed, and the Yagi-Uda antenna architecture is designed. Through the basic driving elements, the reflectors and director of the Yagi-Uda antenna and the outer design of the semicircular arc structure increase the radiation gain of the antenna. This design architecture adopts a 180 nm CMOS technology process, the working frequency is 60 GHz, and the radiation gain is −20 dBi. In [23], the zigzag antenna is designed; the system architecture of the antenna-on-chip is proposed and provides high-speed transmission efficiency.

However, the area that can be planned on the top layer of the chip is limited, and how to design an antenna with a high gain and radiation efficiency in the limited area is a big challenge. Therefore, the use of the area needs to be considered when designing the antenna structure, so the antenna type must be carefully selected. For example, the patch antenna [8,15,17–19] and Yagi-Uda antenna [22] have a high gain and high directivity, which can make up for the low gain of the antenna-on-chip in terms of performance. This article adopts the structure of the monopole patch antenna to optimize the defects of the chip through the characteristics of high gain and high directivity. The design in this paper adopts TSMC 0.18 μm CMOS process technology, as shown in Figure 1a, which consists of six metal layers (Metal 1 to Metal 6 and the top metal layer) of six layers of silicon dioxide and an Si substrate. In the 0.18 μm CMOS process, the top metal layer (Metal 6) is the designed antenna layer, with a thickness of 2.34 μm, while the thickness of the Si substrate is 500 μm. The antenna design architecture consists of a transmission line and a tapered slit monopole patch antenna and is designed on the top metal layer (Metal 6). The design of AMC on the M1 layer, as shown in Figure 1b, can reduce the loss of electromagnetic waves due to the silicon substrate so that the antenna-on-chip designed in this paper has a better gain and wider application bandwidth. Through the high-frequency electromagnetic simulation software performing full-wave simulation, the antenna-on-chip's reflection coefficient (S11) is below the −10 dB standard, covering the frequency band from 37.5 GHz to 69.5 GHz, and the fractional bandwidth is 60%. Among them, the bandwidth covers the 38 GHz and 60 GHz application frequency bands of millimeter waves. The antenna has a maximum gain value at 62.1 GHz, exhibiting −2.64 dBi, and was measured at the Taiwan Semiconductor Research Institute of the National Research Institute. The measurement proves that the designed antenna-on-chip has a wider bandwidth. The measured bandwidth is 20.9 to 67 GHz, and the fractional bandwidth is 104.89%. This bandwidth covers the following application frequencies of the millimeter wave: 28 GHz, 38 GHz, and 60 GHz.
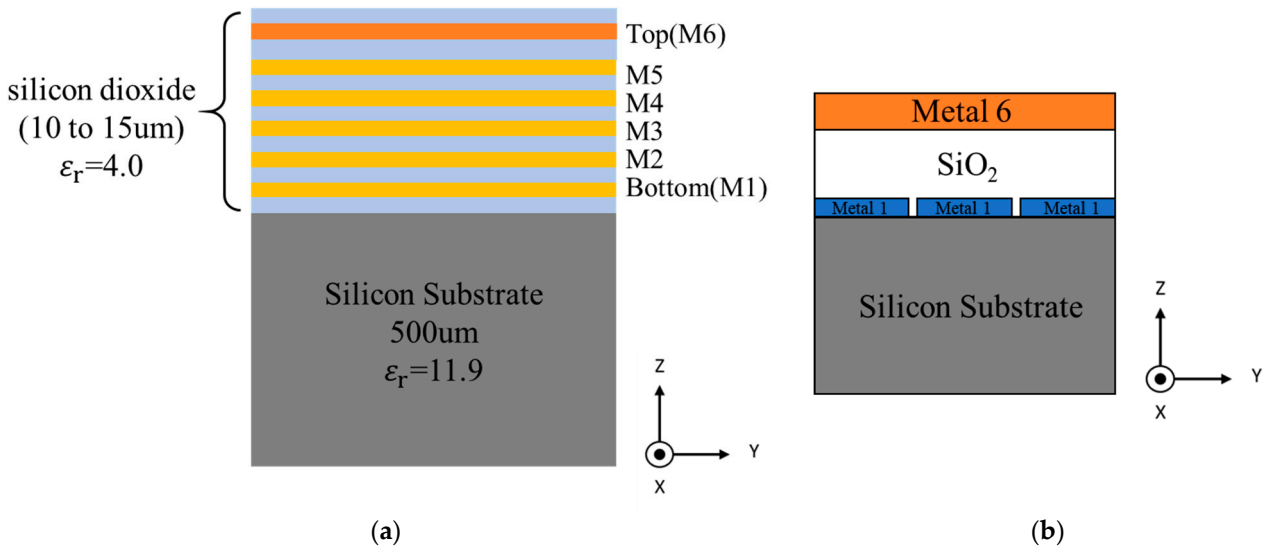
Figure 1. Layer stack of a typical six-metal-layer TSMC 0.18 μm CMOS process: (**a**) Cross-section view of the adopted TSMC 0.18 μm CMOS process; (**b**) The number of layers used in the antenna design on this chip.

2. Structure, Mechanism, and Design

To miniaturize the millimeter wave antenna, the characteristics of a compact size and small assembly components are realized, having performance advantages such as a high gain and high directivity. Figure 2 shows that the patch antenna is the most common design style because of its simple structure. Moreover, structural changes can be designed efficiently for design applications such as cone beams and fan beams, and they are also easy to control.
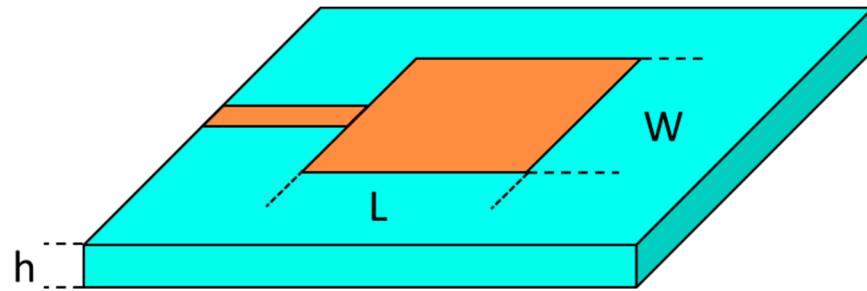
Figure 2. The geometry of the patch antenna.

The following is the basic formula for designing a microstrip patch. The width W of a rectangular patch is obtained by the following Formula (1); the effective dielectric constant can be calculated using (2); the length L is obtained by the following Formula (5):

$$W = \frac{c_o}{2f_r}\sqrt{\frac{2}{\epsilon_r + 1}} \tag{1}$$

$$\epsilon_{\text{eff}} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left[1 + 12\frac{h}{W}\right]^{-\frac{1}{2}} \tag{2}$$

$$\Delta L = 0.412\frac{(\epsilon_e + 0.3)\left(\frac{W}{h} + 0.264\right)}{(\epsilon_e - 0.258)\left(\frac{W}{h} + 0.8\right)} \tag{3}$$

$$L_{\text{eff}} = L + 2\Delta L \tag{4}$$

$$L = \frac{c_o}{2f_r\sqrt{\epsilon_{eff}}} - 2\Delta L \tag{5}$$

where W is the width of the patch antenna, c_o is the speed of light, ϵ_r is the dielectric constant of the substrate, f_r is the frequency, ϵ_e is the effective dielectric constant, ΔL is the length difference affected by the edge effect, L_{eff} is the effective length, and L is the actual length of the patch antenna.

In addition, the antenna element is fed by a microstrip transmission line with a characteristic impedance of 50 Ω. It can be expressed using Formula (6):

$$\frac{W_f}{h} = \frac{2}{\pi}\left\{\frac{60\pi^2}{Z_o\sqrt{\varepsilon_r}} - 1 - \ln\left(\frac{120\pi^2}{Z_o\sqrt{\varepsilon_r}} - 1\right)\right\} + \frac{\varepsilon_r - 1}{2\varepsilon_r}\left[\ln\left(\frac{60\pi^2}{Z_o\sqrt{\varepsilon_r}} - 1\right) + 0.39 - \frac{0.61}{\varepsilon_r}\right] \tag{6}$$

As shown by the above documents, patch antennas have many advantages. Therefore, considering the above documents, this paper designs an antenna-on-chip using TSMC 0.18 µm CMOS process technology, having a high bandwidth in the millimeter wave band. As shown in Figure 3, the overall structure comprises a triangular patch monopole antenna and a transmission line. In addition, the design of the AMC on the M1 layer is designed to enhance the gain of the antenna-on-chip, to prevent electromagnetic waves from spreading to the bottom and damaging the Si substrate, and to reduce the loss of electromagnetic waves [21]. The grounding of the antenna and the transmission line fed into the monopole antenna form a coplanar waveguide (CPW). The radiation gain and direction of the antenna-on-chip can be controlled by adjusting the size of the grounding area to achieve high-gain, high-directivity antenna performance. The geometric size of the antenna-on-chip and the overall size of the chip are marked with parameters, as shown in Figure 4. The values of all parameters are summarized in Table 1. The geometric size and detailed parameter values of the M1-layer AMC single structure are shown in Figure 5 and Table 2 and are simulated by high-frequency electromagnetic simulation software. The simulated reflection coefficient and radiation gain of the antenna-on-chip are shown in Figures 6 and 7. In this simulation, the antenna has the minimum reflection coefficient at 45 GHz, a coverage frequency band from 37.5 GHz to 69.5 GHz, and a maximum gain value of −2.64 dBi at 62 GHz.
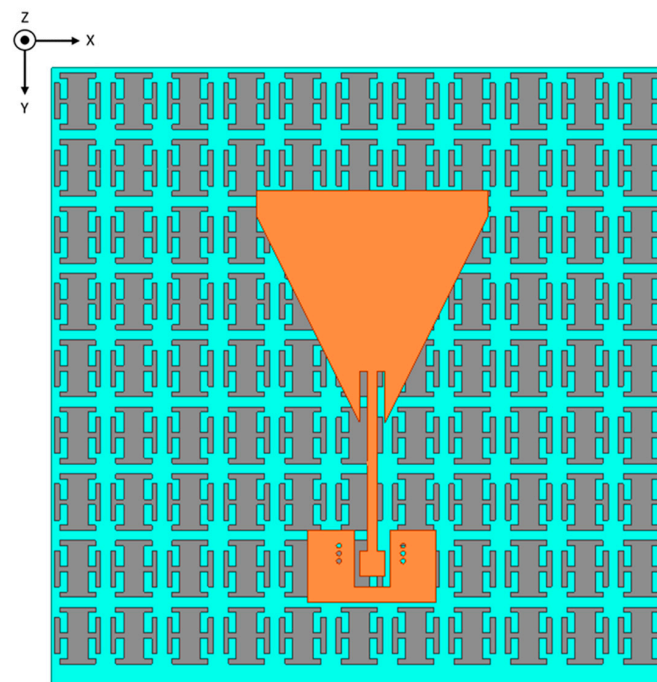

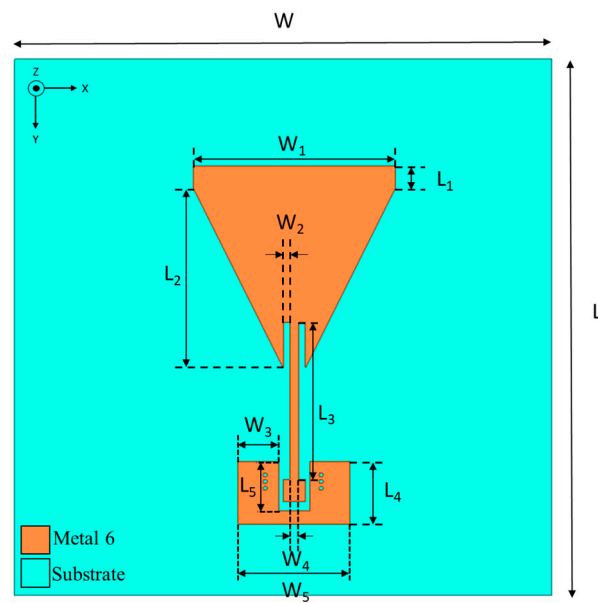**Figure 3.** The geometry of the designed monopole patch antenna and M1 layer AMC.

Figure 4. The geometry of the proposed antenna-on-chip.

Table 1. Detailed value of the proposed antenna.

Parameter	Value (μm)	Parameter	Value (μm)
L	1200	W	1200
L_1	50	W_1	450
L_2	400	W_2	15
L_3	350	W_3	90
L_4	140	W_4	20
L_5	110	W_5	250
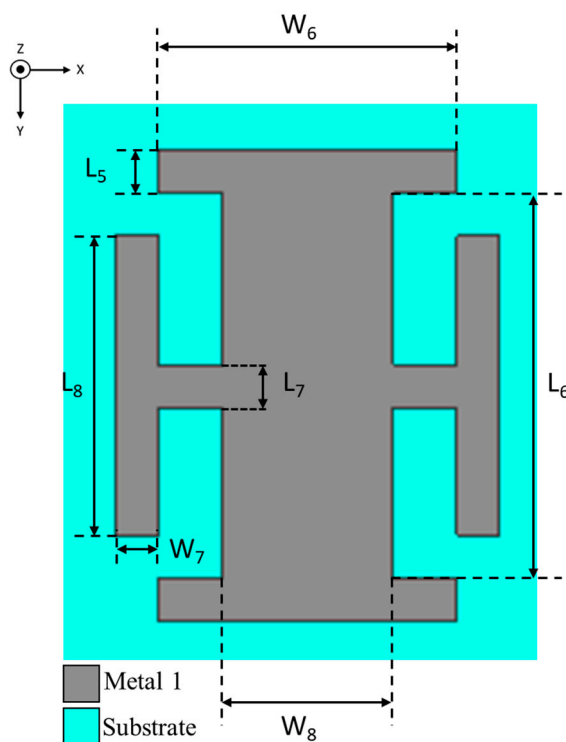
Figure 5. The geometry of AMC in the M1 layer.

Table 2. The detailed value of the proposed AMC.

Parameter	Value (μm)	Parameter	Value (μm)
L_5	10	W_6	70
L_6	90	W_7	10
L_7	10	W_8	40
L_8	70		
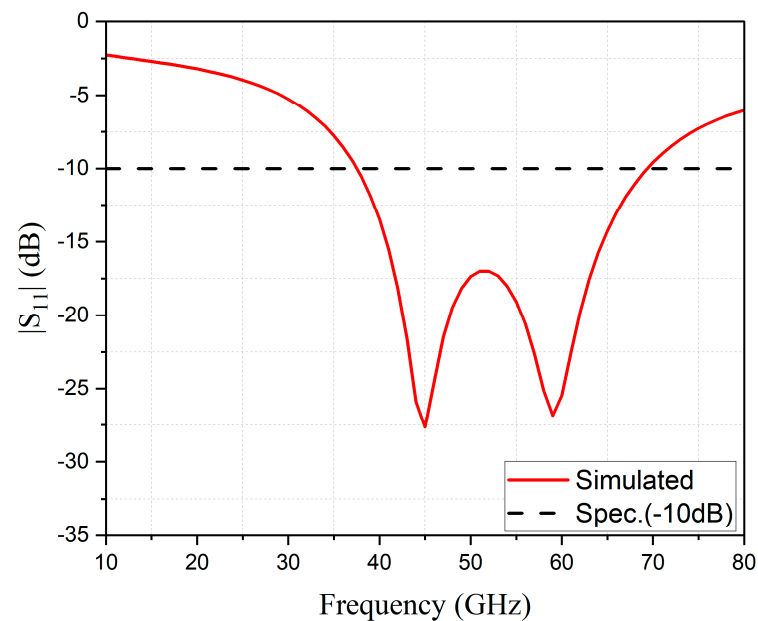
Figure 6. Simulated S11 of the antenna.
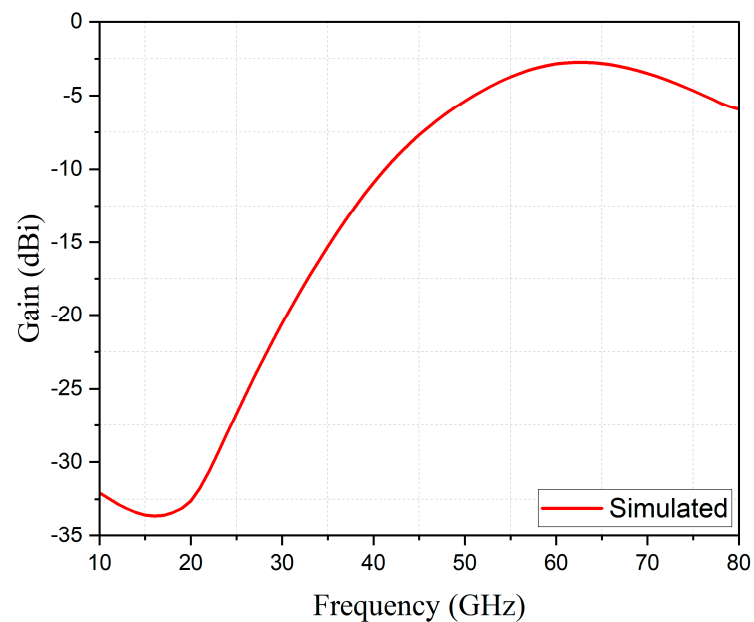
Figure 7. Simulated gain of the antenna.

The parameters of the antenna structure designed in this paper are analyzed to obtain the maximum radiation gain. As shown in Figure 8, the length of the feeder transmission line of this antenna structure is analyzed, and the detailed size and bandwidth are shown in Table 3. When the feed-in line length L_3 is 200 μm, the frequency bandwidth is 35 GHz when the reflection coefficient of the frequency band is lower than −10 dB, but

the minimum reflection coefficient is only −13 dB. Moreover, when the length L_3 of the feed line is increased to 350 μm, the bandwidth is 11 GHz when the reflection coefficient of the frequency band is lower than −10 dB, and the minimum value of the reflection coefficient reaches −20 dB. Finally, when the length L_3 of the feed-in line increases to 450 μm, the bandwidth is 9 GHz when the reflection coefficient of the frequency band is lower than −10 dB. Therefore, through parameter analysis, the optimal length L_3 of the feed-in transmission line can be known, so 350 μm is selected for the length L_3 of the feed-in transmission line to obtain the best bandwidth and minimum reflection coefficient.
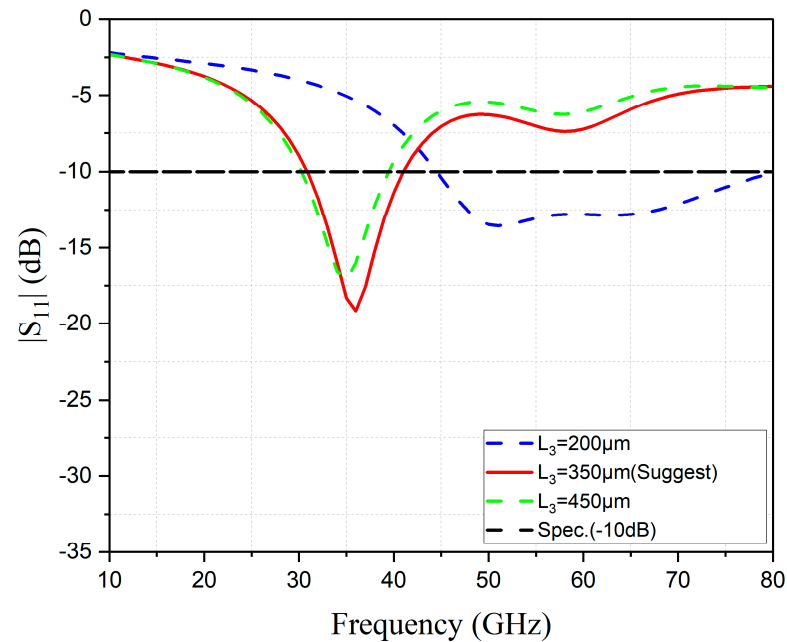
Figure 8. Reflection coefficient of L_3 variation.

Table 3. The bandwidth of L_3 variation.

Value (μm)	Bandwidth (GHz)
200	44.5 GHz~80.5 GHz
350	30 GHz~41 GHz
450	30 GHz~39 GHz

Through parameter analysis, the graphic unit of the M1 layer AMC is designed. It can be seen from Figure 9 that two types of AMCs are designed in this paper, and it can be known that the type of AMC will affect the reflection coefficient (S11) from the Figure 10. In the first type, it can be known that the bandwidth is only 6 GHz under the reflection coefficient standard −10 dB. In the second type, it can be known that, under the reflection coefficient standard −10 dB, a wider bandwidth and a smaller reflection coefficient are obtained. Therefore, the second type in AMC is chosen for the best performance.
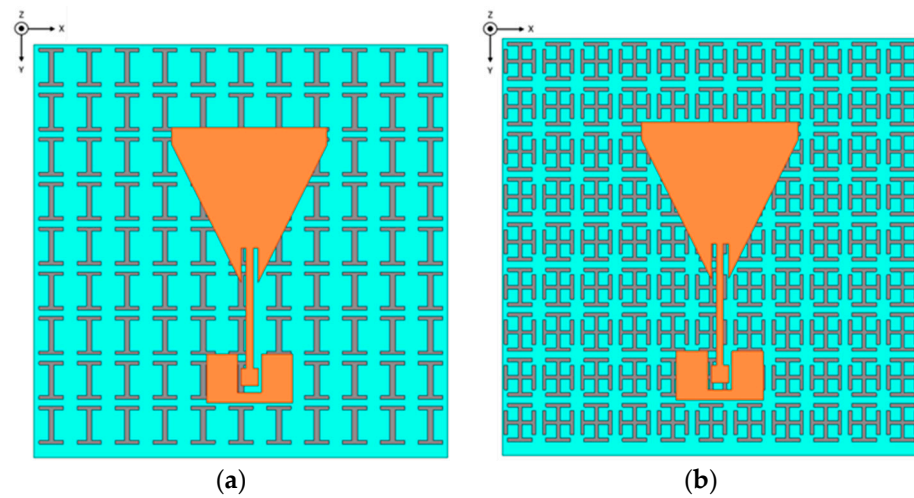
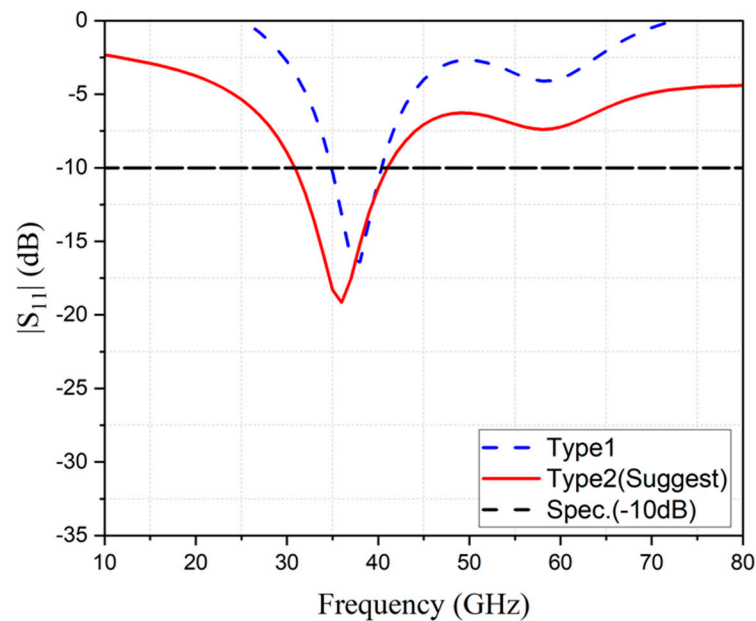**Figure 9.** The type of the proposed AMC: (**a**) Type 1; (**b**) Type 2.

Figure 10. Reflection coefficients (S11) of different types of AMC.

The graphics unit of the M1 layer AMC was analyzed by parametric analysis. It can be known from Figure 11 that the width of the graphic unit pattern will affect the minimum value and bandwidth of the reflection coefficient (S11) in the horizontal structure adjustment of the graphic unit. For example, when the width W_8 of the horizontal structure of the unit pattern is 85 μm, it can be known that, under the reflection coefficient standard of −10 dB, the bandwidth has no obvious tendency to become the surface. Furthermore, when the horizontal frame width of the unit pattern is 90 μm, it can be found that, under the reflection coefficient standard −10 dB, it has a wider bandwidth and a minimum reflection coefficient compared to when W_8 is 85 μm. However, when the horizontal width of the unit pattern reaches 95 μm, it can already be found that the reflection coefficient cannot reach the standard value of −10 dB. Therefore, the lateral structure width of the graphic unit of the AMC of the M1 layer is selected to be 90 μm to obtain the best performance.
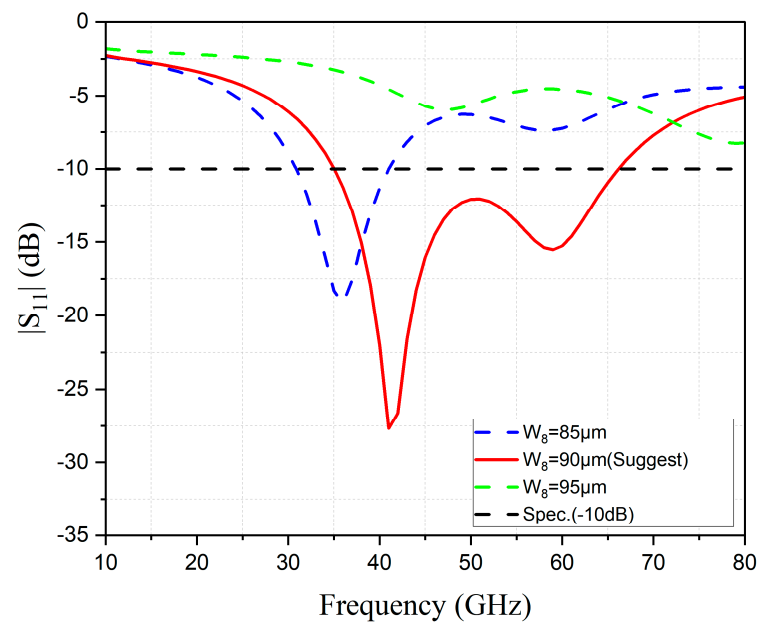
Figure 11. Reflection coefficient of W_8 variation.

The AMC with different periodic array sizes is analyzed, as shown in Figure 12. For example, it can be seen from Figure 13 that, in the AMC with a regular array size of 7×9, it can be known that the minimum reflection coefficient (S11) is -18 dB. On the other hand, in an AMC with a regular array size of 9×11, its bandwidth is 31 GHz, with a minimum reflection coefficient (S11) of -27 dB at a standard reflection coefficient of -10 dB. Therefore, an AMC with a regular array size of 9×11 is chosen.

(**a**)   (**b**)
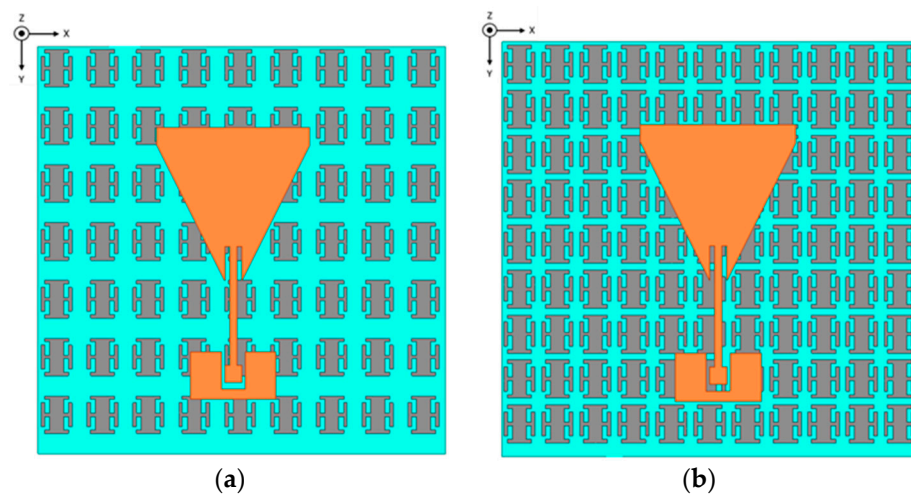
Figure 12. The periodic array size of the proposed AMC: (**a**) Type 1 regular array size is 7×9; (**b**) Type 2 regular array size is 9×11.
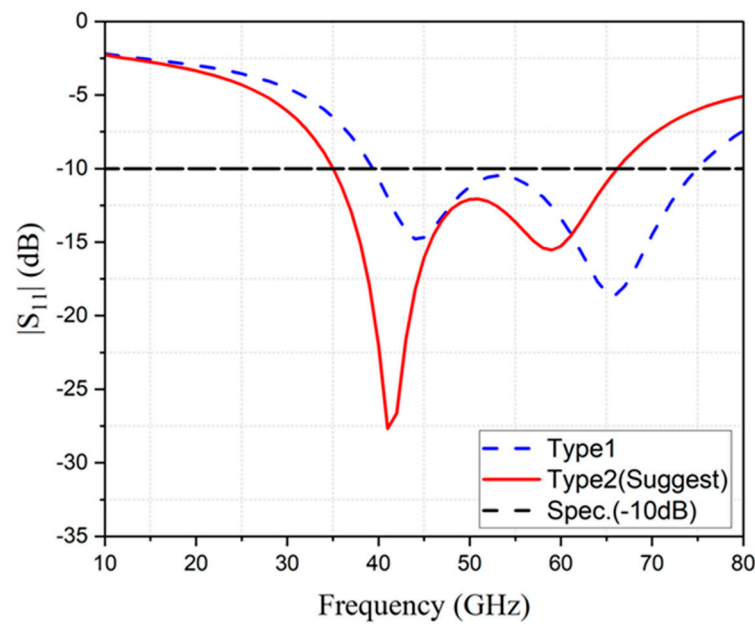
Figure 13. Reflection coefficients (S11) of different periodic array sizes of AMC.

Next, the reflection phase of AMC in the M1 layer is analyzed. Figure 14a is the AMC unit model designed in this paper. It can be known from Figure 14b that the AMC designed in this paper has a phase bandwidth and a high reflection coefficient at an operating frequency of 60 GHz.
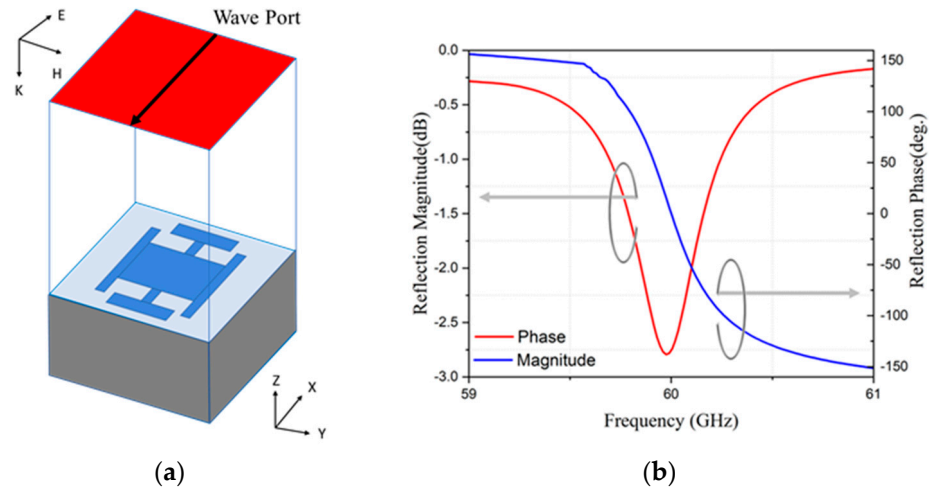

(**a**)	(**b**)

Figure 14. (**a**) Artificial magnetic conductor simulation model; (**b**) Reflection magnitude and phase for AMC.

In Figure 15, parameter analysis is also performed through the presence or absence of M1 AMC. Figure 16 shows that when the AMC is designed with the M1 layer, a lower value of the reflection coefficient (S11) can be obtained. However, when AMC is designed without the M1 layer, the bandwidth cannot continuously reach the standard −10 dB of the reflection coefficient. Therefore, by comparing the simulations, it is possible to analyze the influence on the reflection coefficient of the antenna when designing the AMC with or without the M1 layer.
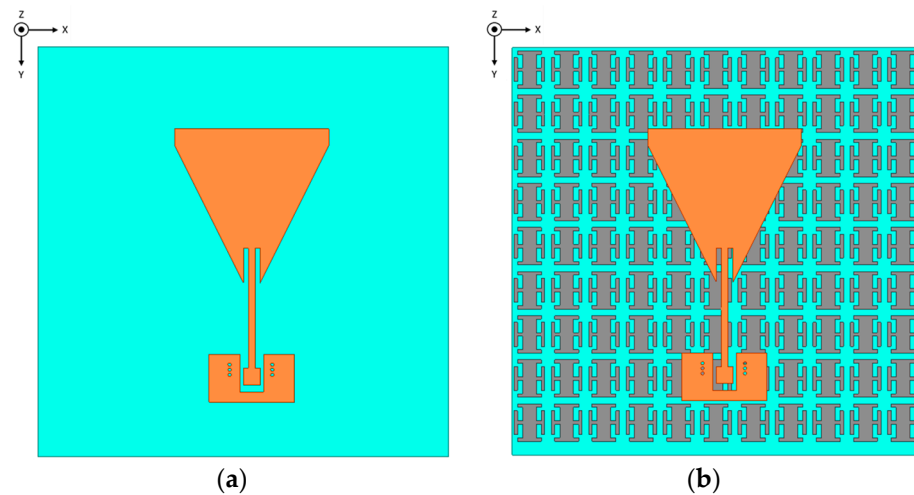
Figure 15. Geometry of the proposed antenna-on-chip: (**a**) Without the M1 layer of AMC; (**b**) With the M1 layer of AMC.
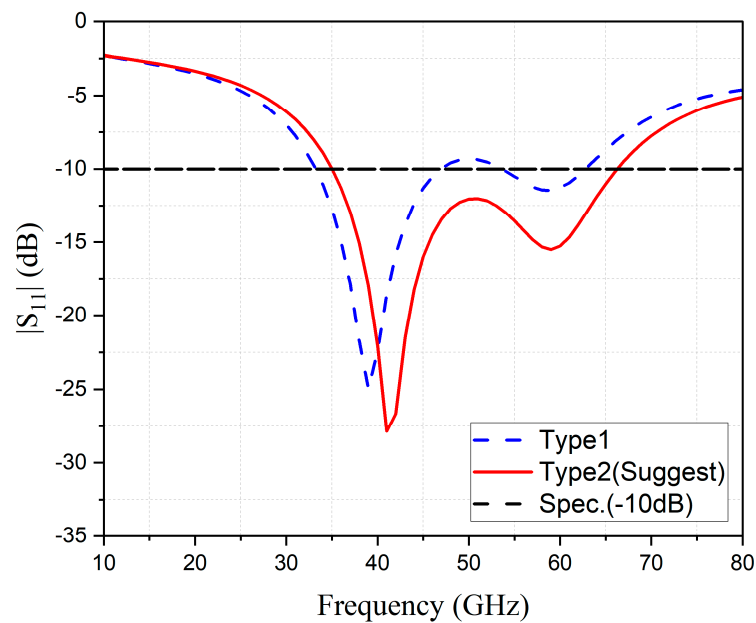

Figure 16. Simulation diagram with and without AMC.

In terms of probe GSG grounding, as shown in Figure 17, in this paper, a circular hole is drilled in the probe grounding area, and the simulation diagram is shown in Figure 18. When the probe GSG grounding area has no holes, and the frequency is 60 GHz, the minimum reflection coefficient is only −14 dB, and the bandwidth is 31 GHz. Then, through the penetration method of the hole in the GSG grounding area, impedance matching is achieved so that the 60 GHz frequency band can reach the standard reflection coefficient of −10 dB, the minimum reflection coefficient can reach −26 dB, and the bandwidth can reach 32 GHz.
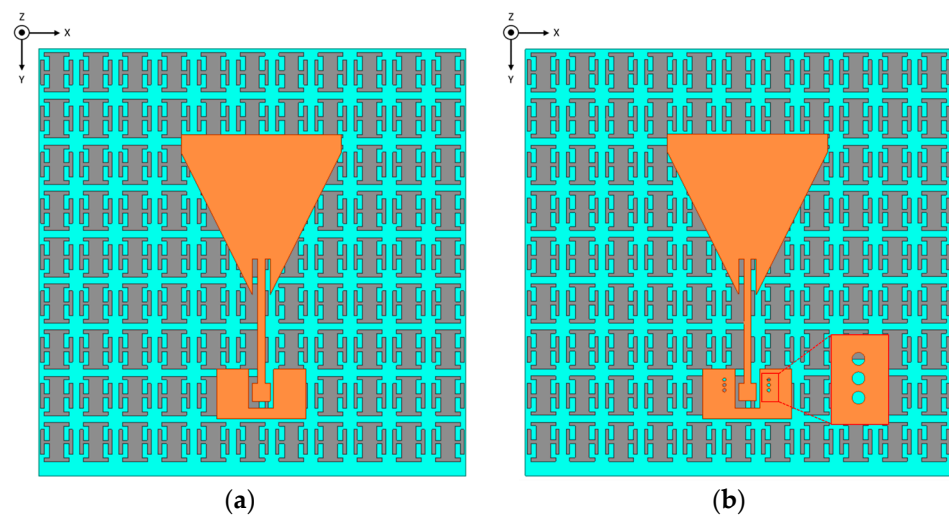
Figure 17. The geometry of the proposed antenna-on-chip: (**a**) Design no holes in the GSG grounding area; (**b**) Design holes in the GSG grounding area.
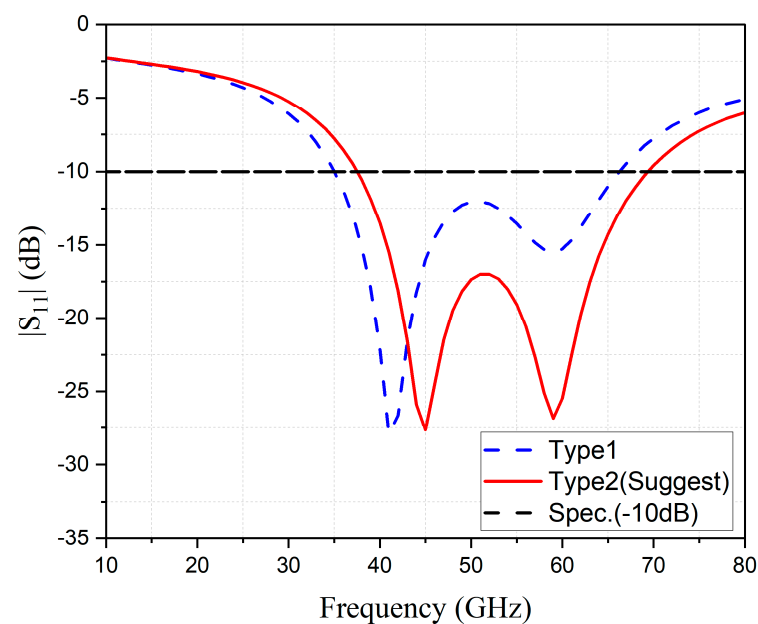

Figure 18. Reflection coefficient of probe GSG grounding with or without holes.

As shown in Figure 19, this paper analyzes the antenna's architectural operation through the current distribution. The antenna designed in this paper uses the probe GSG method to feed the signal, which excites the antenna body to generate the surface current. The current is distributed to the antenna body through the CPW structure of the feeding line. Figure 19a,b show the current distribution state at 38 and 60 GHz. In the 34 GHz to 65 GHz frequency band, the area where the current distribution is more obvious is the area of the tapered patch and its surrounding area. It can be judged that the resonance of the tapered patch antenna generates this frequency band.
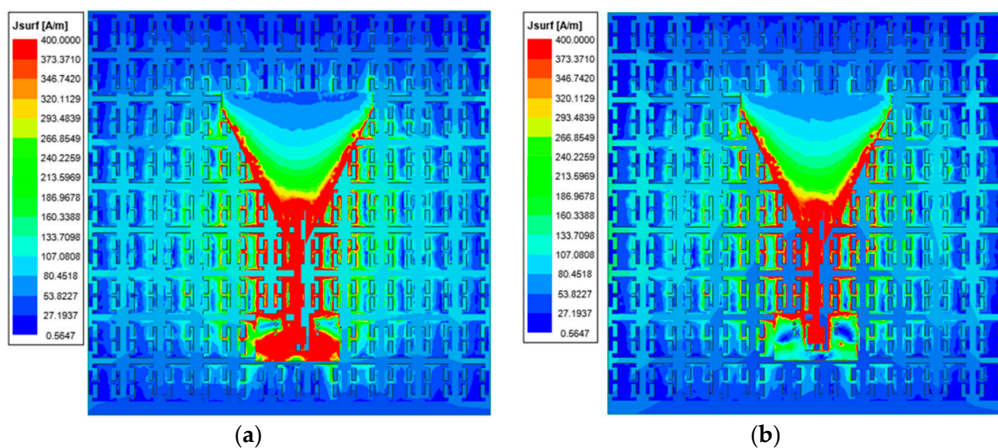
(**a**)   (**b**)

Figure 19. The surface current of the antenna-on-chip: (**a**) 38 GHz; (**b**) 60 GHz.

3. Results

Figure 20 shows the antenna–on-chip designed in this paper, using the GSG probe to perform needle insertion and using the large magnification to measure frontal photos. The measured reflection coefficient (S11) of the antenna designed in this paper was measured at the Taiwan Semiconductor Research Institute of the National Research Institute (Taiwan Semiconductor Research Institute), using a vector network analyzer (Agilent E8361C) as the feed system and using a spacing of 100 μm; the GSG probe transmits signals for the antenna. Figure 21 shows the simulation and measurement results of the millimeter wave band antenna-on-chip designed in this experiment, which have the same trend. However, the difference between the position of the GSG probe and the simulation during the measurement affects the bandwidth result of the measurement, and the bandwidth under the standard reflection coefficient of −10 dB has a higher application frequency than the simulation, covering millimeter wave application frequencies of 28 GHz, 38 GHz, and 60 GHz. The measurement results after the frequency of 67 GHz are unknown, but it can be inferred from the previous measurement trend that the measurement results will be similar to those of the simulation.
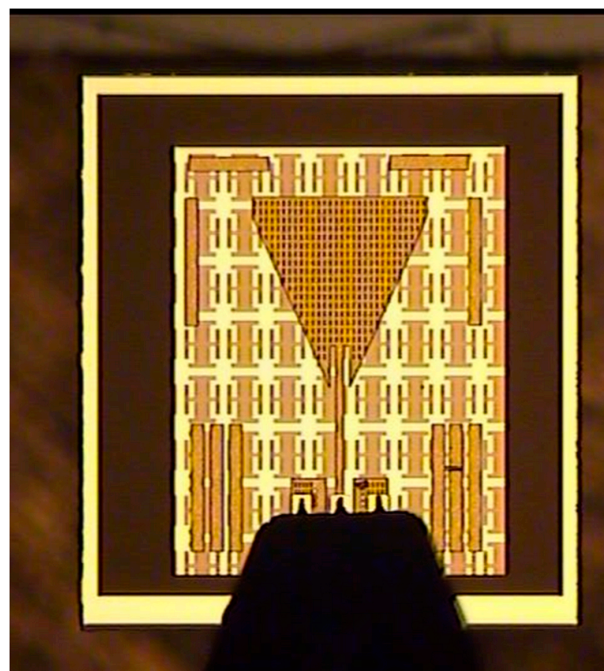

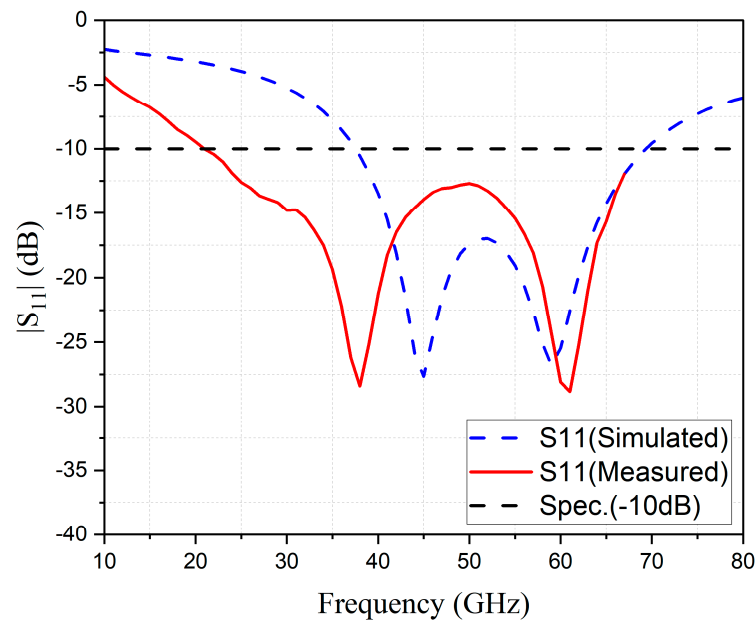**Figure 20.** GSG connector and actual measurement diagram.

Figure 21. Simulation and measurement of reflection coefficient S11.

This paper simulated the radiation direction through high-frequency electromagnetic simulation software regarding the antenna radiation pattern. Through the 2D field pattern, the radiation directions in the xz and yz planes can be analyzed, and the radiation directions of the chip antenna designed in this document at 38 GHz and 60 GHz can be better understood. Figures 22 and 23 are the 2D plane field radiation diagram and the 3D field radiation diagram of 38 GHz. When the theta angle is 1 degree, the maximum gain is −12.2 dBi. The xz plane field radiation diagram shows that when the Theta angle is 2 degrees, the maximum gain is −12 dBi. Figures 24 and 25 are 2D planar field radiation diagrams and 3D field radiation diagrams of 60 GHz. It can be known that when the theta angle is 2 degrees, the maximum gain is −2.64 dBi. The xz plane field radiation diagram shows that when the theta angle is 2 degrees, the maximum gain is −2.56 dBi. According to the above xz, yz plane radiation pattern simulation diagram and 3D radiation simulation diagram, it can be known that the radiation pattern of this antenna is upward, and the maximum gain is −2.64 dBi.
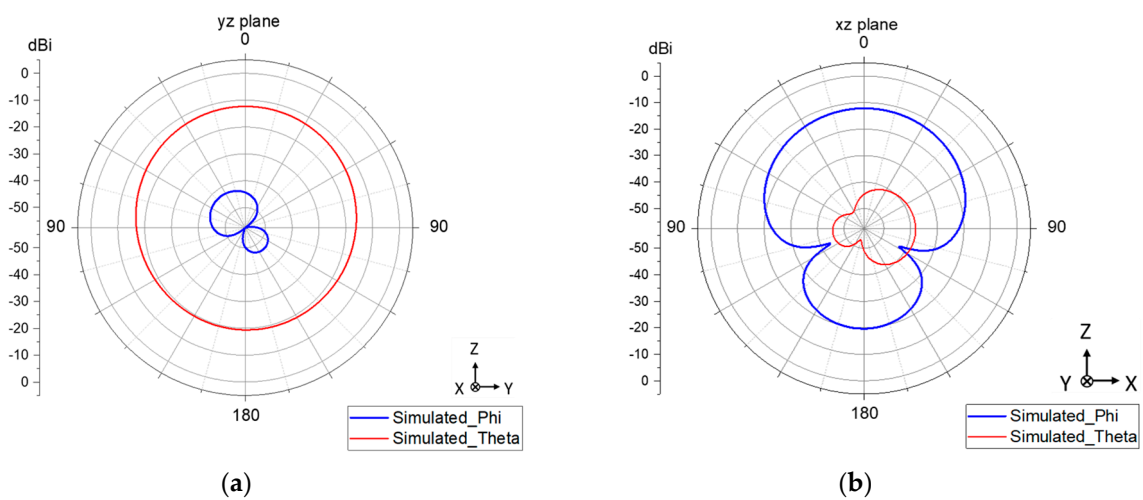

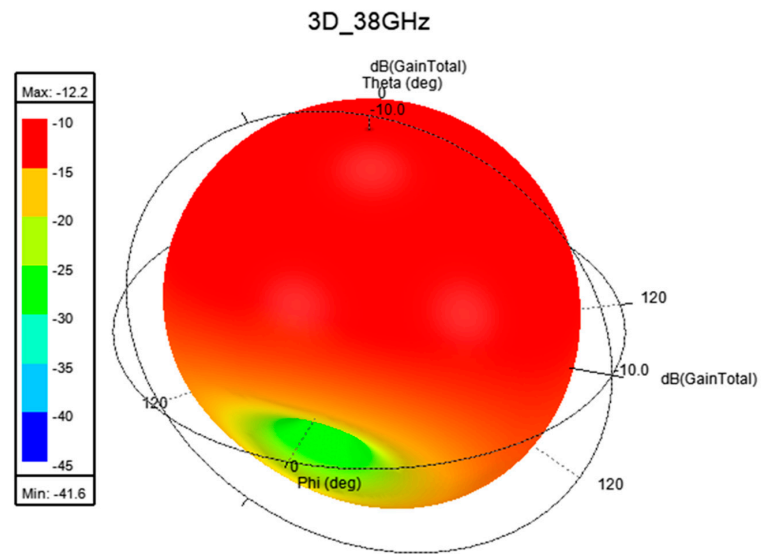**Figure 22.** 2D field simulation at 38 GHz: (**a**) yz plane; (**b**) xz plane.

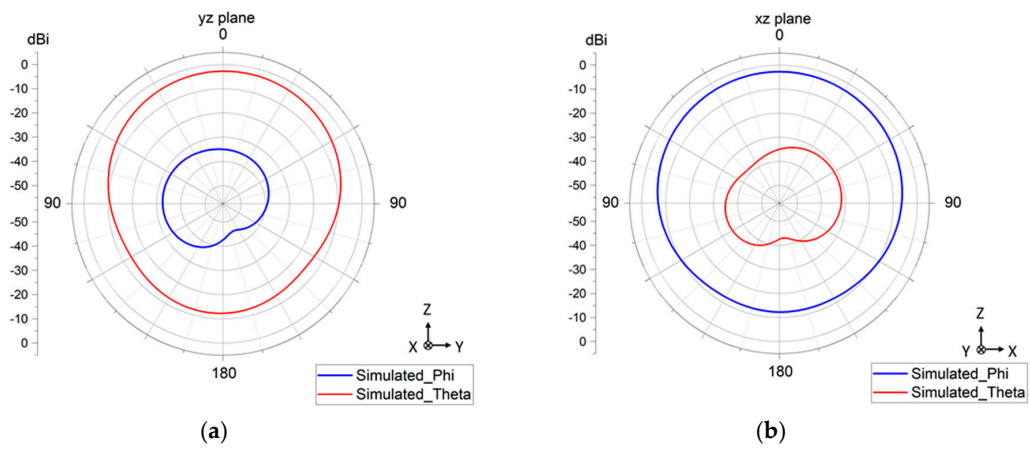**Figure 23.** The 3D field simulation diagram at 38 GHz.

Figure 24. 2D field simulation at 60GHz: (**a**) yz plane; (**b**) xz plane.
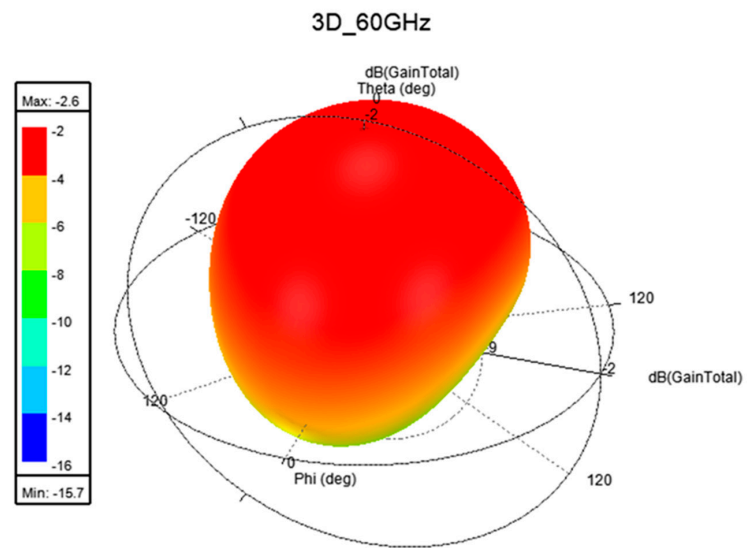

Figure 25. The 3D field simulation diagram at 60 GHz.

4. Discussion

From the above parameter simulation, it can be known that the grounding part of GSG can achieve impedance matching through our hole design so that the design frequency band can reach the standard reflection coefficient of −10 dB and achieve a smaller value of reflection coefficient (S11). By designing AMC in the M1 layer, the antenna-on-chip can achieve a better performance and widen the bandwidth. Coupled with the advantages of the high gain and high directivity of the patch antenna, it can complement the lack of performance of the antenna-on-chip. As shows in Table 4, the measurement results of the antenna designed in this paper are more comprehensive than the bandwidth of the literature [8,9,15,17–23] and have more and broader bandwidth application advantages. In terms of gain, it has a more significant gain value than those in the literature [17,23]. Furthermore, the area part is smaller than the area used in the literature [18,20], using a smaller area to achieve a broader bandwidth.

Table 4. Comparison of the proposed antenna with other research literature.

References	Process	Frequency (GHz)	* FBW	Gain (dBi)	Size (mm^2)
[8]	0.18 μm CMOS	28	84.7%	N/A	1.16 × 0.76
[9]	65 nm CMOS	28 60	5.3% 5.9%	−10 0	0.25 × 0.3
[15]	28 nm CMOS	33	32%	−1.8	0.69 × 0.85
[17]	N/A	77 140	21.28% 35.21%	−3.24 −5.78	0.9 × 0.9
[18]	SiGe	81.5	12.2%	1.61	1.29 × 1.5
[19]	65 nm CMOS	94	25.5%	0.42	N/A
[20]	65 nm CMOS	24	19%	−1	2.5 × 2.5
[21]	0.13 μm CMOS	84	11.76%	−0.58	1 × 1
[22]	0.18 μm CMOS	60	30.5%	0.35	0.63 × 0.46
[23]	N/A	60	17.6%	−20	0.5 × 0.15
Proposed	0.18 μm CMOS	60	104.6%	−2.64	1.2 × 1.2

* FBW = Fractional bandwidth.

5. Conclusions

This paper proposes a monopole patch antenna, and AMC is designed in the M1 layer. Through simulation analysis, it can be known that, without AMC, the antenna bandwidth designed in this paper cannot be lower than the standard reflection coefficient of −10 dB. The design of AMC achieves the minimum reflection coefficient, and the designed bandwidth is lower than the standard reflection coefficient standard of −10 dB. In simulations, the bandwidth ranges from 34 to 65 GHz, with a fractional bandwidth of 104%. At 62 GHz, a maximum radiation benefit value of −2.64 dB is obtained. The measurement obtained a larger bandwidth covering 20.9 GHz to 67 GHz, with a fractional bandwidth of 104.89%. The method proposed in this paper can improve the influence of the antenna-on-chip caused by the CMOS process and can obtain more of a radiation gain and a lower reflection coefficient (S11). As a result, future millimeter wave antennas can be implemented on chips, making the antennas compact and less susceptible to external factors while still having a good radiation gain and efficiency.

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